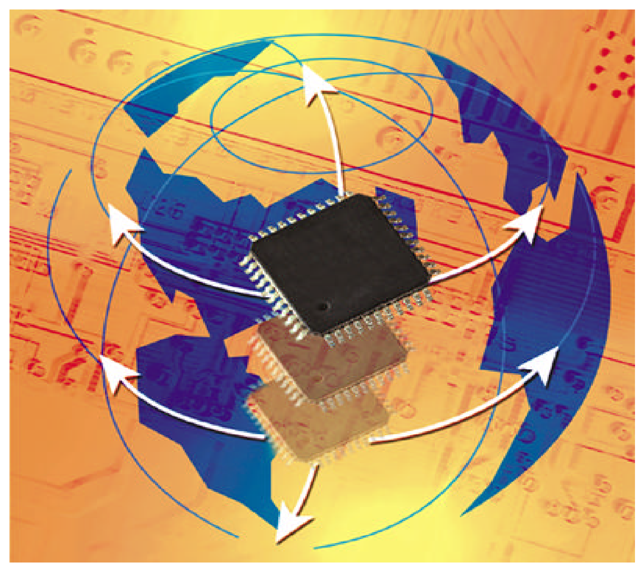
Qualification Package

AT89C51RB2 / RC2 & T89C51IC2

FLASH C51 Microcontrollers



AT89C51RB2 / RC2 & T89C51IC2

June 2002

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2 General Information

Product Name:	AT89C51RC2 / RB2
Function:	8-bit Microcontrollers with 32KB / 16KB FLASH
Product Name:	T89C51IC2
Function:	8-bit Microcontroller with 32KB FLASH Two Wires Interface (TWI), 32KHz Oscillator
Wafer Process:	Logic CMOS 0.35um with embedded FLASH
Available Package Types	PLCC 44, VQFP 44 1.4mm, PDIL40 *(not available for T89C51IC2)*
Other Forms:	Die, Wafer
Locations:	
Process Development,	Atmel Colorado Springs, USA
Product Development	Atmel Nantes, France
Wafer Plant	Atmel Colorado Springs, USA
QC Responsibility	Atmel Nantes, France
Probe Test	Atmel Colorado Springs, USA
Assembly	Dependant upon Package
Final Test	Dependant upon Package
Lot Release	Atmel Nantes, France
Shipment Control	Global Logistic Center, Philippines
Quality Assurance	Atmel Nantes, France
Reliability Testing	Atmel Nantes, France
Failure Analysis	Atmel Nantes, France

Quality Management
Atmel Nantes, France

Signed: Pascal LECUYER

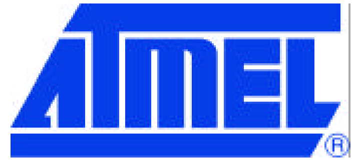
3 Technology Information

3.1 Wafer Process Technology

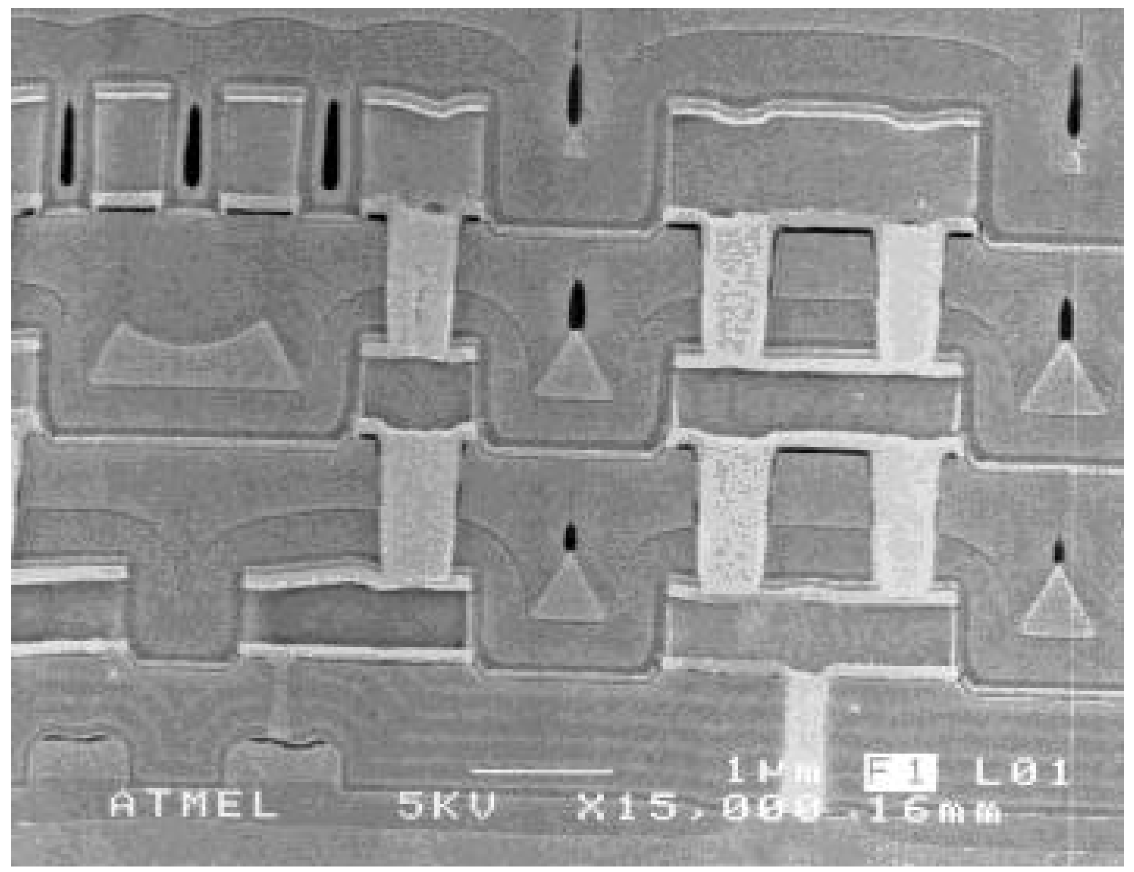
Process Type (Name):	Logic 0.35um with embedded FLASH (AT56800)
Base Material:	Epitaxied Silicon
Wafer Thickness (final)	475um
Wafer Diameter	150mm
Number Of Masks	27
Gate Oxide (Logic transistors)	
Material	Silicon Dioxide
Thickness	68 A
Gate Oxide (EPROM cell)	
Material	Silicon Dioxide
Thickness	390 A
Polysilicon	
Number of Layers	2
Thickness Poly 1	1400A Amorphous
Thickness Poly 2	3200A
Metal	
Number of Layers	3
Material:	AlCu
Layer 1 Thickness	5000A
Layer 2 Thickness	5000A
Layer 3 Thickness	8000A
Passivation	
Material	Oxide HDP/ Oxynitride
Thickness	21000A

3.2 Product Design

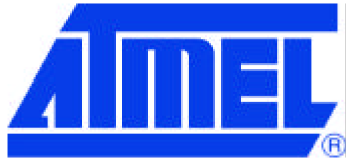
Die Size	14.13 mm^2
Pad Size Openning / Pitch	79um * 91um / 126um
Logic Effective Channel Length	0.35µm
Gate Poly Width (min.)	0.35µm
Gate Poly Spacing (min.)	0.42µm
Metal 1 Width	0.42µm
Metal 1 Spacing	0.49µm
Metal 2 Width	0.56µm
Metal 2 Spacing	0.49µm
Metal 3 Width	0.56µm
Metal 3 Spacing	0.49µm
Contact Size	0.35µm
Contact Spacing	0.42µm
Via 1 Size	0.42µm
Via 2 Size	0.42µm



3.3 Device cross section



AT56Kxx cross section



4 Qualification

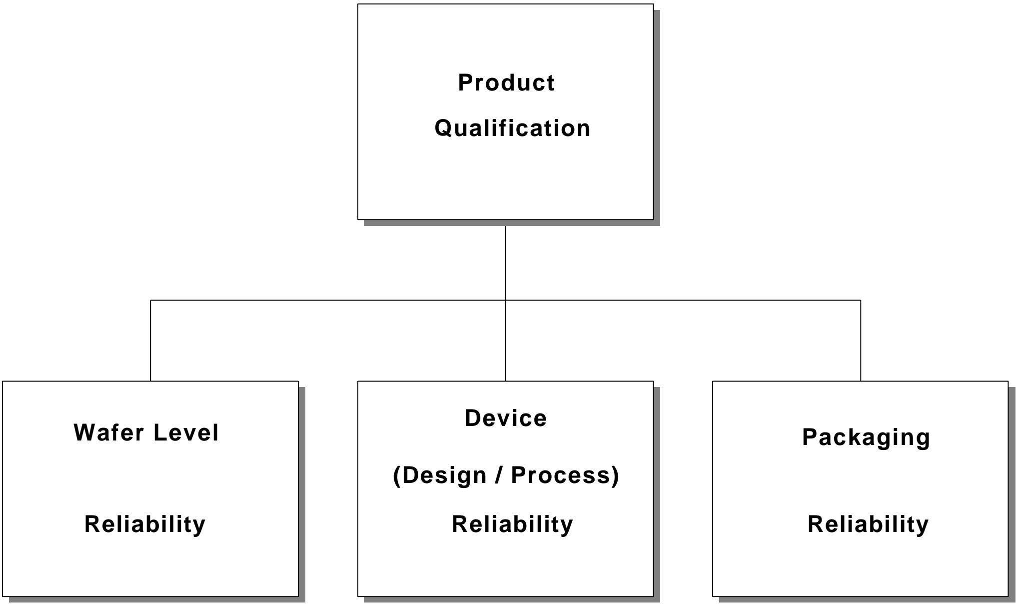
4.1 Qualification methodology

All product qualifications are split into three distinct steps as shown below. Before a product is released for use, successful qualification testing are required at wafer, device and package level.

- Wafer Level Reliability consists in testing individually basic process modules regarding their well known potential limitations (Electromigration, Hot Carriers Injection, Oxide Breakdown, NVM Data Retention). Each test is performed using wafer process specific structures.

- Device reliability is covering either dice design and processing aspects. The tests are performed on device under qualification, but generic data may also be considered for reliability calculation.

- For each package type proposed in the Datasheet, it is verified that qualification data are available. If not qualification tests are carried out for the new package types. In addition, one package type is selected to verify packaging reliability of the device under qualification.



4.2 Qualification test methods

General Requirements for Plastic packaged CMOS Ics.

Standard	Test Description	Acceptance
MIL-STD 883 Method 1005	**Electrical Life Test (Early Failure Rate)** 48 hours 140°C	0/300 - 48h
MIL-STD 883 Method 1005	**Electrical Life Test (Latent Failure Rate)** 1000 hours 140°C Dynamic or Static	0/100 - 500h
MIL-STD 883 Method 3015.7	**Electrostatic Discharge HBM** +/-2000v 1.5kOhm/100pF/3 pulses	0/3 per level
JEDEC 78	**Latch up** 50mW power injection, 50% overvoltage @125°C	0/5 per stress
AEC Q100 Method 005	**NVM Endurance** Program Erase Cycles 25°C	0/50 - 100kc
AEC Q100 Method 005	**NVM Data Retention** High Temperature Storage 165°C	0/50 - 500h
MIL-STD 883 Method 1010	**Temperature Cycling** 1000 cycles -65°C/150°C air/air	0/50 - 500c
Atmel PAQA0184	**HAST after Preconditioning** 144 hours 130°C/85%RH	0/50 - 72h
EIA JESD22-A101	**85/85 Humidity Test** 1000 hours 85°C/85%RH	0/50 - 500h
EIA JESD22-A110	**HAST** 336 hours 130°C/85%RH/5.5V	0/50 - 168h
EIA JEDEC 20-STD	**Preconditioning** Soldering Stress 220°C/235°c/3 times	0/11 per class
MIL-STD 883 Method 2003	**Solderability**	0/3
MIL-STD 883 Method 2015	**Marking Permanency**	0/5

4.3 Wafer Level Reliability

4.3.1 Electromigration

Purpose:

To evaluate the AT56800, AT35500, and AT37000 processes for Metal 1, Metal 3 & Via Electromigration Reliability.

Test Parameters:

Metal 1 & Metal 3:
Sample Size = 15
Temp = 250C with Joule heating .
J = 3.5E06 A/cm2.

Via:
Sample Size = 15
Temp = 200C with Joule heating.
J = 2.5E06 A/cm2.

Black's Equation Parameters:

Failure Criteria - 10% increase in resistance. Data taken every 1% change.
n = 2
Ea = 0.6eV

Lifetime Predictions:

Metal 1 :
Split 1 - $Tf_{.1\%\ exp}$ = ~ 28 hrs $Tf_{.01\%\ op}$ = ~ 28 hrs x 39706 accel = **127 years**.
(Sigma = 2.7118 hours, $Accel_{temp}$ = 130, $Accel_{current}$ = 306)

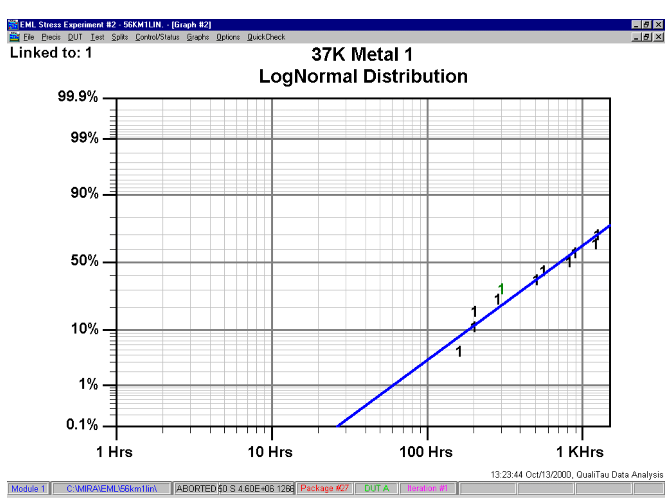
Metal 3 :
Split 3 - $Tf_{.1\%\ exp}$ = ~ 140 hrs $Tf_{.01\%\ op}$ = ~ 140 hrs x 39706 accel = **634 years**.
(Sigma = 1.8782 hours, $Accel_{temp}$ = 130, $Accel_{current}$ = 306)

VIA :
Split 4 - $Tf_{.1\%\ exp}$ = ~ 22 hrs $Tf_{.1\%\ op}$ = ~ 22 hrs x 7144 accel = **18 years**.
(Sigma = 2.59 hours, $Accel_{temp}$ = 31.75, $Accel_{current}$ = 225) (9/15 fails)

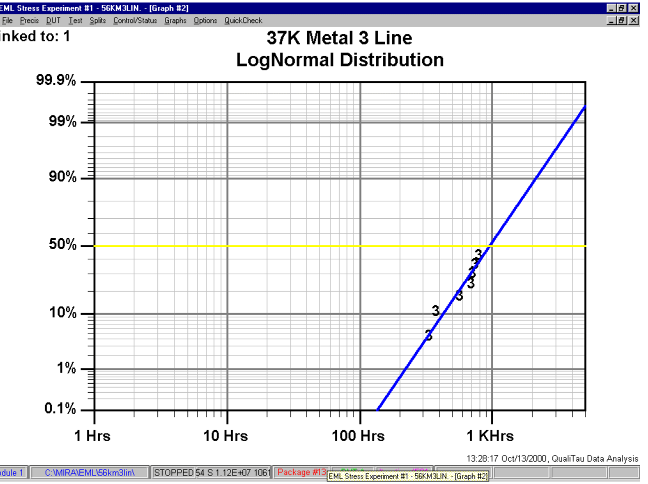
Conclusion:

All splits pass the minimum 10 years lifetime.

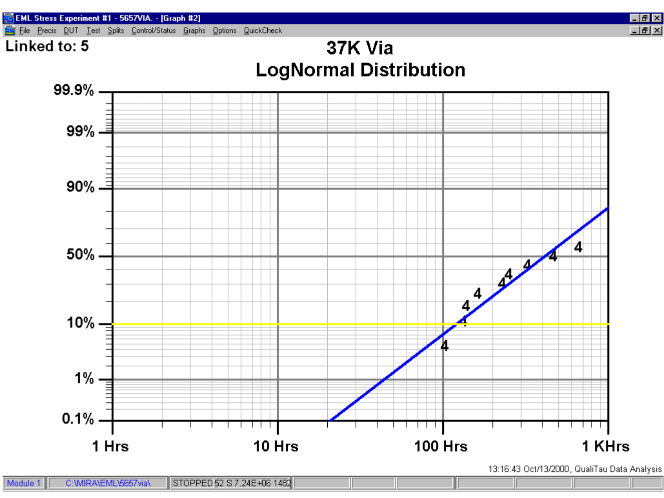
Test results :



AT56800 metal 1 results



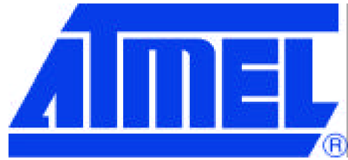
AT56800 metal 3 results



AT56800 VIA results

Electromigration summary table:

Level	Sample Size	Fails @ 10%	Tf.1% Lifetime (yrs)
M1	15	9	140
M3	15	7	1088
Via	15	9	19



4.3.2 Hot carriers injection

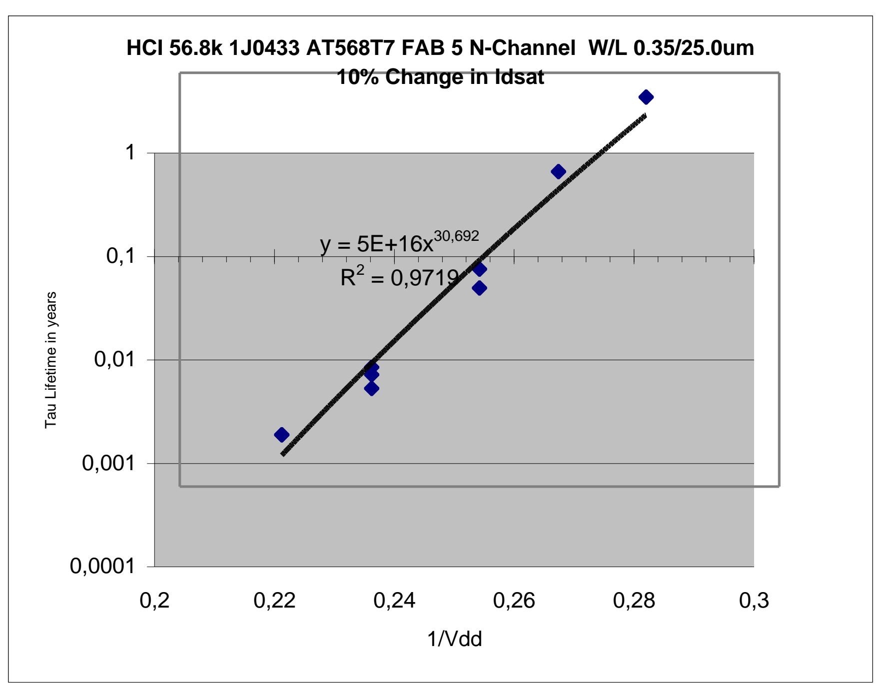
Test conditions

The test is performed by forcing a high drain bias on the test device (Vds>Vddmax) to accelerate the carriers to the maximum. At the same time the gate bias (Vgs) is chosen in order to maximize the injection of carriers into the gate oxide and also the substrate. WLR_B n-channel W/L 0.35um/25um the stress is performed on a number of transistors, each at a different stress condition Vds,stress and Vgs,stress. For each transistor, the time to reach the failure criteria (dIdsat/Idsat=10%) is obtained. NMOS is more sensitive to hot carriers compared to PMOS. Consequently NMOS is the only structure tested.

Measurement

AT568T7 lot 1J0433 has been measured using the WLR_B hot electron structure with standard drain.
NMOS W/L = 25/0.35um.

Results



Conclusion

The extrapolated life time in the worst case conditions (@Vds=Vdd max & Vgs set to maximize substrate current) is much greater than 0.2 years in DC mode (qualification requirement) which is equivalent to more than 10 years in AC mode.

4.3.3 Time Dependent Dielectric Breakdown

Purpose:

To evaluate the AT56800 thin gate oxide TDDB performance as follows:

a) To determine the activation energy of gate oxide failures on STI active edge capacitors
b) To determine the field acceleration factor for intrinsic gate oxide failures
c) To determine the sigma the lognormal standard deviation of the time to breakdown distribution of the intrinsic gate oxide

Test Parameters:

Lot 9G3470 (wafers 4, 5, 18)
Min thickness: 72.9A
Max thickness: 74.7A
Capacitor size: 6.267um^2

The stress conditions used are shown below:

Temperature/Field	9.5MV/cm	10.0MV/cm	10.5MV/cm
225C	N=5	N=5	N=5
200C	N=5	N=5	N=5
175C	N=5	N=5	N=6

Accumulated total stress time: 132 hours / 46 capacitors

Calculation Parameters:

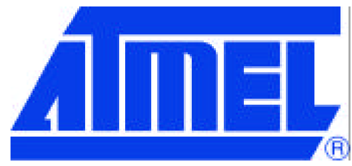
Failure Criteria: 0.01% failures
Temp/Voltage use: 105°c / 3.3v
Oxide thickness: 63A (target –10%)

Lifetime Prediction:

The equation used to describe the breakdown of gate oxides is:

Tbd(i) = exp(SIGMA*Z(i) + GAMMA*Eox +Ea/kT + T0)

Where
Tbd(i) is the time to breakdown of the ith capacitor,
SIGMA is the lognormal standard deviation of the breakdown distribution,
Z(i) is the Z-score of the ith capacitor (essentially the difference between its breakdown time and the mean measured in standard deviations),
GAMMA is the Field acceleration constant,
Eox is the oxide field,
Ea is the activation energy of this failure mechanism,
K is Boltzmann's constant,
T is the Kelvin Temperature, and
T0 is a fitting constant.



The best fit coefficients in the regression analysis are:

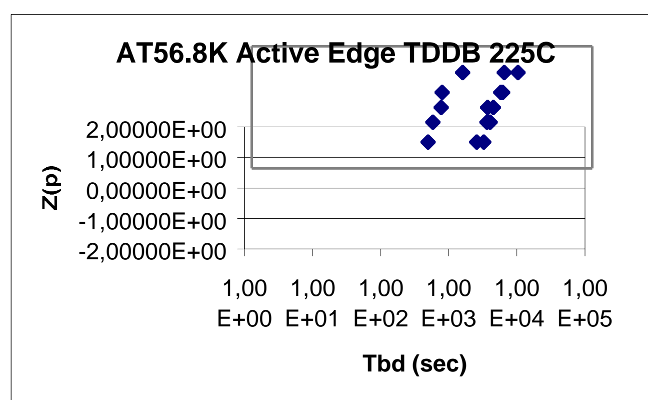
T0= 14.25034317 LN-sec
Ea= 1.060043152 eV
GAMMA= -3.2454227 LN-sec-cm/MV
SIGMA= 0.414655753 LN-sec

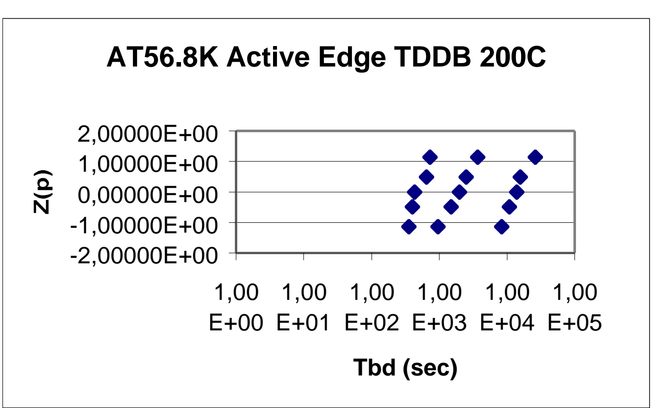
with an adjusted r-squared of 97.99%. The intrinsic lifetime at use conditions calculated from this regression is 56174 years.

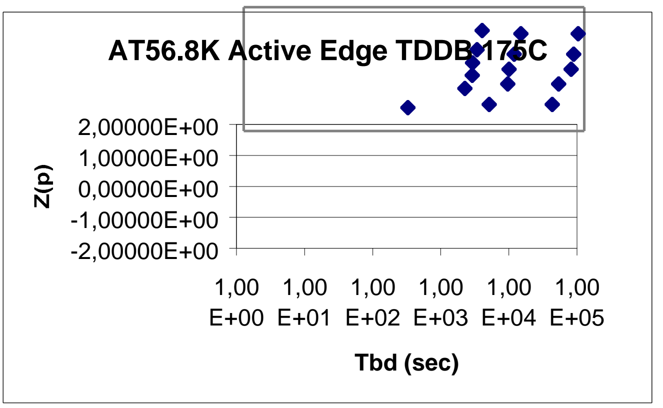
Conclusion:

Using the coefficients determined above, the time to reach any cumulative percent failure level can be estimated given the stress conditions. Using 105C and 3.3 volts on 63 Angstrom N-Channel gate2 oxide, we may expect 0.01% of capacitors having 6,267 square microns area with 6,174 microns of active edge to fail in about 613 years, exceeding the technology requirement of ten years.

Test results :







4.3.4 FLASH characteristics

4.3.4.1 Cell endurance

Purpose:

To evaluate the ability of memory cell to withstand high number of program/erase cycles without change of electrical characteristics.

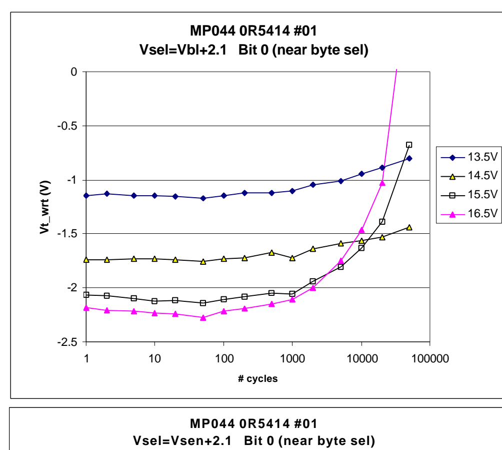
Test Parameters:

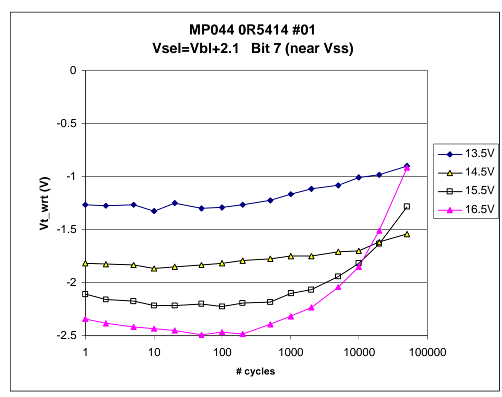
Measurements have been done on lot 0r5414 (MP044 reticle).
Test done on 2 cells in a byte :

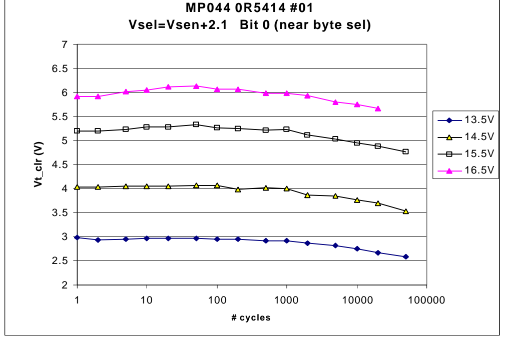
- cell near byte select transistor, called bit0 (1st column)
- cell near Vss contact, called bit 7 (8th column).

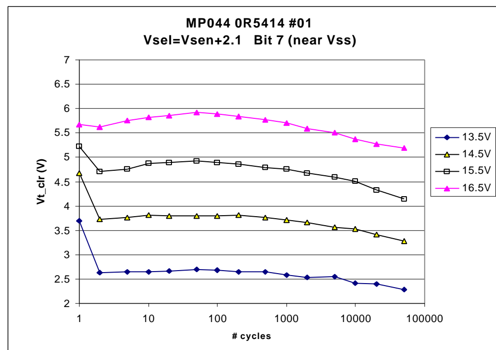
Cycling is done for various programming voltages :

- write : @5ms	13.5V on BL / 15.6V on select 14.5V on BL / 16.6V on select 15.5V on BL / 17.6V on select 16.5V on BL / 17.6V on select	- clear : @5ms	13.5V on sense / 15.6V on select 14.5V on sense / 16.6V on select 15.5V on sense / 17.6V on select 16.5V on sense / 17.6V on select









Conclusions:

- Vt_wrt shift of 200mV after 10k cycles
- I_read decrease of 2.5uA after 10kcycles (- 7 to 9 %)
- No big difference between bit0 and bit 7 in terms of Vt or current variations Using the coefficients

4.3.4.2 Cell retention

Purpose:

To extrapolate cell life duration at 125°c from bake measurements at high temperature.

Test parameters:

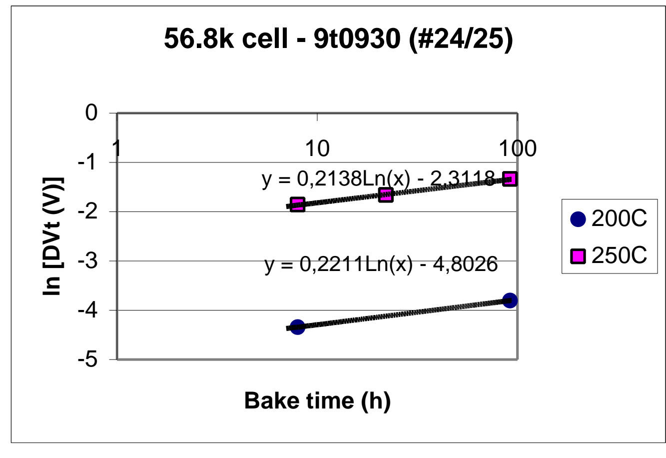
Lot: 9T0930
Temperature: 250°c and 200°c
Duration: 92 hours

Lifetime Prediction:

The equation used to describe memory cell retention is:

DVt (V) = A * (t[h])^m * exp (-1.05eV/kT[K])

Results :



Test measurements

Extrapolated Life Time

Conclusions :

Extrapolation to 125C - 10years = Vt loss is less than 0.8mV

4.3.4.3 Cell Read Disturb

Purpose:

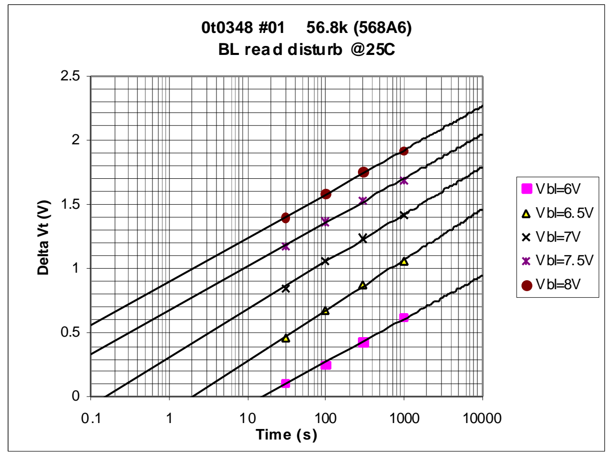
To measure read disturb influence on 56k8 memory cell.

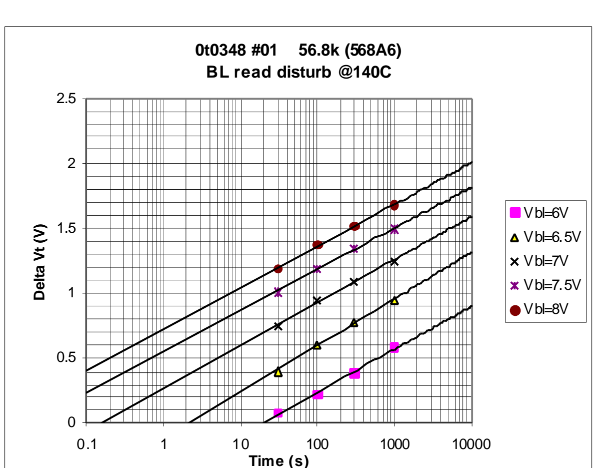
Test parameters:

Lot: 0t0348
Programming: 14V on WL and sensegate @5ms
Temperature: 25°c and 140°c

The cell is stressed with BL voltage much higher than standard read conditions (around 6V) to accelerate disturb phenomenon : electrons from the Floating gate can move through the tunnel oxide. This charge loss is measured after stress by a Vt measurement.

Test results:





Conclusion:

Extrapolation to 10 years lifetime give a maximum BL voltage of around 4V in read operation, which is much higher than nominal BL read voltage (~1V). So there is no sensitivity to read disturb either at room temperature or high temperature.

4.3.4.4 Wafer probe Data retention measurement

Data retention has been verified after bake for 168 hours at 250°C on 3 wafers of a standard production lot. The results are summarized in the table below:

Lot	Wafer	% Retention loss	Failure rate extrapolation at 55°C	Time to failure
1G4448	6	0%	3.91fit	>> 10 years
1G4448	8	0%	4.19fit	>> 10 years
1G4448	12	0%	3..96fit	>> 10 years
Total		0%	1.34fit	>> 10 years

Conclusion:

Data Retention measurements at wafer probe stand out high data retention capability of AT56800 products, exceeding the technology requirement of ten years.

4.4 Device reliability

4.4.1 AT89C51RB2 / RC2 & T89C51IC2 tests

AT89C51RC2 test results are summarized in the table below:

Lot	Device Type	Test Description	Step	Result	Comment
A00498A	T89C51RC2 PLCC 44	EFR Dynamic Life Test	12h 48h	0/270 0/266	
		LFR Life Test	168h 500h 1000h	0/100 0/100 0/100	
A00637B	T89C51RC2 PLCC 44	EFR Dynamic Life Test	12h 48h	0/350 0/350	
		LFR Life Test	168h 500h 1000h	0/100 0/100 0/100	
		FLASH Data Retention	500h 1000h	0/50 0/50	
		FLASH Endurance	10kc	0/33	
A00366	T89C51IC2 PLCC 44	ESD-HBM Model	2000V 3000V 4000V	0/3 0/3 3/3	Class 2 of MIL STD 883 Functional
		LATCH-UP Over-Voltage Power Injection	 5.5v 50mW	 0/5 0/5	Test done at 90°c Classified latch-up free in commercial and industrial range

4.4.2 AT89C51RB2 / RC2 & T89C51IC2 reliability calculation

In the next table, it is proposed a AT89C51RC2 reliability prediction calculated at 55°c for 60% confidence level from generic test data collected during the 12 last months process monitor.

Lots	Device Type	Test Description	Step	Result	Comment
A00151S A00712 A00588A	T89C51CC01 TQFP 44	EFR Dynamic Life Test	48h	1/809	1 Icc drift caused by a contact particle
		LFR Life Test	1000h	0/264	
A00498A A00637B	T89C51RC2 PLCC 44	EFR Dynamic Life Test	48h	1/616	1 Ipd drift caused by an interlayer oxide thinning
		LFR Life Test	1000h	0/200	
A00330K A00365J	T83C51IC2 PLCC 44	EFR Dynamic Life Test	48h	0/300	
		LFR Life Test	1000h	0/200	
A00470K	T89C51CC02 SOW 28	LFR Life Test	168h	0/100	

Global	All products	EFR Dynamic Life Test LFR Life Test	48h -	2/1725 0/764	1159 ppm 8 fit

4.5 AT89C51RB2 / RC2 & T89C51IC2 Packaging reliability

In this section are presented the packaging qualification measurements carried out for AT89C51RC2 in PLCC 44.

Lots	Device Type	Test Description	Step	Result	Comment
A00498A	T89C51RC2 PLCC44	85/85 Humidity	168h 500h 1000h	0/50 0/50 0/50	
		Thermal Cycles	200c 500c 1000c	0/50 0/50 0/50	
		HAST & Thermal shocks post Preconditioning L1	72h 144h	0/50 0/50	
		Preconditioning Level 1	SAM Visual Elect.	0/22 0/50 0/50	
A00637B	T89C51RC2 PLCC 44	85/85 Humidity	168h 500h 1000h	0/50 0/50 0/50	
		Thermal Cycles	100c 500c 1000c	0/50 0/50 0/50	
		HAST & Thermal Shocks post Preconditioning L1	72h 144h	0/50 0/50	
		Preconditioning Level 1	SAM Visual Elect.	0/22 0/50 0/50	

4.6 AT89C51RB2 / RC2 & T89C51IC2 Qualification status

Atmel digital 0.35um wafer process is qualified since 1999, October.

Derived from this technology, the AT89C51RC2 has demonstrated high reliability all over the various testing reported in this document. Full qualification has been pronounced on 2002, January.

5 Environmental Information

Atmel Nantes Environmental Policy aims are :

- Reducing the use of harmful chemicals in its processes

- Reducing the content of harmful materials in its products

- Using re-usable materials wherever possible

- Reducing the energy content of its products

As part of that plan, Ozone Depleting Chemicals are being replaced either by Atmel Nantes or its sub-contractors.

Atmel Nantes site is ISO14001 certified since May 2000.

6 Other Data

6.1 ISO9001 and QS9000 Certificates

CERTIFICAT AFAQ **CERTIFICATE**

N° QS/1999/12758a

AFAQ certifie que le système qualité adopté par,
AFAQ certifies that the quality system developed by :

ATMEL NANTES SA

pour les activités suivantes,
for the following activities :

CONCEPTION ET PRODUCTION DE CIRCUITS INTEGRES ET ASICS.

DESIGN AND PRODUCTION OF INTEGRATED CIRCUITS AND ASICS.

exercées sur le(s) site(s) suivant(s),
carried out in the following location(s) :

La Chantrerie BP 70602 F-44306 NANTES CEDEX 3

a été évalué conformément au code de déontologie de l'annexe B du QS-9000
et jugé conforme aux exigences des référentiels,
has been assessed in accordance with QS-9000 appendix B code of practice
and found to conform to the requirements of the standards :

ISO 9001 (1994) **QS-9000 (03/98)**

Le présent certificat, délivré dans les conditions fixées par AFAQ, est valable à dater du,
This certificate, delivered under AFAQ rules, is valid as from :

2001-01-30

(année-mois-jour) *jusqu'au / until** 2003-07-17 (year-month-day)

Le Président du Comité de Certification *The President of the Certification Committee*	Le Directeur Général d'AFAQ *The Managing Director of AFAQ*	Le Représentant de l'Entreprise *On Behalf of the Firm*
A. PIGEONNIER	O. PEYRAT	F. FAES

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6.2 Data Book Reference

The data sheet is available upon request to sales representative or upon direct access on Atmel web site:

http://www.atmel.com/

Address References
All inquiries relating to this document should be addressed to the following:

Atmel Nantes
BP70602
44306 Nantes Cedex 3
France
Telephone (33) 2 40 18 18 18
Telefax (33) 2 40 18 19 00

Or direct contact
Pascal LECUYER
Telephone (33) 2 40 18 17 73
Telefax (33) 2 40 18 19 00

6.3 Revision History

Issue	Modification Notice	Application Date
0	Initial Product Qualification (T89C51RB2/RC2/IC2)	2002 January
1	Die Size update (AT89C51RB2/RC2 & T89C51IC2)	2002 June

Remarks:

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