



XR-T3591A

Single Chip V.35
Transceiver

November 1998-1

FEATURES

- Single Device Provides Three Receivers and Transmitters Fully Compliant with Electrical Specification of V.35 Interface (Receiver Differential Inputs are V.11 Compliant)
- Supports all V.35 Clock and Data Signals in DTE and DCE Modes of Operation
- Transmitters Are Short Circuit Protected
- Supports A Maximum Data Rate Of 10 MBPS Up To 100 Meters
- Full Compliance with CCITT V.35 Specification
- Supports Mirrored Diagnostic Loopbacks in DTE and DCE Modes of Operation
- Allows Disabling all Receivers, or all Drivers, or all Receivers and Drivers
- During the Disable Mode the Outputs are placed in Hi-Z State
- Maximum Power Dissipation 540mW (All Active Mode)
- Maximum Power Consumption 600mW (All Drivers Loaded)
- Current Consumption During Shut Down Mode is less than 300µA

APPLICATIONS

- Bridges and Routers
- Modems
- Digital Service Units (DSUs)
- Multiplexers
- HDSL and ADSL equipment
- Inverse Multiplexers
- Workstations

GENERAL DESCRIPTION

XR-T3591A is a single chip device which contains three V.35 receivers and transmitters. This device by itself is sufficient to implement all the data and clock signals required for a V.35 interface. For the handshaking signals, separate RS-232 transceivers are necessary.

This device supports multiple modes of operation including DCE and DTE. Diagnostic loopbacks are supported both in the DCE and DTE modes. To accommodate diagnostics in both direction, a mirrored loopback is implemented. Both clock and data paths are looped back during the diagnostics mode. This feature can be invoked by applying appropriate patterns to SEL lines. (See *Table 1.*) For power management flexibility, all of the drivers and receivers can be placed in a shut down mode. For applications where only receivers are

required, all the drivers can be disabled and vice versa. During disable mode the output drivers are placed in Hi-Z state.

The differential V.35 output drivers of this device are implemented using a current mode type design. This minimizes the number of external resistors required. Due to low voltage swing required in the current mode of operation, the emission in a typical V.35 interface using this device is minimized. Each transmitter and receiver would require an external resistor network consisting of 3 resistors for termination. This device does not require any large capacitors in addition to two 0.1µF decoupling caps needed across the power supplies. In order to reduce the number of external components, resistor network can be used to realize both the driver and receiver termination.

ORDERING INFORMATION

| Part No. | Package | Operating Temperature Range |
|-------------|----------------------------|-----------------------------|
| XR-T3591AIP | 24 Lead 600 Mil PDIP | -40°C to +85°C |
| XR-T3591AID | 24 Lead 300 Mil JEDEC SOIC | -40°C to +85°C |

Rev. 1.01

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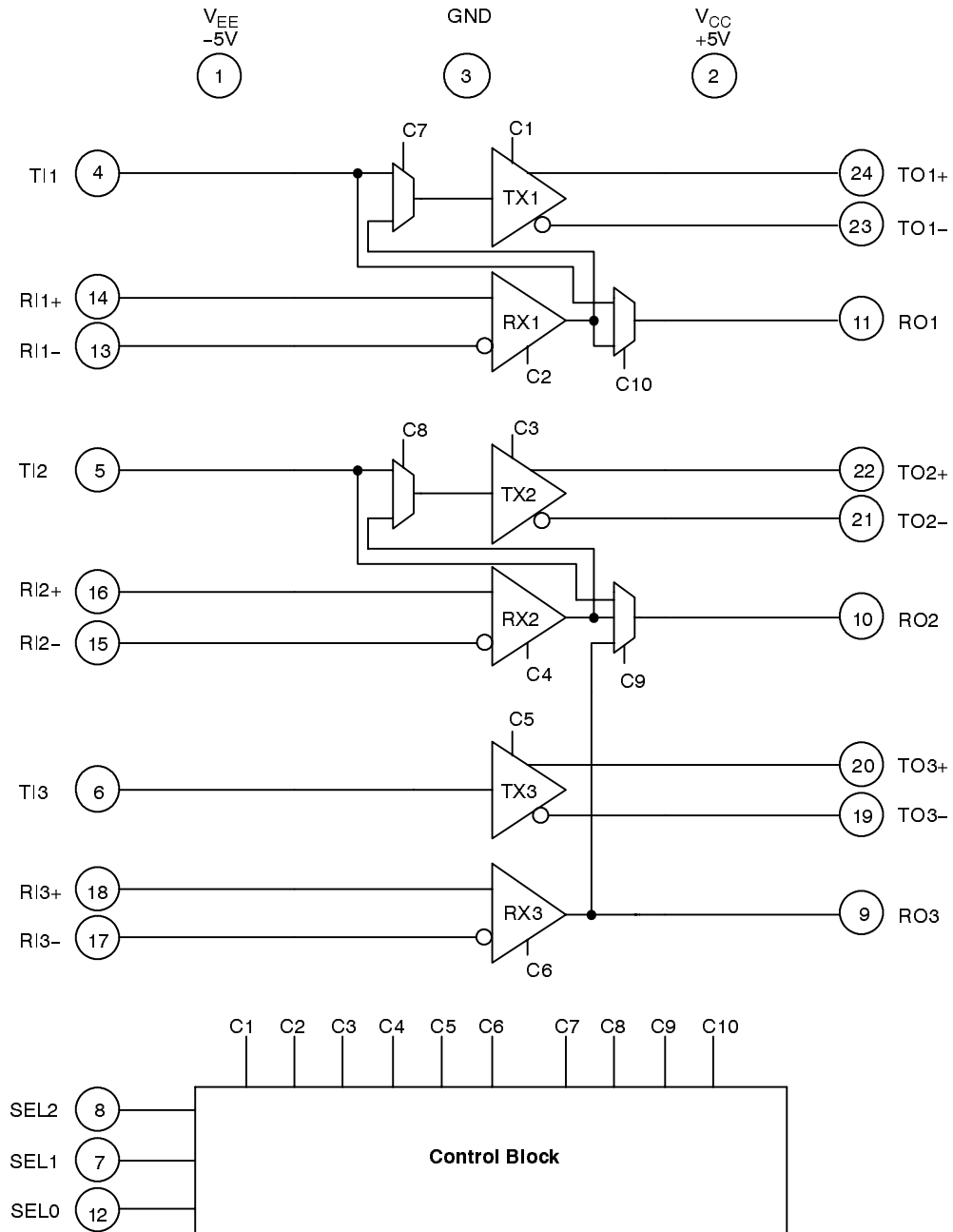
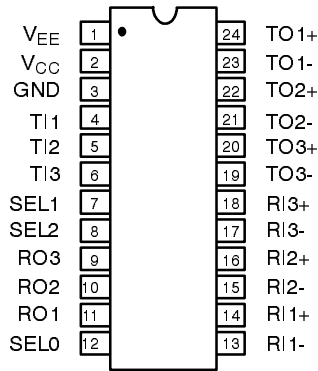
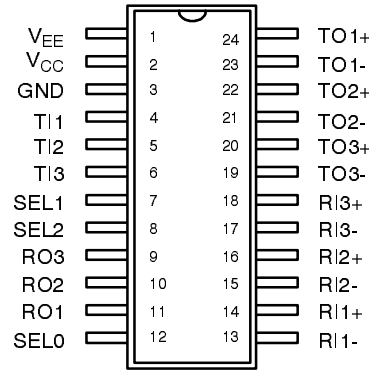


Figure 1. XR-T3591A Block Diagram

PIN CONFIGURATIONS



24 Lead PDIP (0.600")



24 Lead SOIC (Jedec, 0.300")

PIN DESCRIPTION

| Pin # | Symbol | Type | Signal | Description |
|-------|-----------------|------|--------|---|
| 1 | V _{EE} | - | - | -5 V (+/-0.25 V). |
| 2 | V _{CC} | - | - | +5 V (+/-0.25 V). |
| 3 | GND | - | - | Ground. |
| 4 | TI1 | | TTL | Transmitter 1 input. |
| 5 | TI2 | | TTL | Transmitter 2 input. |
| 6 | TI3 | | TTL | Transmitter 3 input. |
| 7 | SEL1 | | TTL | Mode select 1. (see <i>Table 1</i> for details) |
| 8 | SEL2 | | TTL | Mode select 2. (see <i>Table 1</i> for details) |
| 9 | RO3 | O | TTL | Receiver 3 output. |
| 10 | RO2 | O | TTL | Receiver 2 output. |
| 11 | RO1 | O | TTL | Receiver 1 output. |
| 12 | SEL0 | | TTL | Mode select 0. (see <i>Table 1</i> for details) |
| 13 | RI1- | | V.35 | Receiver 1 negative input. |
| 14 | RI1+ | | V.35 | Receiver 1 positive input. |
| 15 | RI2- | | V.35 | Receiver 2 negative input. |
| 16 | RI2+ | | V.35 | Receiver 2 positive input. |
| 17 | RI3- | | V.35 | Receiver 3 negative input. |
| 18 | RI3+ | | V.35 | Receiver 3 positive input. |
| 19 | TO3- | O | V.35 | Transmitter 3 negative output. |
| 20 | TO3+ | O | V.35 | Transmitter 3 positive output. |
| 21 | TO2- | O | V.35 | Transmitter 2 negative output. |
| 22 | TO2+ | O | V.35 | Transmitter 2 positive output. |
| 23 | TO1- | O | V.35 | Transmitter 1 negative output. |
| 24 | TO1+ | O | V.35 | Transmitter 1 positive output. |

DC ELECTRICAL CHARACTERISTICS

Test Conditions: $V_{CC} = +5.0V \pm 5\%$, $V_{EE} = -5.0V \pm 5\%$, $T_A = 25^\circ C^1$, driver and receiver are enabled unless otherwise specified. (See Figure 2)

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Conditions |
|------------|---|--------------|-----------|----------------------------|------------|--|
| $ V_{OD} $ | Transmitter Differential Output Voltage | 0.44 | 0.55 | 0.66 | V | $-4V \leq V_{OS} \leq +4V$ |
| V_{OC} | Transmitter Common-Mode Output Voltage | -0.3 | 0 | +0.3 | V | $V_{OS} = 0V$ |
| I_{OH} | Transmitter Output High Current | -12.6 | -11 | -9.4 | mA | |
| I_{OL} | Transmitter Output Low Current | 9.4 | 11 | 12.6 | mA | |
| I_{OZ} | Transmitter Output Leakage Current | | ± 1 | ± 100 | μA | $V_{TO}^+ = \pm 5V$ $V_{TO}^- = \pm 5V$ While driver disabled |
| R_O | Transmitter Output Impedance | | 50 | | K Ω | |
| V_{TH} | Differential Receiver Input Threshold Voltage | | | 150 | mV | $f = 10$ Mbps |
| V_{HYST} | Receiver Input Hysteresis | | 30 | | mV | $V_{OS} = 0V$ |
| I_{IN} | Receiver Input Current | | | +0.4 | mA | $-5V \leq V_{RI}^+, V_{RI}^- \leq 5V$ |
| R_{IN} | Receiver Input Impedance Differential | | 35 | | K Ω | $-5V \leq V_{RI}^+, V_{RI}^- \leq 5V$ |
| V_{OH} | Receiver Output High Voltage | 3 | 4.5 | | V | $I_{OH} = -4mA$ |
| V_{OL} | Receiver Output Low Voltage | | 0.4 | 0.8 | V | $I_{OL} = 4mA$ |
| I_{OSC} | Receiver Output Short-Circuit Current | | 13 | | mA | $0 \leq V_O \leq V_{CC}$ |
| I_{OZR} | Receiver Three-State Output Current | | | ± 10 | μA | Receiver Disabled $0 \leq V_O \leq V_{CC}$ |
| V_{IH} | Logic Input High Voltage | 2 | | | V | T_{In} , SEL2-0 |
| V_{IL} | Logic Input Low Voltage | | | 0.8 | V | T_{In} , SEL2-0 |
| I_{IN} | Logic Input Current | | ± 2.5 | ± 10 | μA | T_{In} , SEL2-0 |
| I_{CC} | V_{CC} Supply Current | | 36 | 50 | mA | All On, Loaded, $F = 10Mbps$ |
| | | | 250 | | μA | All Off |
| I_{EE} | V_{EE} Supply Current | | -38 | -50 | mA | All On |
| | | | -180 | | μA | All Off |

Notes

¹ All currents flowing into the device pins are marked positive. All current flowing out of the device pins are marked negative. **Bold face parameters** are covered by production test and guaranteed over operating temperature range.

Specifications are subject to change without notice

AC ELECTRICAL CHARACTERISTICS

Test Conditions: $V_{CC} = +5.0\text{V} \pm 5\%$, $V_{EE} = -5.0\text{V} \pm 5\%$, $T_A = 25^\circ\text{C}^1$, driver and receiver are enabled unless otherwise specified.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Conditions |
|-------------|--|------|------|-----------|------|--------------------|
| T_R, T_F | Transmitter Rise or Fall Time | | 5 | 30 | ns | $V_{OS}=0\text{V}$ |
| T_{TPLH} | Transmitter Input to Output Propagation Delay | | 25 | 40 | ns | $V_{OS}=0\text{V}$ |
| T_{TPHL} | Transmitter Input to Output Propagation Delay | | 27 | 40 | ns | $V_{OS}=0\text{V}$ |
| T_{OSKEW} | Transmitter Output to Output Skew | | 3 | | ns | $V_{OS}=0\text{V}$ |
| T_{RPLH} | Receiver Input to Output Propagation Delay (rising) | | 37 | 50 | ns | $V_{OS}=0\text{V}$ |
| T_{RPHL} | Receiver Input to Output Propagation Delay (falling) | | 35 | 50 | ns | $V_{OS}=0\text{V}$ |
| T_{ISKEW} | Differential Receiver Skew ($T_{RPLH} - T_{RPHL}$) | | 2 | | ns | $V_{OS}=0\text{V}$ |
| T_{ZL} | Receiver Enable to Output Low | | 34 | | ns | |
| T_{ZH} | Receiver Enable to Output High | | 37 | | ns | |
| T_{LZ} | Receiver Disable to Output Low | | 55 | | ns | |
| T_{HZ} | Receiver Disable to Output High | | 57 | | ns | |

Notes

¹ All currents flowing into the device pins are marked positive. All current flowing out of the device pins are marked negative. **Bold face parameters** are covered by production test and guaranteed over operating temperature range.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Storage Temperature -65°C to $+150^\circ\text{C}$
 Operating Temperature -40°C to $+85^\circ\text{C}$
 Supply Voltage $\pm 7\text{V}$

| SEL2 | SEL1 | SEL0 | Drivers On | Receivers On | Description |
|------|------|------|------------|--------------|---------------------------------|
| 0 | 0 | 0 | - | 1, 2, 3 | All receivers on |
| 0 | 0 | 1 | - | - | All off |
| 0 | 1 | 0 | 1, 2, 3 | 1, 2 | DCE mode |
| 0 | 1 | 1 | 1, 2, 3 | 1, 2 | DCE mode with mirrored loopback |
| 1 | 0 | 0 | 1, 2 | 1, 2, 3 | DTE mode |
| 1 | 0 | 1 | 1, 2 | 1, 2, 3 | DTE mode with mirrored loopback |
| 1 | 1 | 0 | 1, 2, 3 | 1, 2, 3 | All on |
| 1 | 1 | 1 | 1, 2, 3 | - | All drivers on |

Note: The driver and receiver outputs which are not on, are placed in Hi-Z state.

Table 1. Function Table

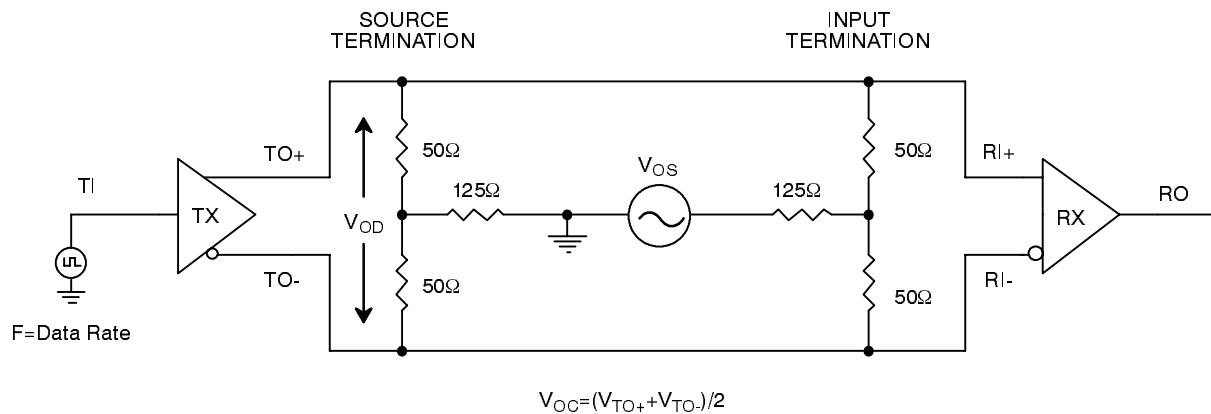


Figure 2. XR-T3591A Test Circuit

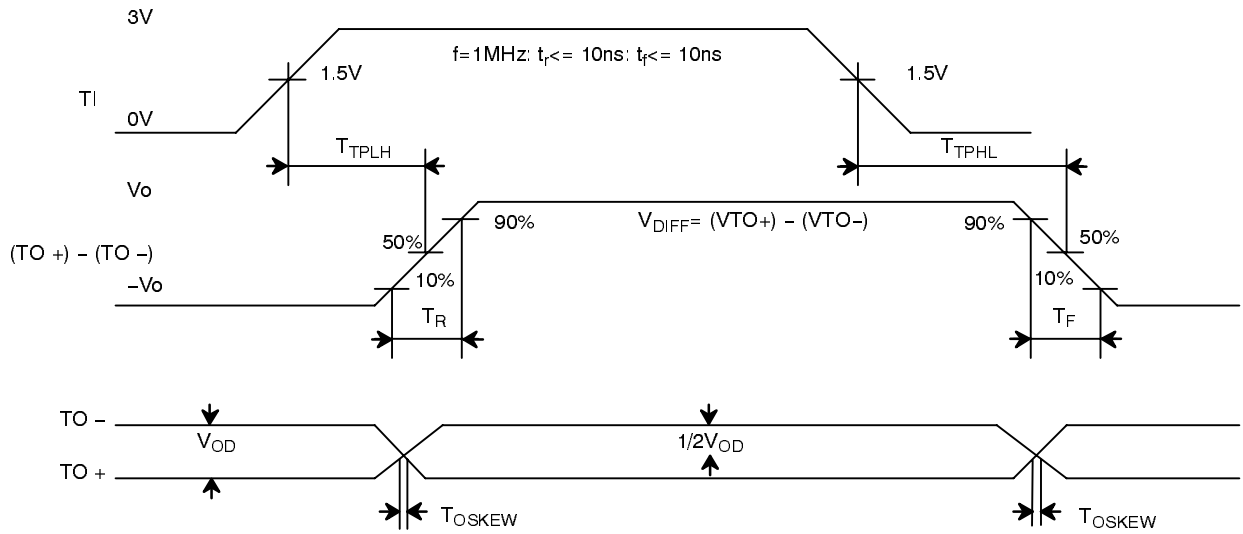


Figure 3. V.35 Transmitter Propagation Delays

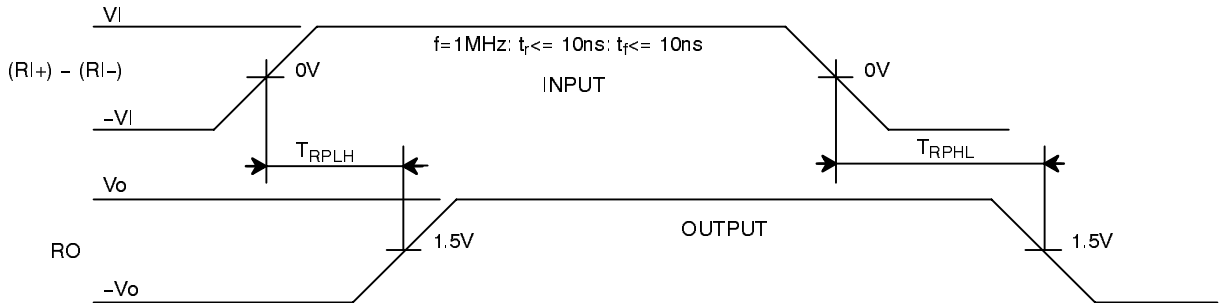


Figure 4. V.35 Receiver Propagation Delays

Cable Termination

For proper operation, the differential inputs and outputs of the XR-T3591 must be properly terminated. This is a requirement to assure full adherence to V.35 electrical signal specifications. The following diagram is a proposed termination configuration:

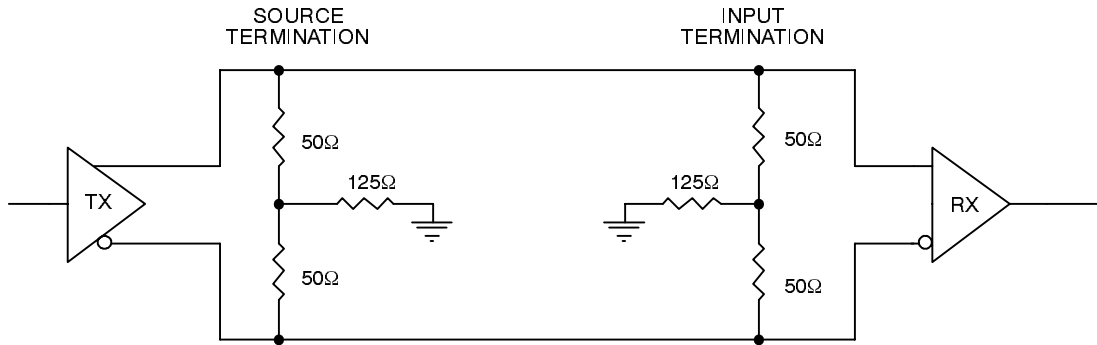


Figure 5. Proposed Source And Input Terminations

Note: In order to implement the terminations proposed above, standard 1/8 W surface mount or through hole 5% resistors can be used. Furthermore, appropriate resistor networks can be used as well.

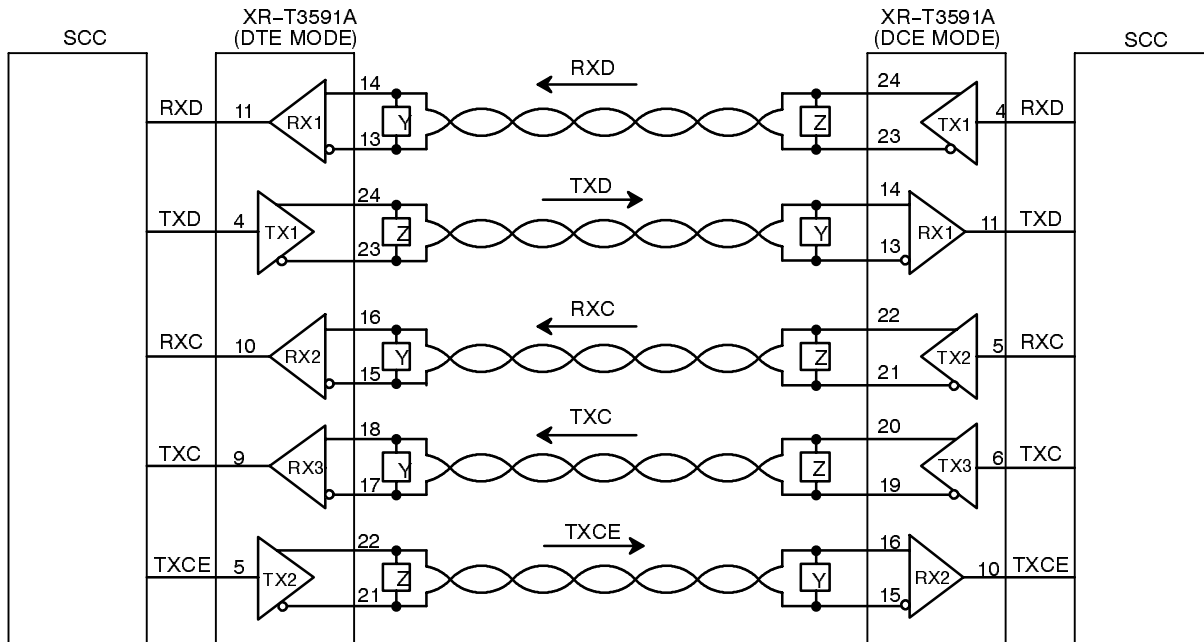


Figure 6. Typical V.35 Clock And Data Configuration

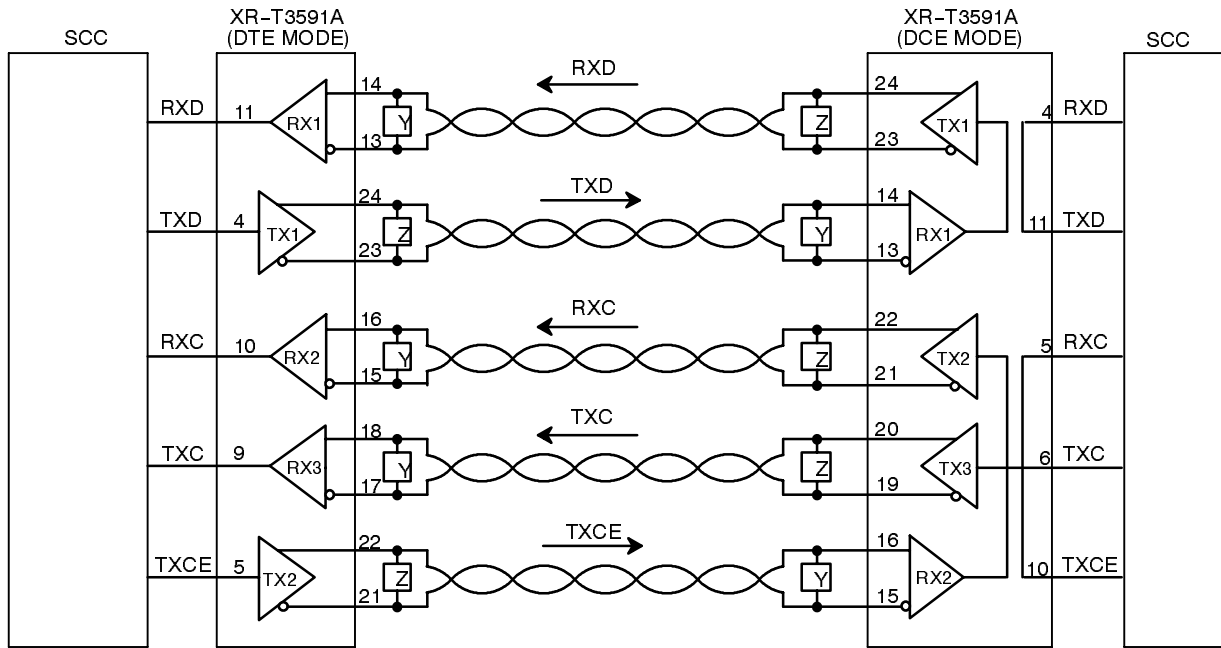


Figure 7. Typical V.35 Configuration During DCE Mirrored Loopback

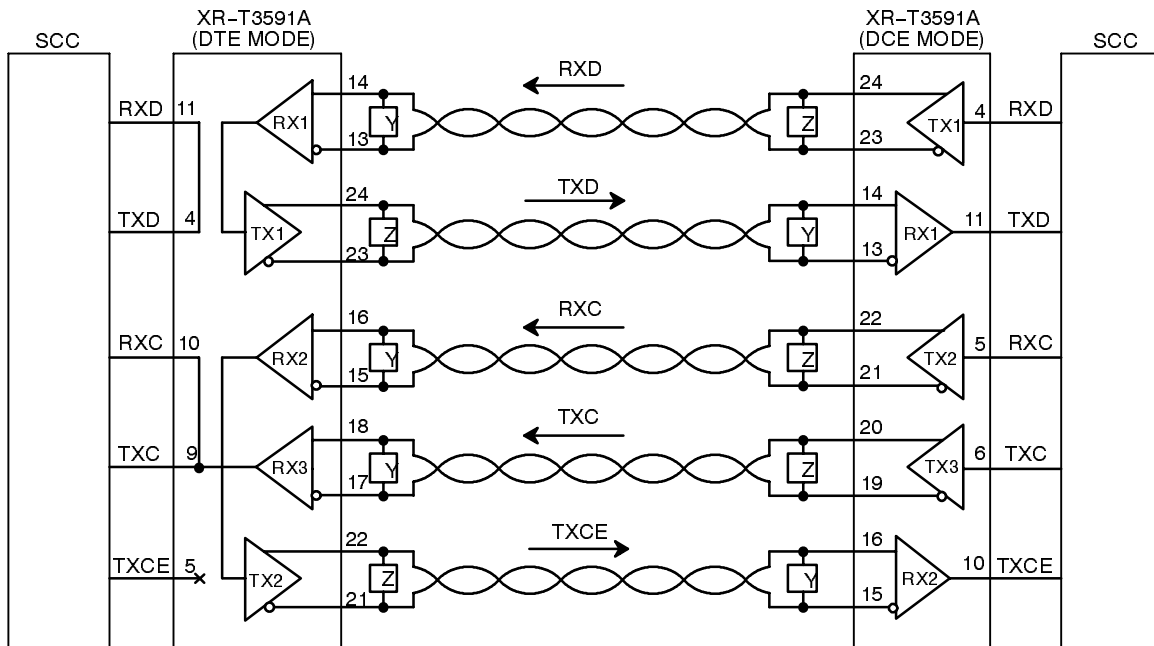


Figure 8. Typical V.35 Configuration During DTE Mirrored Loopback

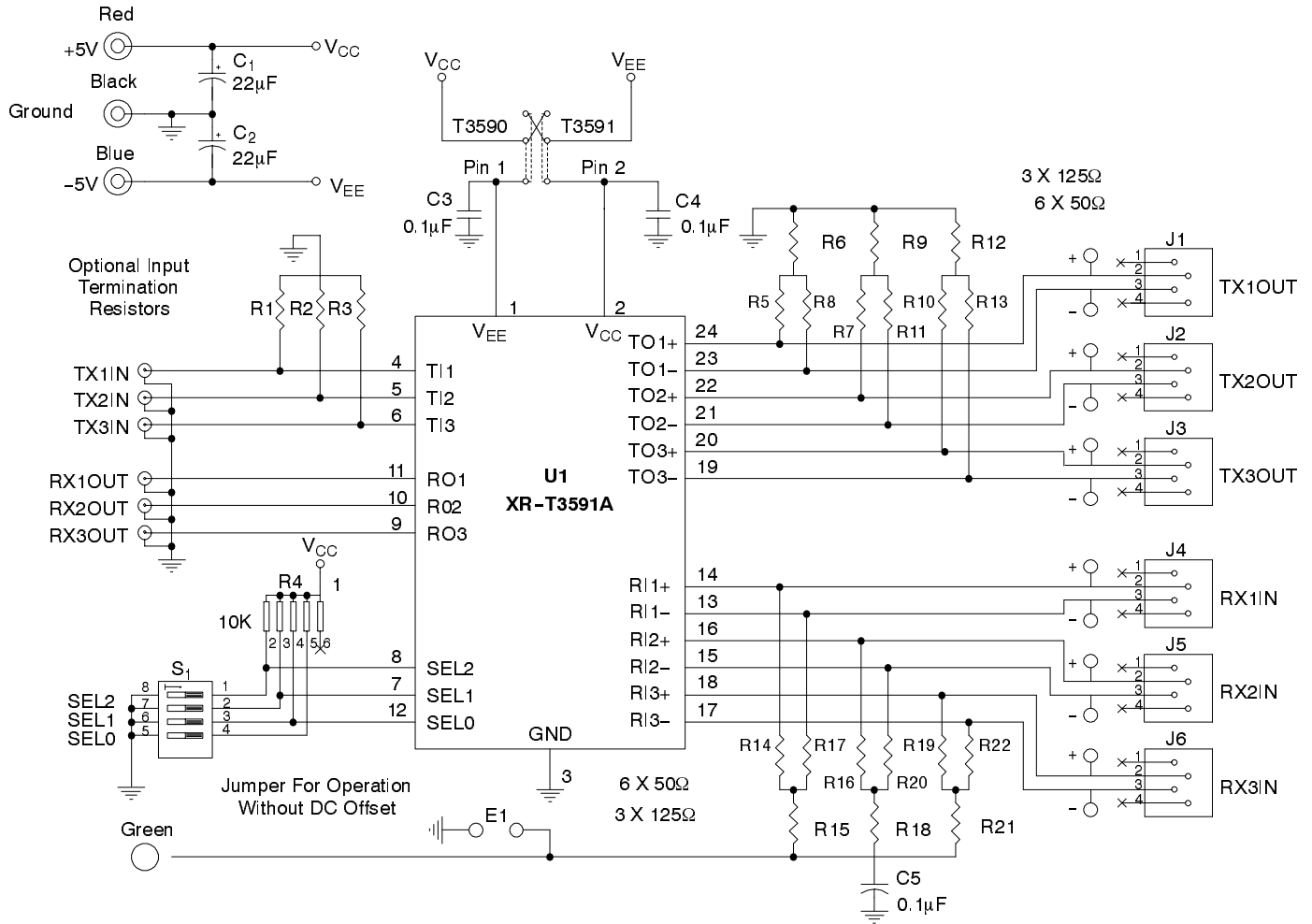
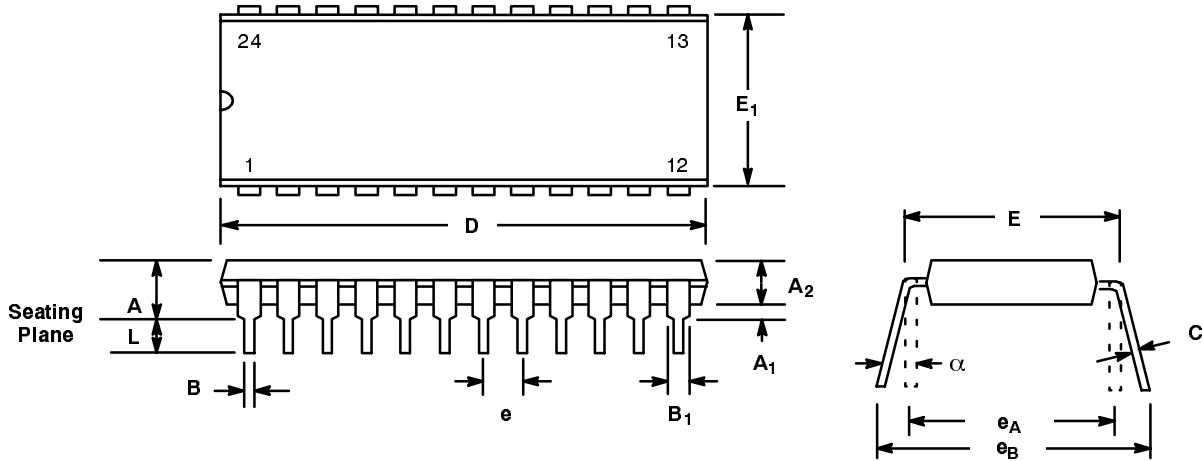


Figure 9. XR-T3591A Demo Board

**24 LEAD PLASTIC DUAL-IN-LINE
(600 MIL PDIP)**

Rev. 1.00

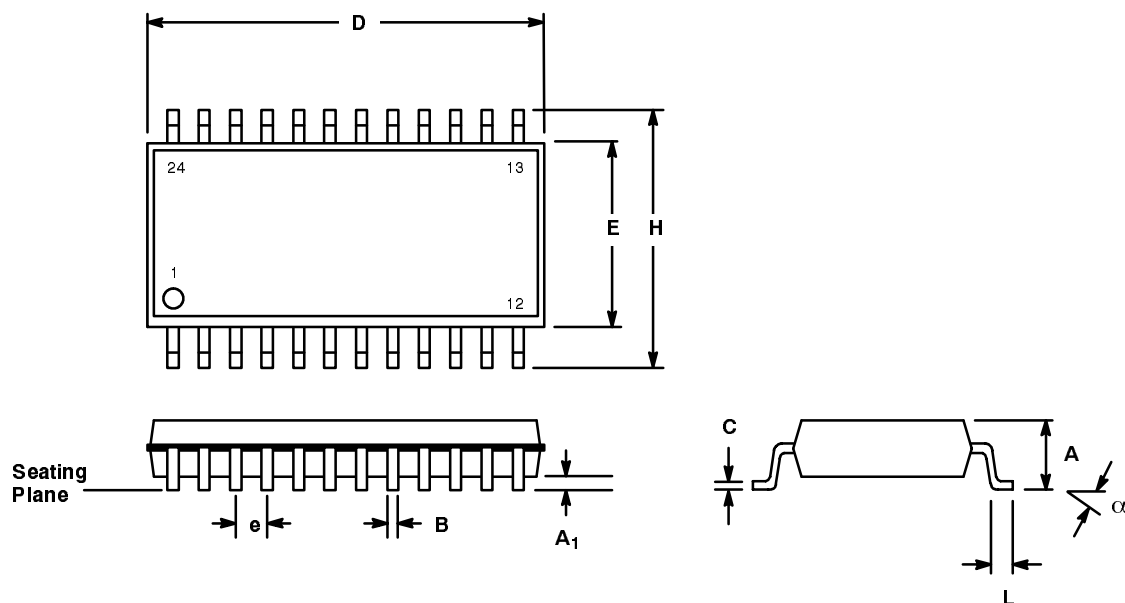


| SYMBOL | INCHES | | MILLIMETERS | |
|----------------|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.160 | 0.250 | 4.06 | 6.35 |
| A ₁ | 0.015 | 0.070 | 0.38 | 1.78 |
| A ₂ | 0.125 | 0.195 | 3.18 | 4.95 |
| B | 0.014 | 0.024 | 0.36 | 0.56 |
| B ₁ | 0.030 | 0.070 | 0.76 | 1.78 |
| C | 0.008 | 0.014 | 0.20 | 0.38 |
| D | 1.150 | 1.290 | 29.21 | 32.77 |
| E | 0.600 | 0.625 | 15.24 | 15.88 |
| E ₁ | 0.485 | 0.580 | 12.32 | 14.73 |
| e | 0.100 BSC | | 2.54 BSC | |
| e _A | 0.600 BSC | | 15.24 BSC | |
| e _B | 0.600 | 0.700 | 15.24 | 17.78 |
| L | 0.115 | 0.200 | 2.92 | 5.08 |
| α | 0° | 15° | 0° | 15° |

Note: The control dimension is the inch column

24 LEAD SMALL OUTLINE (300 MIL JEDEC SOIC)

Rev. 1.00



| SYMBOL | INCHES | | MILLIMETERS | |
|----------|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.093 | 0.104 | 2.35 | 2.65 |
| A1 | 0.004 | 0.012 | 0.10 | 0.30 |
| B | 0.013 | 0.020 | 0.33 | 0.51 |
| C | 0.009 | 0.013 | 0.23 | 0.32 |
| D | 0.598 | 0.614 | 15.20 | 15.60 |
| E | 0.291 | 0.299 | 7.40 | 7.60 |
| e | 0.050 BSC | | 1.27 BSC | |
| H | 0.394 | 0.419 | 10.00 | 10.65 |
| L | 0.016 | 0.050 | 0.40 | 1.27 |
| α | 0° | 8° | 0° | 8° |

Note: The control dimension is the millimeter column

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