PLL FREQUENCY SYNTHESIZER AND CONTROLLER
FOR FM/MW/LW TUNER

The μPD1703C-015 is a single chip CMOS LSI designed for a Phase Locked Loop (PLL) Frequency synthesizer digital tuning system controller of FM/MW/LW European band.

The μPD1703C-015 provides a high performance varactor-tuned FM/MW/LW tuner accompanied with the prescaler μPB553AC.

The μPD1703C-015 is packed in a 28-pin slim dual in-line package (DIP).

FEATURES

- Fluorescent Indicator Panel (FIP) segments direct drive output
- Incorporated PLL frequency synthesizer, swallow-counter, and controller
- Easy back-up preset memories (less than 10 μA)
- Display a preset station by LED lamp
- High FM reference frequency 25 kHz (By employing pulse swallowing method)
- Alterable frequency bands: either FM/MW/LW or FM/MW by initial set switch
- 14 preset station memories by 7 preset memories switches; (FM/MW; 7 stations/7 stations, or FM/MW/LW; 7 stations/4 stations/3 stations)
- Accepts to use either 'momentary switch' or 'alternate switch' for preset key and 'frequency band selecting key'
- One last station memory each for FM/MW/LW capability
- Up/Down searching by both way; AUTO and MANUAL
- IF OFF-set capability (10.650, 10.675, 10.700, and 10.725 MHz)
- Two way display; multipler or static selectable by initial-set switch.
- Channel number display capability (−2 CH through 70 CH, FM band only)
- 'EXTERNAL DATA PRESET' function, usefull for tracking-point adjustment on massproduction
- 4 1/2-digit display for tuned frequency
- 28-pin slim dual in-line package (DIP)
- Single power supply; 5 V ±10 %

FUNCTION

Receiving frequency, channel spacing, reference frequency, intermidiate frequency

BAND	FREQUENCY RANGE	CHANNEL SPACING	REFERENCE FREQUENCY	INTERMIDIATE FREQUENCY
FM	87.50 to 108.00 MHz	50 kHz	25 kHz	10.650, 10.675, 10.700, 10.725 MHz
MW	522 to 1 611 kHz	9 kHz	9 kHz	450 kHz
LW	155 to 353 kHz	9 kHz	1 kHz	450 kHz

Station selection modes;

(1) AUTO UP/DOWN TUNING ('triangle wave form' tuning)

During the SD, station detector, terminal receives high level input signal, searching operation stops and continues to receive the detected station. If the top or bottom of the band is reached, the searching operation will reverse direction — from upwards to downwards, or reversely.

(2) MANUAL UP/DOWN TUNING ('triangle wave form' tuning)

The 'Down' (tune down) and the 'UP' (tune up) keys are dual function keys.

A) A single momentary depression will tune to next station.

B) Continuous depression over 0.5 seconds allows traversing down or up the entire band until these keys are released.
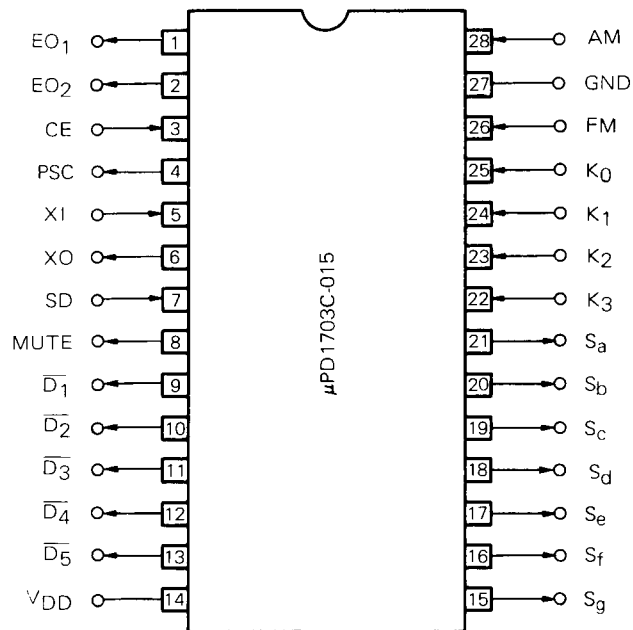
If the top or bottom of the band is reached, the Manual searching operation will stop.

(3) RECALL PRESET MEMORY

A) When 'WITH LW' key is released, seven preset stations (M1 to M7) can be recalled from the memory for each FM and MW band.

B) When 'WITH LW' key is depressed, seven preset stations (M1 to M7) can be recalled from the memory of FM band, four stations (M1 to M4) from MW band, and three stations (M5 to M7) from LW band.

PIN CONFIGURATION (Top View)

Left pin	#		#	Right pin
EO_1	1		28	AM
EO_2	2		27	GND
CE	3		26	FM
PSC	4		25	K_0
XI	5		24	K_1
XO	6		23	K_2
SD	7		22	K_3
MUTE	8		21	S_a
$\overline{D_1}$	9		20	S_b
$\overline{D_2}$	10		19	S_c
$\overline{D_3}$	11		18	S_d
$\overline{D_4}$	12		17	S_e
$\overline{D_5}$	13		16	S_f
V_{DD}	14		15	S_g

μPD1703C-015

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PIN DESCRIPTION

PIN NO.	PIN SYMBOL	PIN NAME	DESCRIPTION
1 2	EO$_1$ EO$_2$	Error out	These pins provide charge-pump output from phase-detector of PLL. When the divided oscillation frequency is higher than reference frequency, these pins output high level, when lower, output low level. When these two frequency are same, outputs float. These pins accept to be connected with any LPF, Low pass filter, of MW, LW, or FM, because outputs of EO$_1$ and EO$_2$ are coincident.
3	CE	Chip enable	This pin is a input terminal of selection of this device operation. The high level input allows device operation. When low level is input, display is extinguished the operation of PLL is stopped, the internal clock generation is also stopped, but the contents of memories are held. The stored preset stations information is held by low level of this pin with low consumption current less than 10 μA. When high level is applied to this pin, it is required to make high after V$_{DD}$ rises over 4.5 V. When low level is applied, it is required to make low before V$_{DD}$ comes down to 4.5 V. The less than 134 μs of high or low level applying speed never accepted.
4	PSC	Prescaler control	This output provides a signal for selecting the divise of prescaler when the frequency is divided down by 'Pulse swallowing method. This output can be directly connected to 'PSC' pin of the prescaler μPB553AC. The divisers of μPB553AC are 16 and 17.
5 6	XI XO	X'tal	These inputs are for connection to a 4.5 MHz crystal.
7	SD	Station detector	This input is used to control the station searching operation. It is high to indicate the presence of a station. The high level received within 75 ms after PLL is locked brings to stop of automatic searching operation.
8	MUTE	Mute output	This output line goes high to mute the shock noise in the case of PLL lock. If the CE terminal becomes low level, this pin goes low automatically. The mute durations in each mode are as follows: ○ Band change ....800 ms approx. ○ Manual searching ....200 ms approx. each tune ○ Automatic searching......200 ms approx. after SD pin receives high level signal ○ Recall preset memory ...450 ms approx. These mute durations are output time after data of PLL is changed, and in fact, joined mute leading time (before data of PLL is changed): 50 ms approx. (See 4.2 Mute timing charts)

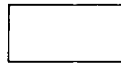| PIN NO.	PIN SYMBOL	PIN NAME	DESCRIPTION
9 to 13	$\overline{D_1}$ to $\overline{D_5}$	Digit outputs	These outputs are digit drivers. (Active-low) (See 2. Display)
14	V_{DD}	Power supply	5 V ±10 % Volt supply to the chip. If the device operation is not needed except holding the memorised station information, the decrease down 3.0 V is allowed. The rising time of V_{DD} voltage is required to be within 500 ms, if the time takes too long, the operation of initialization may be insufficient.
15 to 21	S_a to S_g	Segment outputs	These outputs are segment drivers. They are also used as horizontal driver for the keyboard matrix. An output, 30 V, is high for a segment of FIP to be on. (See 1.1 Configuration of key matrix and 2. Display.)
22 to 25	K_0 to K_3	Key return signal inputs	These are Key return signal inputs from Key matrix. (See 1.1 Configuration of Key matrix.)
26	FM	FM local oscillator signal inputs	This input is the FM band local oscillator input. The frequency is devided down by 16 or 17, using the prescaler μPB553AC. The DC of input signal must be cut by a capacitor because the AC amplifier is provided internally.
27	GND	Ground	System grounds
28	AM	AM local oscillator signal inputs	This input is the MW, LW band local oscillator input. The DC of input signal must be cut by a capacitor because the AC amplifier is provided internally.

CONTENTS

1. KEY MATRIX

1.1 CONFIGURATION OF KEY MATRIX

Input / Output	K) (25)	K₁ (24)	K₂ (23)	K₃ (22)
Sₐ (21)	DOWN	UP	MEMORY	EXT. DATA PRESET
Sᵦ (20)	M4	M3	M2	M1
S_c (19)		M7	M6	M5
S_d (18)		LW	FM	WN
S_e (17)				
S_f (16)	WITH LW	STATIC/DYNA	AUTO/MANUAL	CH/FREQ
S_g (15)			IF1	IF0

Numbers in parentheses are pin No.

☐	: Momentary switch
▨ (boxed hatched)	: Momentary or alternate switch
▨ (hatched)	: Alternate switch
▢ (dotted)	: Diode matrix

1.2 KEY MATRIX CONNECTION

Key Input

Segment Output

or

or

Open
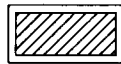
⊕ Momentary switch

⊡ Momentary or alternate switch

▢ Alternate switch

△ Diode matrix (Short or open)
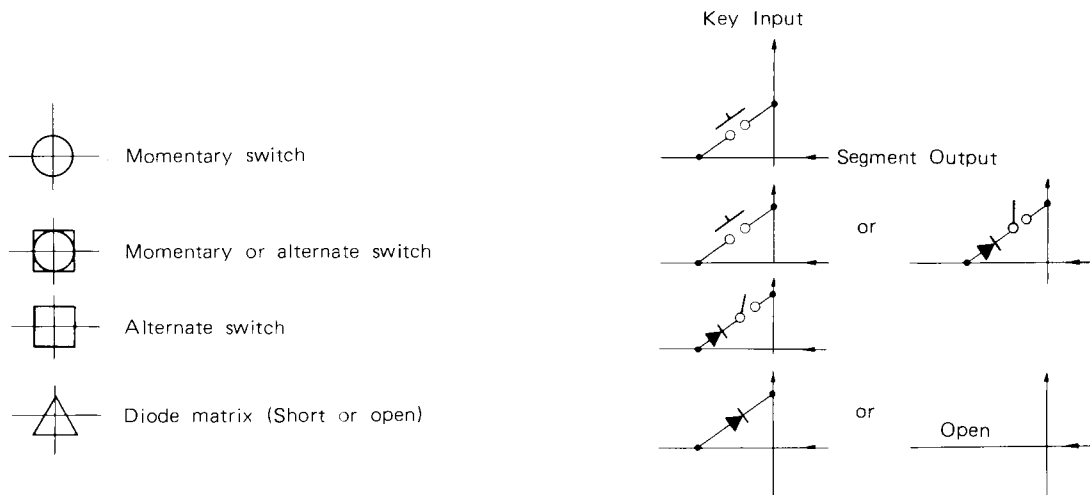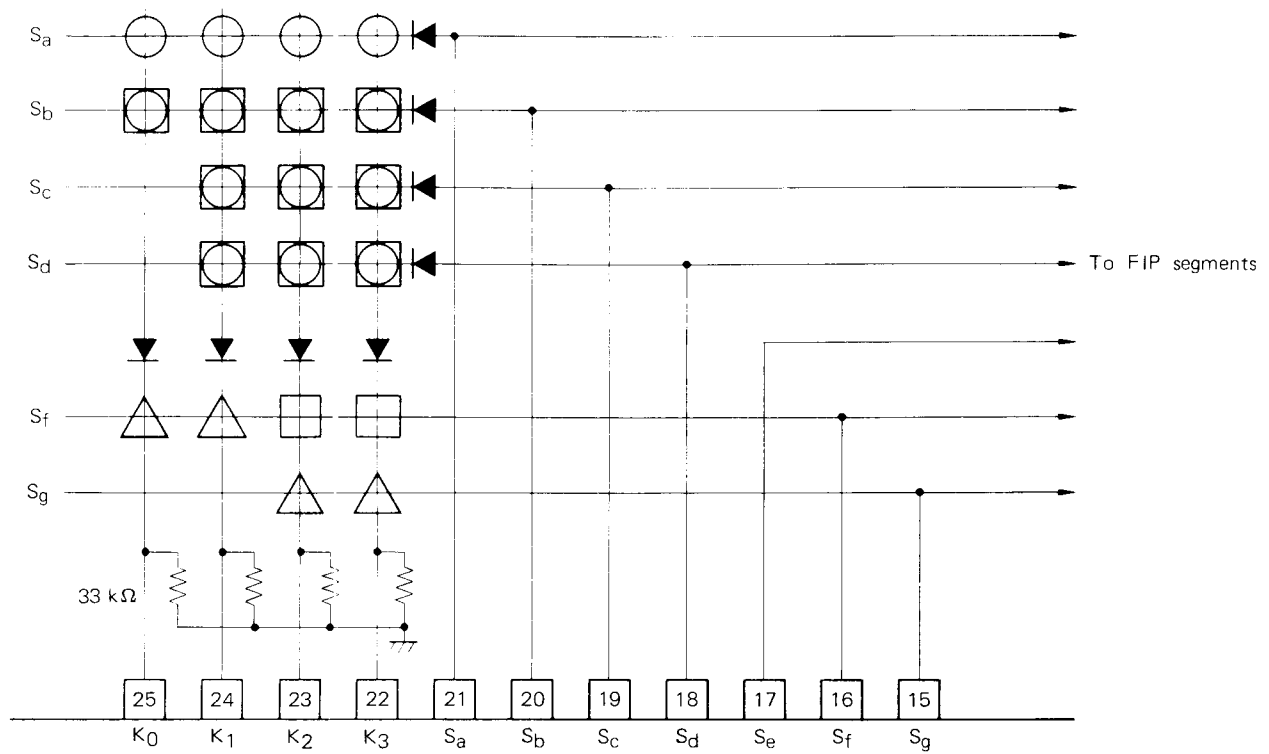
Although the PRESET KEY (M1 to M7) and BAND-SWITCH KEY (FM , MW , LW) allow to use momentary or alternate type switch, the diodes for preventing the leak-in of key return signal should be connected as follows according to the switch type addopted.

Example—1. Momentary switches are used for PRESET and BAND SWITCH KEY
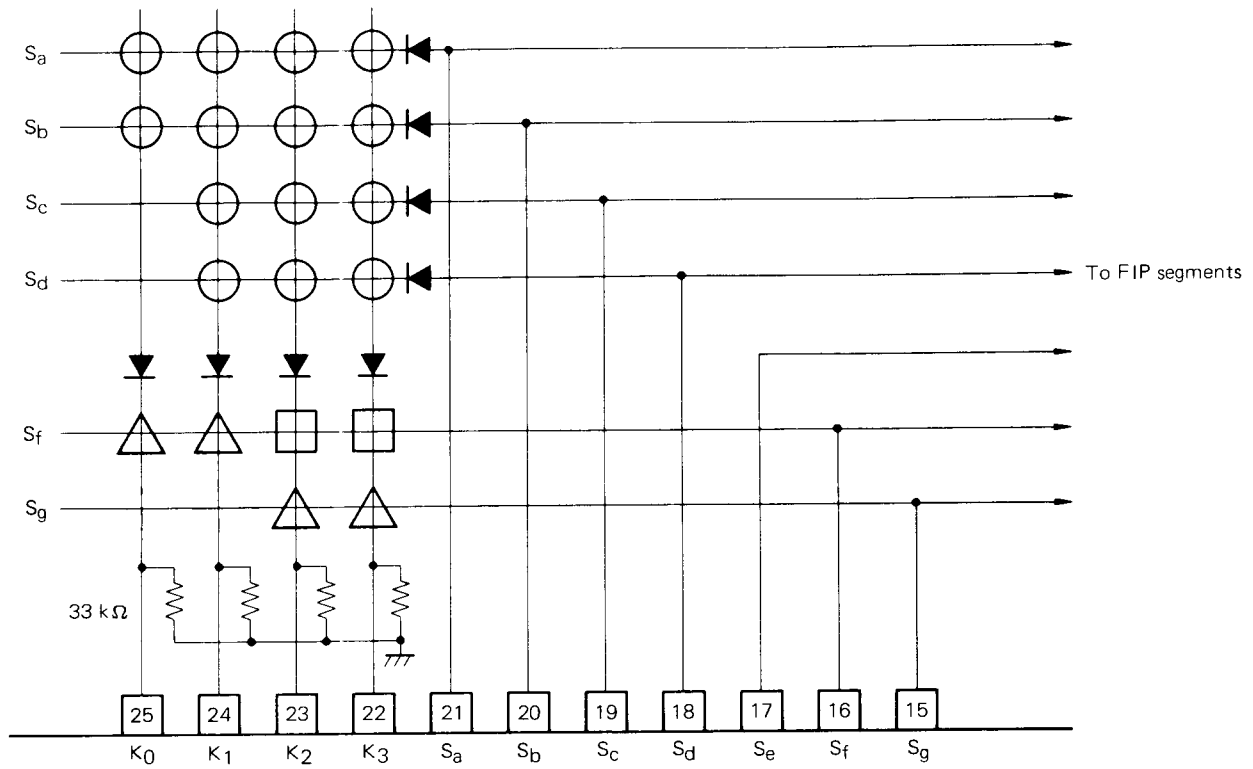
Example—2. Momentary switch is used for PRESET KEY, alternate switch for BAND SWITCH KEY

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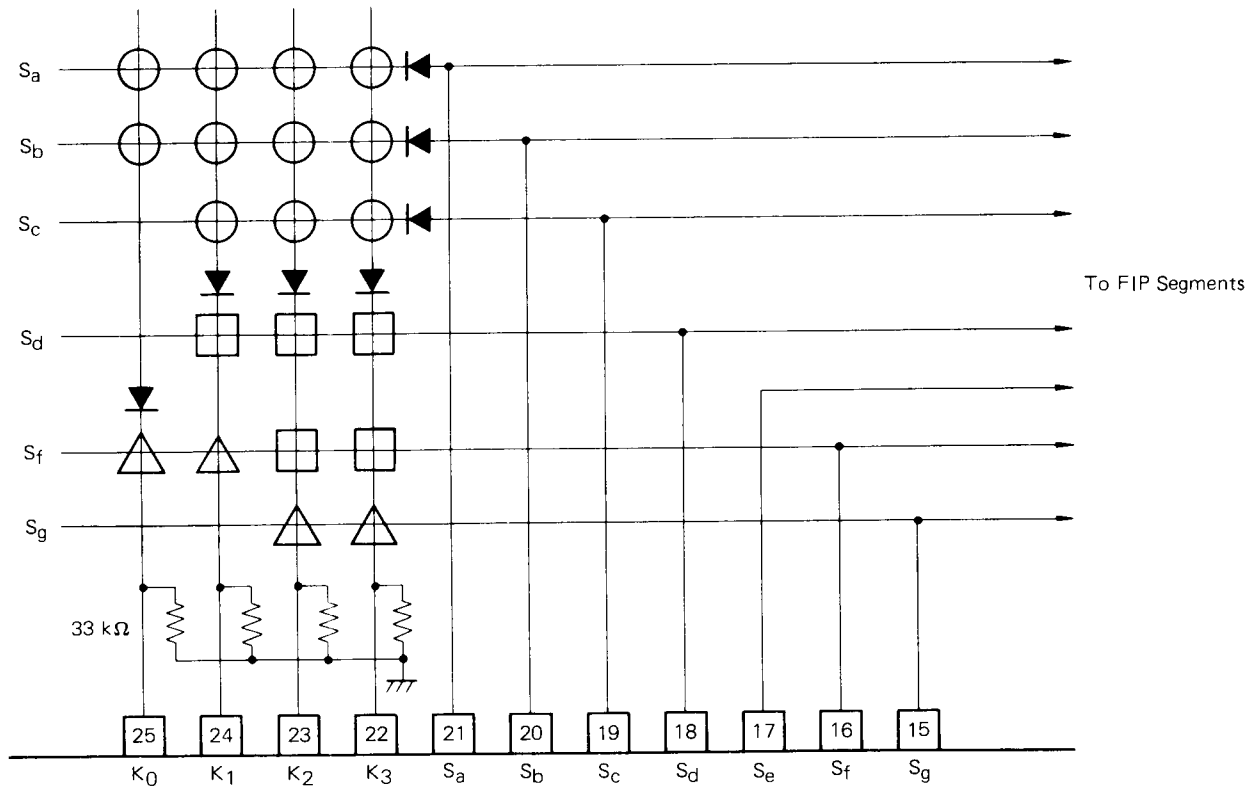
Example—3. Alternate switches are used for PRESET and BAND SWITCH KEY

To FIP segments

33 kΩ

25	24	23	22	21	20	19	18	17	16	15
K_0	K_1	K_2	K_3	S_a	S_b	S_c	S_d	S_e	S_f	S_g

S_a
S_b
S_c
S_d
S_f
S_g

1.3 DESCRIPTION OF KEY MATRIX

INITIAL SETTING DIODE MATRIX

There are three kinds of diode matrix for initial setting.

These conditions are read into controller IC when the power initially applied to V_{DD} terminal or when the level of CE terminal is changed from low to high.

(1) The switch for setting IF OFF-set frequency of FM.
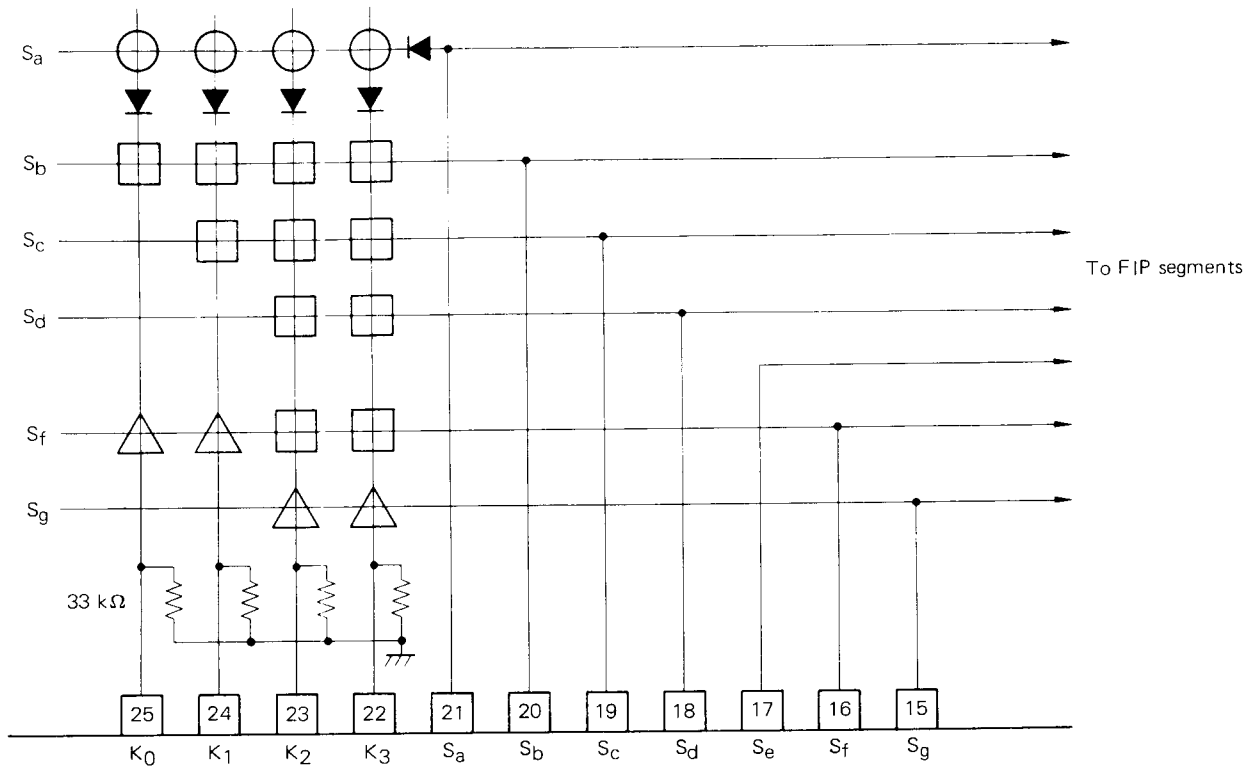
IF1, IF0

(2) The switch for receiving LW band.

WITH LW

(3) The switch for selecting static or dynamic drive display.

STATIC/DYNA

These setting are to put diode across the points matrix intersection, or open (The meaning of "1" is short and "0" is open in the following description.)

SYMBOL	DESCRIPTION
IF1 IF0	The four intermediate frequencies can be selected. | IF1	IF0	IF
---	---	---
0	0	10.700 MHz
0	1	10.725
1	0	10.650
1	1	10.675	
WITH LW	By setting this switch preset memories are divided into as follows. OFF (0) : FM (M1 to M7), MW (M1 to M7) ON (1) : FM (M1 to M7), MW (M1 to M4), LW (M5 to M7)
STATIC/DYNA	OFF (0) : multiplex drive display ON (1) : static drive display In the case of static drive display, DATA signal is output from SEGMENT S_C terminal, clock signal from DIGIT $\overline{D_1}$, and LOAD signal from $\overline{D_2}$ terminal. (See 2. Display)

ALTERNATE SWITCH

There are two kinds of alternate switch:

SYMBOL	DESCRIPTION
CH/FREQ	Selecting switch for frequency or channel display of the FM band. OFF (0 : to display the FM frequency ON (1 : to display the FM channel The following is corresponding table of frequency and channel. For example, "88.00 MHz" is display "+3 CH" by switching this switch. <table><tr><th>Frequency</th><th>Channel</th><th>Frequency</th><th>Channel</th></tr><tr><td>87.50 MHz</td><td>−2 CH</td><td>96.05 MHz</td><td>+30 CH</td></tr><tr><td>87.55</td><td>−2</td><td>96.10</td><td>+30</td></tr><tr><td>87.60</td><td>2</td><td>96.15</td><td>+30</td></tr><tr><td>87.65</td><td>+2</td><td>96.20</td><td>−40</td></tr><tr><td>87.70</td><td>+2</td><td>96.25</td><td>−40</td></tr><tr><td>87.75</td><td>+2</td><td></td><td></td></tr><tr><td>87.80</td><td>−3</td><td>107.45</td><td>+68</td></tr><tr><td>87.85</td><td>−3</td><td>107.50</td><td>+68</td></tr><tr><td>87.90</td><td>3</td><td>107.55</td><td>+68</td></tr><tr><td>87.95</td><td>+3</td><td>107.60</td><td>−69</td></tr><tr><td>88.00</td><td>+3</td><td>107.65</td><td>−69</td></tr><tr><td>88.05</td><td>+3</td><td>107.70</td><td>69</td></tr><tr><td>88.10</td><td>−4</td><td>107.75</td><td>+69</td></tr><tr><td>88.15</td><td>−4</td><td>107.80</td><td>+69</td></tr><tr><td>88.20</td><td>4</td><td>107.85</td><td>+69</td></tr><tr><td></td><td></td><td>107.90</td><td>−70</td></tr><tr><td>96.00</td><td>30</td><td>107.95</td><td>−70</td></tr><tr><td></td><td></td><td>108.00</td><td>70</td></tr></table>
AUTO/MANUAL	Selecting switch for auto tuning or manual tuning. OFF (0) : Manual tuning ON (1) : Auto tuning Each tuning operation starts by depressing UP/DOWN momentary switch after setting this switch. (See. momentary/alternate switch on page 12) Note 1: The searching operation continues even if this switch is changed into MANUAL mode during AUTO TUNING mode. If searching operation is required to stop at the same time changing from AUTO to MANUAL, high level signal should be always input to SD terminal during MANUAL mode. Note 2: In Auto tuning mode, the μPD1703C-015 increases or decreases frequency step by step confirming that the PLL system is completely locked, in order to scan the band as fast as possible. Therefore if the PLL system is malfunctioning and is not locked, the μPD1703C-015 halts the AUTO tuning operation and waites for the PLL to be locked. In this condition, all the keys are not accepted. To escape this condition, force CE terminal to low level then high level, and the frequency can be varied by manual tuning. In the recommended application, the CE terminal is to be connected to the main-power-supply of the set. So the end user can vary the frequency after operating the power-supply-switch, even if the above malfunction occurs.

MOMENTARY/ALTERNATE SWITCH

Either momentary or alternate switch can be used for PRESET KEY (| M1 | to | M7 |) and BAND SWITCH KEY (| FM | , | MW | , | LW |).

If alternate switch is used for PRESET KEY, it should be connected with operation of | UP | or | DOWN | key.

SYMBOL	DESCRIPTION
EXTERNAL DATA PRESET	This switch is provided for writing the FM, MW frequency data into the PRESET memory (M1 to M7) from external microprocessor. This is useful to check the function of varactor tuned tuner using this IC at the massproduction. The following five terminals are used for data transfer. K_0 to K_3 .... input terminal of frequency data (4 bit parallel input) SD .... input terminal for indicating of signal receipt. (See 6. EXTERNAL DATA PRESET)
MEMORY	This is used to write a new frequency into preset memory. If any one of the memory key,	M1	to	M7	, is depressed within 5 sec. after this key is depressed, the displayed frequency is written into the memory corresponding to depressed memory key. In order to cancell the state that memory is ready to be written, press the	UP	/	DOWN	key or change the band of FM, MW, or LW.
UP DOWN	These key for automatic or manual tuning. (1) If AUTO/MANUAL switch is set in 'AUTO': ○ The depression of up key will result in traversing up the complete band at the speed of 80 ms/step. If the top of the band is reached the searching operation will turn to traverse down. (Triangle-wave tuning) If the SD terminal receive high level signal during traversing the band, searching operation will be stopped. If the	DOWN	key is depressed during searching up, traversing turns downward. ○ The depression of	DOWN	key will result in completely reversed operation mentioned above. Note: If the UP key is depressed during the searching up operation, or the DOWN key during down operation, each searching operation will be continued. Continuous depression of UP, DOWN key will result in continuous searching even if the SD terminal receive the high level signal. (2) If AUTO/MANUAL switch is set in 'MANUAL': ○ Each one depression of	UP	or	DOWN	key will result in traversing one step (or channel spacing) up or down. ○ If the	UP	or	DOWN	key is continuously depressed over 0.5 sec., the band is traversed upward or downward at the speed of 80 ms/step until the key is released. * If the band edge is reached, searching operation will stop. Even if AUTO/MANUAL switch is set to MANUAL during auto tuning operation, auto tuning operation is not stopped. If SD terminal always is input high level signal when AUTO/MANUAL switch is MANUAL, auto tuning operation is stopped at the same time that MANUAL switching.

SYMBOL	DESCRIPTION
	These keys are provided to write/read preset memories.
	Each memory memorizes one station each of FM and MW band.
	(WITH LW key: OFF)
	If the WITH LW key is on, M1 through M4 memorizes FM and MW band, and M5 through M7 are of FM and LW.

WITH LW: ON

M1	M2	M3	M4	M5	M6	M7
FM	FM	FM	FM	FM	FM	FM
MW	MW	MW	MW	LW	LW	LW

WITH LW: OFF

M1	M2	M3	M4	M5	M6	M7
FM	FM	FM	FM	FM	FM	FM
MW	MW	MW	MW	MW	MW	MW

SYMBOL: M1 to M7

(1) WRITE IN:

If one of the memory keys from [M1] through [M7] is depressed within 5 sec. after depression of MEMORY key, new frequency is written in a memory corresponding depressed key.

If WITH LW key is set 'ON', M1 to M4 accept the station of FM and MW, M5 through M7 accept of FM and LW. In this case M1 through M4 and M5 through M7 can not accept LW band and MW band respectively.

(2) READ OUT:

If one of the memory keys from M1 through M7 is depressed, the content of the memory corresponding depressed key is read out.

If the WITH LW key is ON, no action occurs by the depression of one key from [M1] through [M4] at receiving of LW band or M5 through M7 at MW band.

By depressing these perset keys the mute signal of approximately 450 ms duration is output.

(See 4.2 MUTE TIMING CHART)

* The minimum frequency of FM is read out when V_{DD} is on for the first time. Preset memory is write in the minimum frequency of each bands (FM, MW, LW) at this time.

SYMBOL: FM, MW, LW

These are for selection of frequency band. Either of momentary or alternate type is acceptable for these switches. The mute signal of approximately 850 ms duration will be output when the band is changed.

2. DISPLAY

2.1 MULTIPLEX DRIVE DISPLAY

The following figure shows display format and connection with pins of μPD1703C-015 in case of multiplex drive display (STATIC/DYNA key is OFF).

The pins of D_1 through D_5 and S_a through S_g in the figure are corresponding the digit terminal($\overline{D}_1$ to $\overline{D}_5$) and segment (S_a to S_g) of μPD1703C-015, respectively.

The segment terminal of μPD1703C-015 has 30 V output voltage (Pch open drain output) to be directly connected with FIP. To drive the digits one buffer amplifier by P N P transistor is required for digit drive because the digit output of μPD1703C-015 is complementary and active low signal is output.
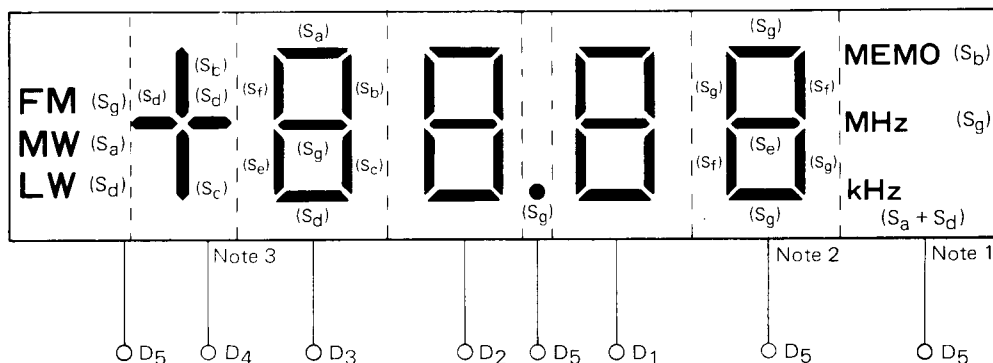
Fig. 1 Multiplex drive display connection diagram

Note 1: The indication of "kHz" is displayed by OR-signal of S_a and S_d. In case of without LW it can be displayed by S_a.

Note 2: This digit is provided for the tenth digit of FM 50 kHz. (only "$\square$" or "$\overline{}$") There is no display in MW and LW band.

Note 3: This digit is for display "$|$" (the upper or most left digit of frequency) or "$+$", "$--$" of FM channel.

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Followings are examples of display using the format of Fig. 1.

(1) Indication of FM frequency:

FM **89.45** MHz

(2) Indication of FM channel number:

FM -|- **37**

(3) Indication of MW frequency:

MW **1620** MEMO Note kHz

(4) Indication of LW frequency:

LW **200** kHz

Note: If the | MEMORY | key is depressed, (or new frequency is written in the memory) this 'MEMO' display is turn on during 5 sec. If one of preset station keys from | M1 | through | M7 | is depressed within 5 sec., the new frequency is written and then MEMO display is turn off.

2.2 STATIC DISPLAY

If the STATIC/DYNA key is set on, DATA signal is output from S_C segment terminal, CLOCK signal from digit $\overline{D_1}$, and LOAD signal from $\overline{D_2}$ terminal. The DATA signal is serially output by one bit at a time in the sequence shown below.

Output order	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
Display kind	--	LW	5	0	MEM	MW	FM	‖	BCD 100 kHz				BCD 1 MHz				BCD 10 MHz				BCD preset station display			
									0	1	2	4	0	1	2	4	0	1	2	4	0	1	2	4

The CLOCK signal corresponding to one bit of DATA signal makes the data shifted by one bit. If the BCD, binary coded decimal, data for preset station display completes to be shifted, LOAD signal is output and then the static converting has finished. The figure 2 shows the timing in this process.

The CLOCK and LOAD signal are shown as active high signal through inverter from $\overline{D_1}$, $\overline{D_2}$ terminal.
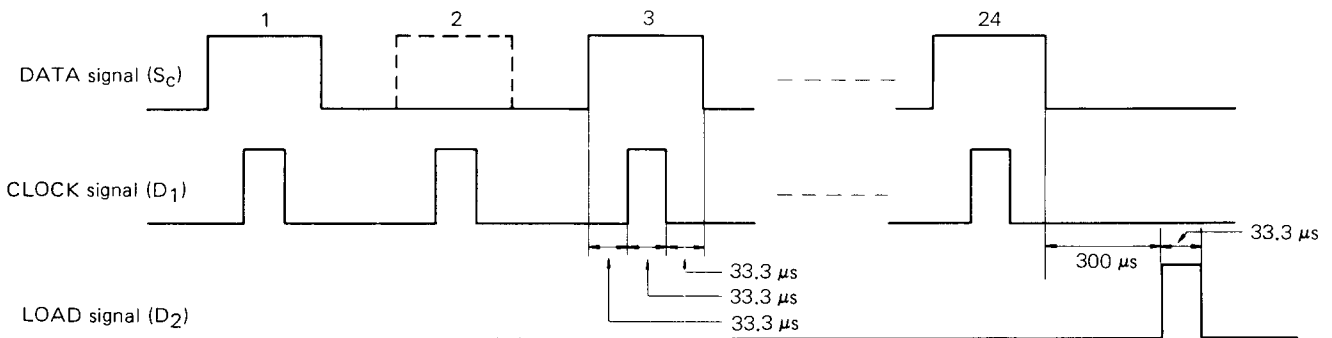
Fig. 2 Timing chart

These pulse sequence is output when the switch changing the contents of display is depressed, and after that it is output at 5 sec. intervals.

Followings are examples of static display.

In these examples high level output is shown in '1' and low level in '0'.

Ex. 1 FM 104.30 MHz

Output order	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
Display kind	--	LW	5	0	MEM	MW	FM	¦	BCD 100 kHz				BCD 1 MHz				BCD 10 MHz				BCD preset station display			
Output level	0	0	0	1	0	0	1	1	1	1	0	0	0	0	1	0	0	0	0	0	0	1	0	0

1　　3　　4　　0　　2(M2)

Ex. 2 FM +57 ch

Output order	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
Display kind	--	LW	5	0	MEM	MW	FM	¦	BCD 1 ch				BCD 10 ch				Blank				BCD preset station display			
Output level	0	1	0	0	0	0	0	0	0	0	1	0	0	1	1	0	1	0	0	0	1	1	1	0

+　　7　　5　　F (Blank)　　0 (last channel)

Ex. 3 LW 164 kHz

Output order	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
Display kind	--	LW	5	0	MEM	MW	FM	¦	BCD 1 kHz				BCD 10 kHz				BCD 100 kHz				BCD preset station display			
Output level	0	1	0	0	0	0	0	0	0	0	1	0	0	1	1	0	1	0	0	0	1	1	1	0

4　　6　　1　　7(M7)

Ex. 4 MW 810 kHz

Output order	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
Display kind	--	LW	5	0	MEM	MW	FM	¦	BCD 1kHz				BCD 10 kHz				BCD 100 kHz				BCD preset station display			
Output level	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	1	0	0

0　　1　　8　　3(M3)

3. PRESET STATION DISPLAY (Note)

BCD code is transmitted from S_e to S_g at timing of digit signal $\overline{D_4}$.

An example is shown in Fig. 3, and the timing chart in Fig. 4.
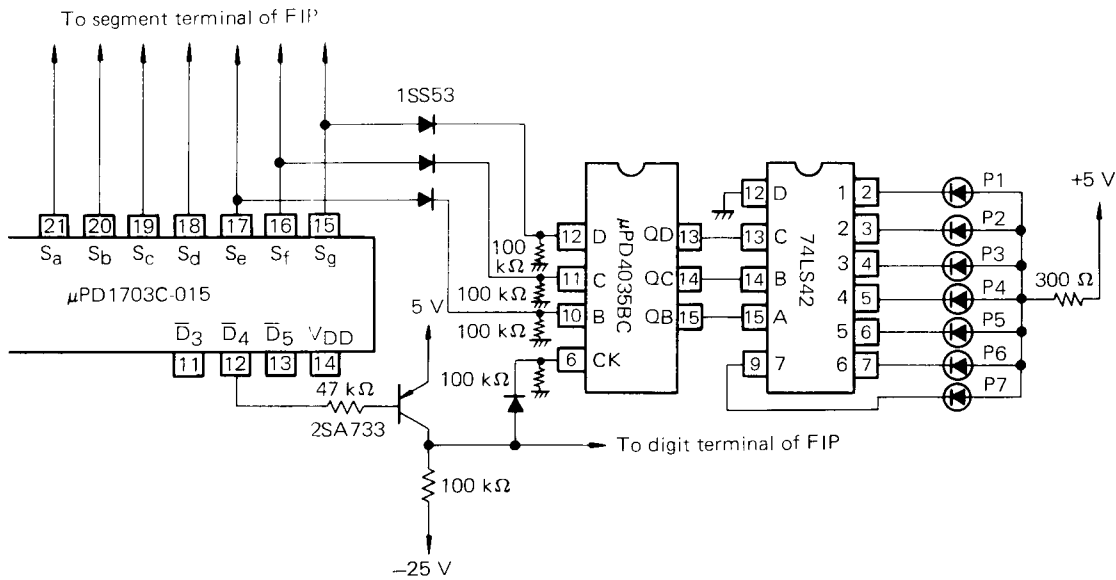
Fig. 3 Example of preset station display connection
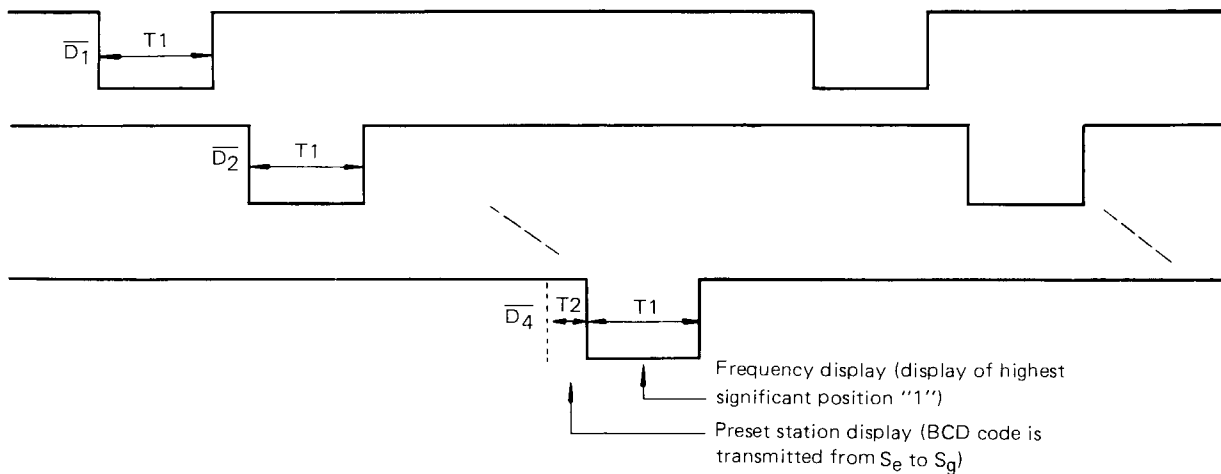
Fig. 4 Timing chart

At the timing T1 of digit signal $\overline{D_4}$, S_b and S_c provide the display signal of '1', upper digit of frequency. At the timing of T2, S_e to S_g provide BCD output to display the preset station.

Note: The preset stations are indicated by 7 discrete LED's (P1 to P7) by depressing corresponding PRESET keys
(M1 to M7).

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As shown in Fig. 4, these BCD otuput is multiplex, it is required to be converted to static drive output. The μPD4035C is a D-F/F for this purpose. In order to luch μPD4035C by rising signal of digit $\overline{D_4}$, active high, the digit output of μPD1703C-015 should be inverted.

Output status of segment terminal, S_a to S_g at the timing T1, T2 of digit $\overline{D_4}$

SEGMENT / TIMING	S_a	S_b	S_c	S_d	S_e	S_f	S_g
T1	blank	display '1' of upper digit	blank	blank	blank	blank	blank
T2	blank	blank	blank	blank	BCD output		

Preset station BCD code output

S_g	S_f	S_e	PRESET CHANNEL
0	0	1	P1 (M1 key)
0	1	0	P2 (M2 key)
0	1	1	P3 (M3 key)
1	0	0	P4 (M4 key)
1	0	1	P5 (M5 key)
1	1	0	P6 (M6 key)
1	1	1	P7 (M7 key)

4. TIMING CHART

4.1 DISPLAY AND TAKING IN

(1) $\overline{D}_1$ to $\overline{D}_3$, $\overline{D}_5$

(2) $\overline{D}_4$

4.2 MUTE TIMING CHART

① Key ON chattering preventing time

② Mute leading time

③ Division ratio setting and display content updating time

④ Mute trailing time

⑤ Scan time

⑥ PLL lock up time

(1) Manual up/down

(2) Auto up/down

When SD signal is input

When no SD signal is input

(3) Preset memory call

(4) When FM/MW/LW are switched and power is ON (CE = Low High)
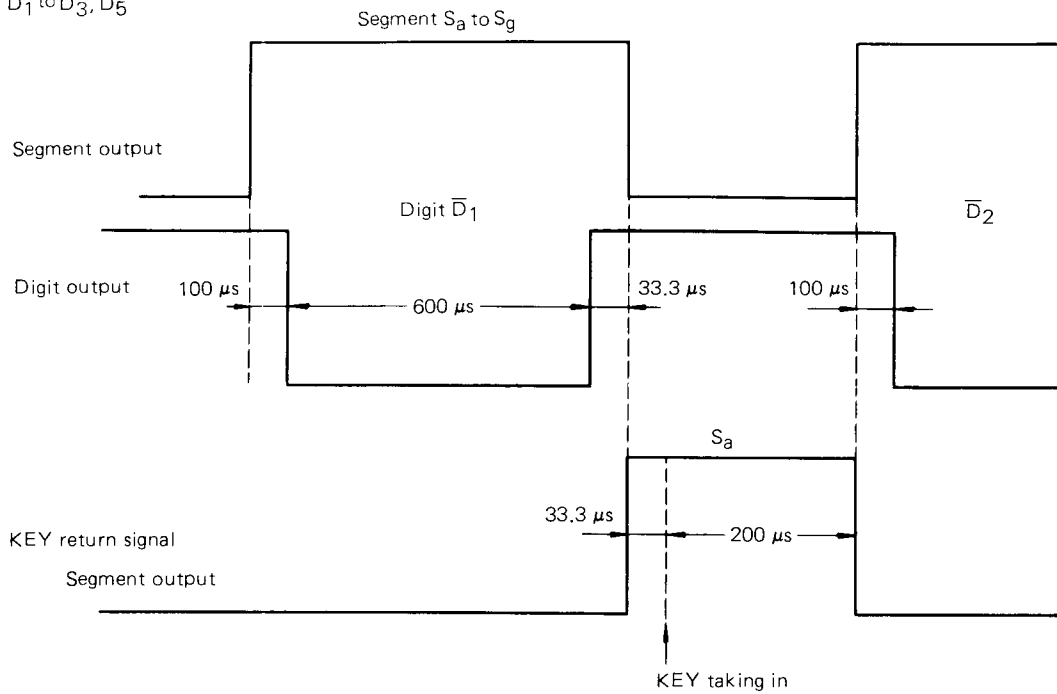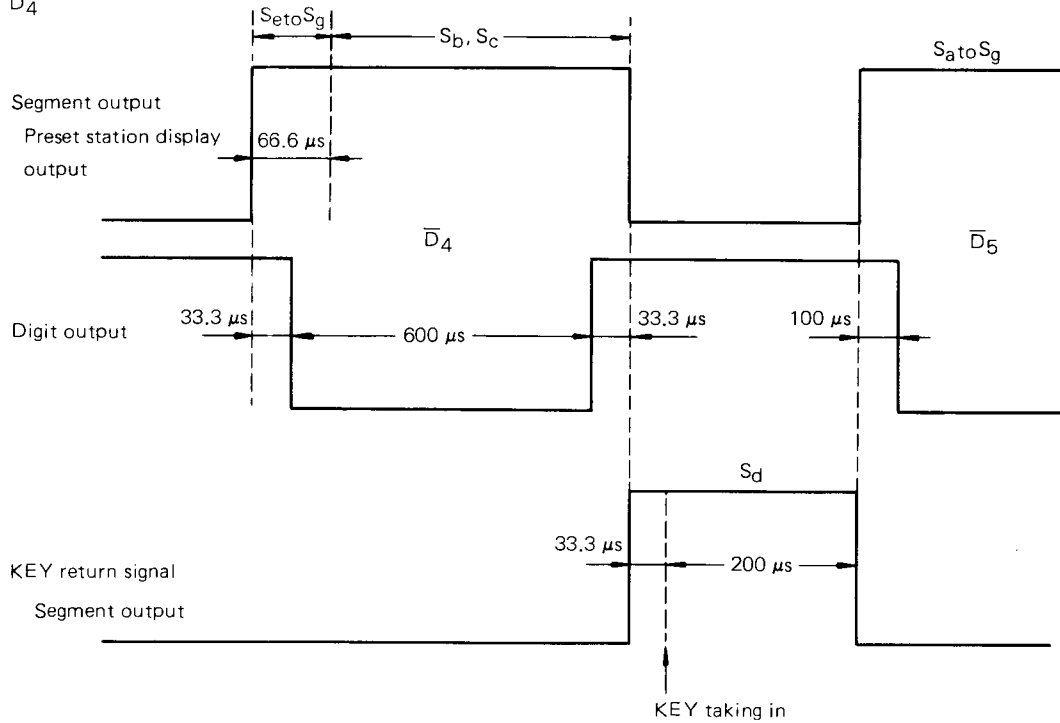
5. APPLICATION OF BAND SELECTION

If the momentary switch is used for band selection of FM, MW, LW, it is possible to switch over power supply of the tuner as shown below. The character display output signal, "FM", "MW", "LW", are used to be input of above circuits.

The active high signal is feeded through a buffer, consist of one PNP transistor, from $\overline{D}_5$ terminal of μPD1703C-015 and used to be CLOCK signal ($\overline{D}_5$).

Application I

Application II

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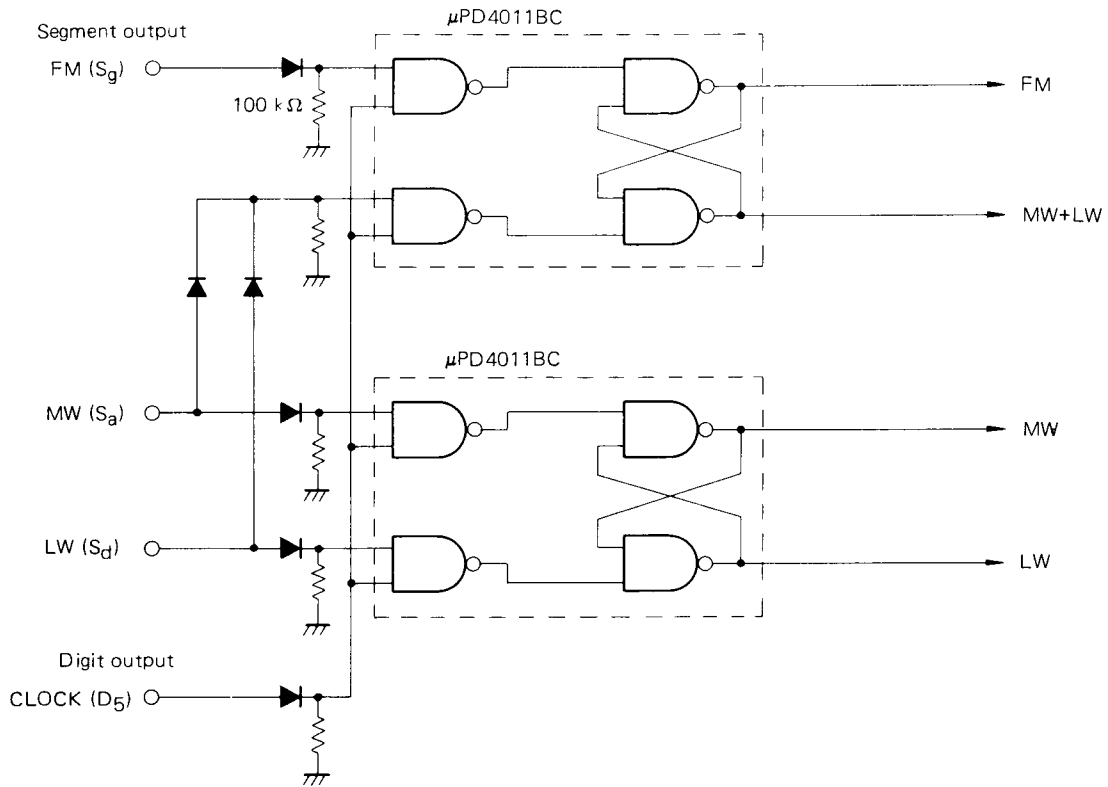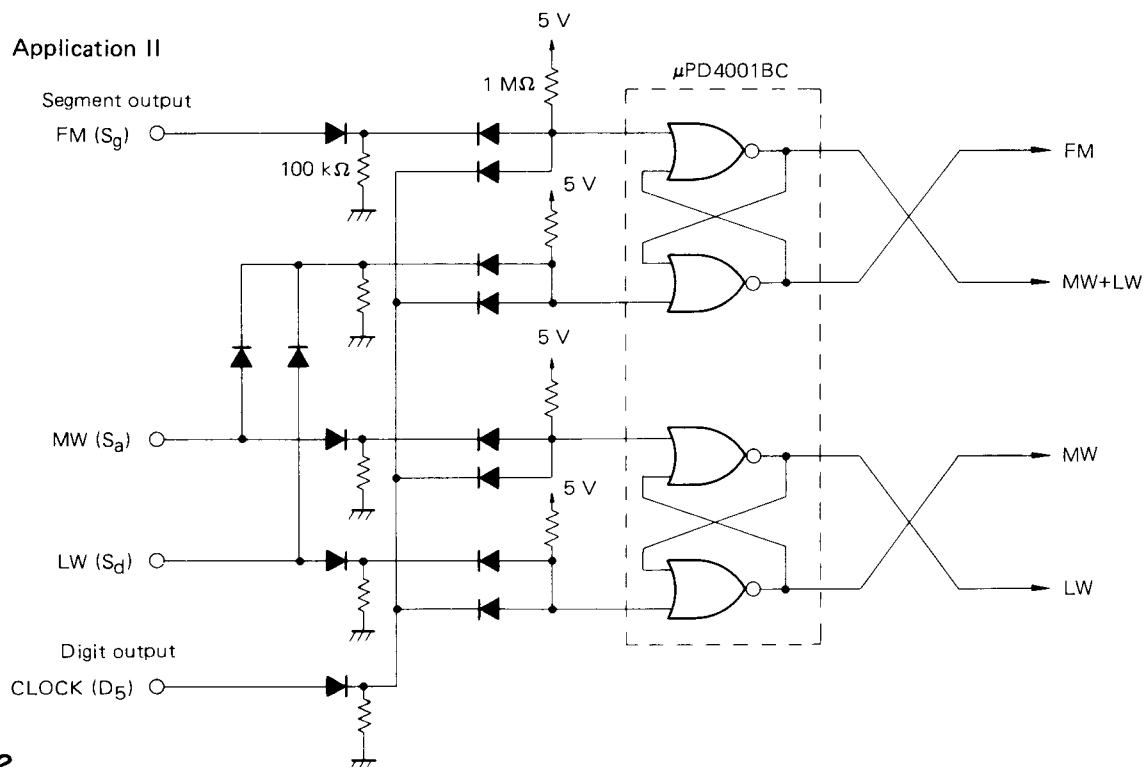
6. EXTERNAL DATA PRESET

The frequency information consisted by 8 bits data is stored into the FM, MW preset memories (M1 to M7) through key inputs (K0 to K3) of μPD1703C-015 from external microprocessor, such as TK-80, etc.

The frequency data consists of channel number coded in 8 bits; these 8 bits data are divided into two 4 bits portion — "DATA H" and "DATA L". Any frequency in the radio band — FM: 87.50 to 108.00 MHz, MW: 522 to 1 611 kHz — can be stored.

Fig. 5 shows flow chart of μPD1703C-015.

; Wait for 1 ms after EXT. DATA PRESET key is released.

; Wait for 125 ms detecting the input of SD pin.

; If it passes over 125 ms receiving no high level input to SD pin, the program jump out from this routine, and the last channel is recalled.

; Receive DATA H (4 bits) of FM.

; Receive DATA L (4 bits) of FM.
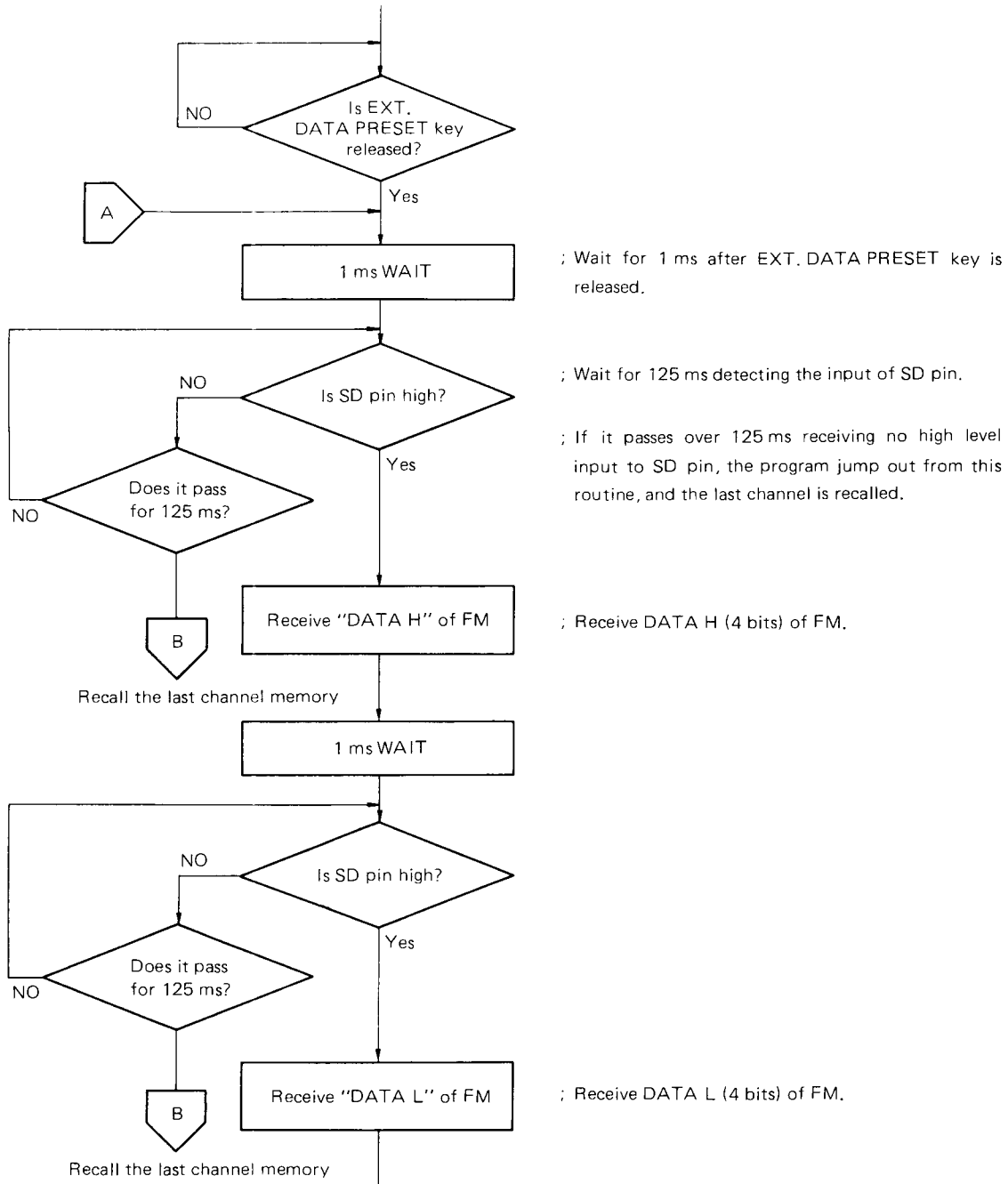
Fig. 5 Flow chart of external data preset
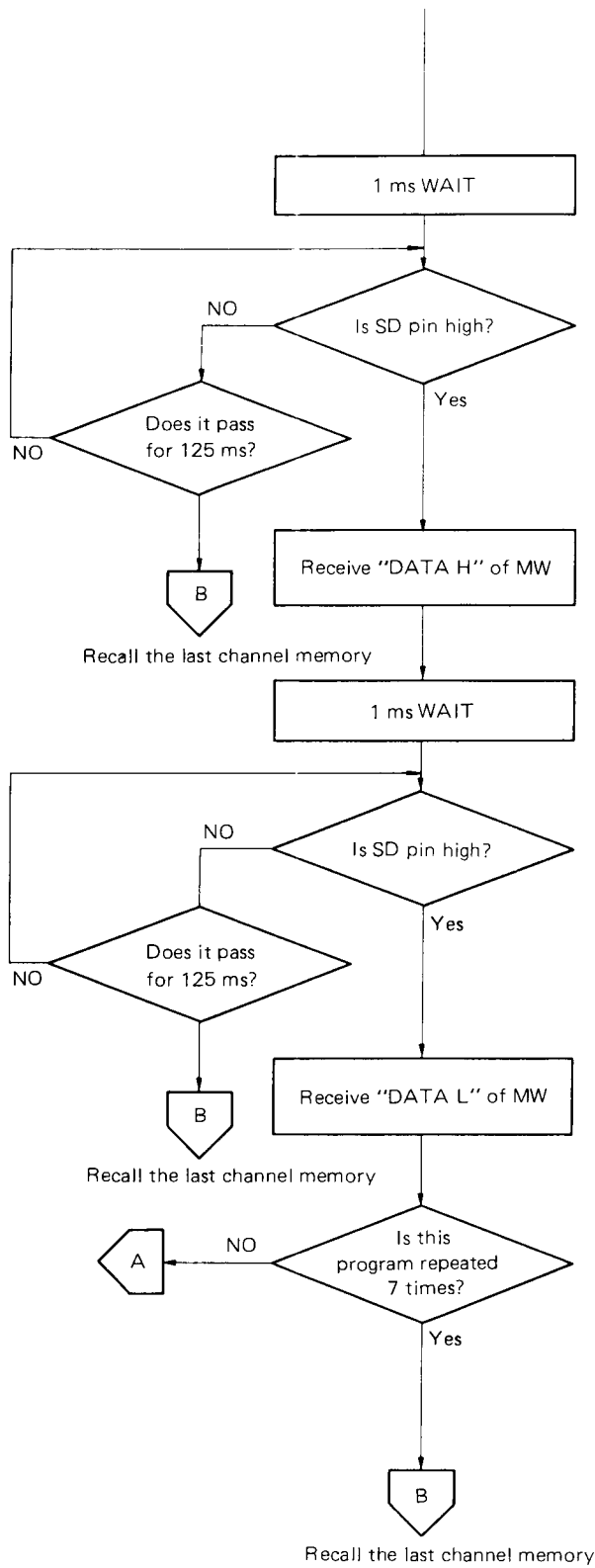
```
                    ┌─────────────────────┐
                    │      1 ms WAIT      │          ; Occupy DATA of MW after this.
                    └─────────────────────┘
                              │
        ┌─────────────────────┤
        │            NO   ◇ Is SD pin high? ◇
        │         ┌──────◇                 ◇
        │         │       ◇               ◇
        │         ▼           │ Yes
        │    ◇ Does it pass ◇     │
        │    ◇              ◇     │
   NO   └────◇ for 125 ms?  ◇     │
                ◇          ◇      │
                     │            ▼
                     ▼     ┌─────────────────────┐
                    ╱B╲    │  Receive "DATA H" of MW │   ; Receive DATA H (4 bits) of MW.
                   ╱___╲   └─────────────────────┘
          Recall the last channel memory     │
                                             ▼
                    ┌─────────────────────┐
                    │      1 ms WAIT      │
                    └─────────────────────┘
                              │
        ┌─────────────────────┤
        │            NO   ◇ Is SD pin high? ◇
        │         ┌──────◇                 ◇
        │         ▼           │ Yes
        │    ◇ Does it pass ◇     │
   NO   └────◇ for 125 ms?  ◇     │
                     │            ▼
                     ▼     ┌─────────────────────┐
                    ╱B╲    │  Receive "DATA L" of MW │   ; Receive DATA L (4 bits) of MW.
                   ╱___╲   └─────────────────────┘
          Recall the last channel memory     │
                                             ▼
                ╱A╲   NO   ◇ Is this          ◇
               ╱___╲◄──────◇ program repeated ◇
                          ◇   7 times?        ◇
                               │ Yes
                               ▼
                              ╱B╲
                             ╱___╲
                 Recall the last channel memory
```

; After the preset memories, M1 through M7 are occupied by the data, this procedure go out from this flow to another mode which recall the last channel memory.

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Table 2. EXT. DATA PRESET frequency data (channel number)

DATA H	DATA L	FM Freq.	MW Freq.
0	0	87.50 MHz	522 kHz
0	1	87.60	531
0	2	87.70	540
0	3	87.80	549
0	4	87.90	558
0	5	88.00	567
0	6	88.10	576
0	7	88.20	585
0	8	88.30	594
0	A	88.40	603
0	B	88.50	612
0	C	88.60	621
0	D	88.70	630
0	E	88.80	639
0	F	88.90	648
1	0	89.00	657
1	1	89.10	666
1	2	89.20	675
7	7	99.40	1493
7	8	99.50	1502
7	9	99.60	1611
7	A	99.70	1611
7	B	99.80	1611
C	9	107.60	1611
C	A	107.70	1611
C	B	107.80	1611
C	C	107.90	1611
C	D	108.00	1611

Note: DATA H, L is HEX decimal code.

7. APPLICATION CIRCUIT
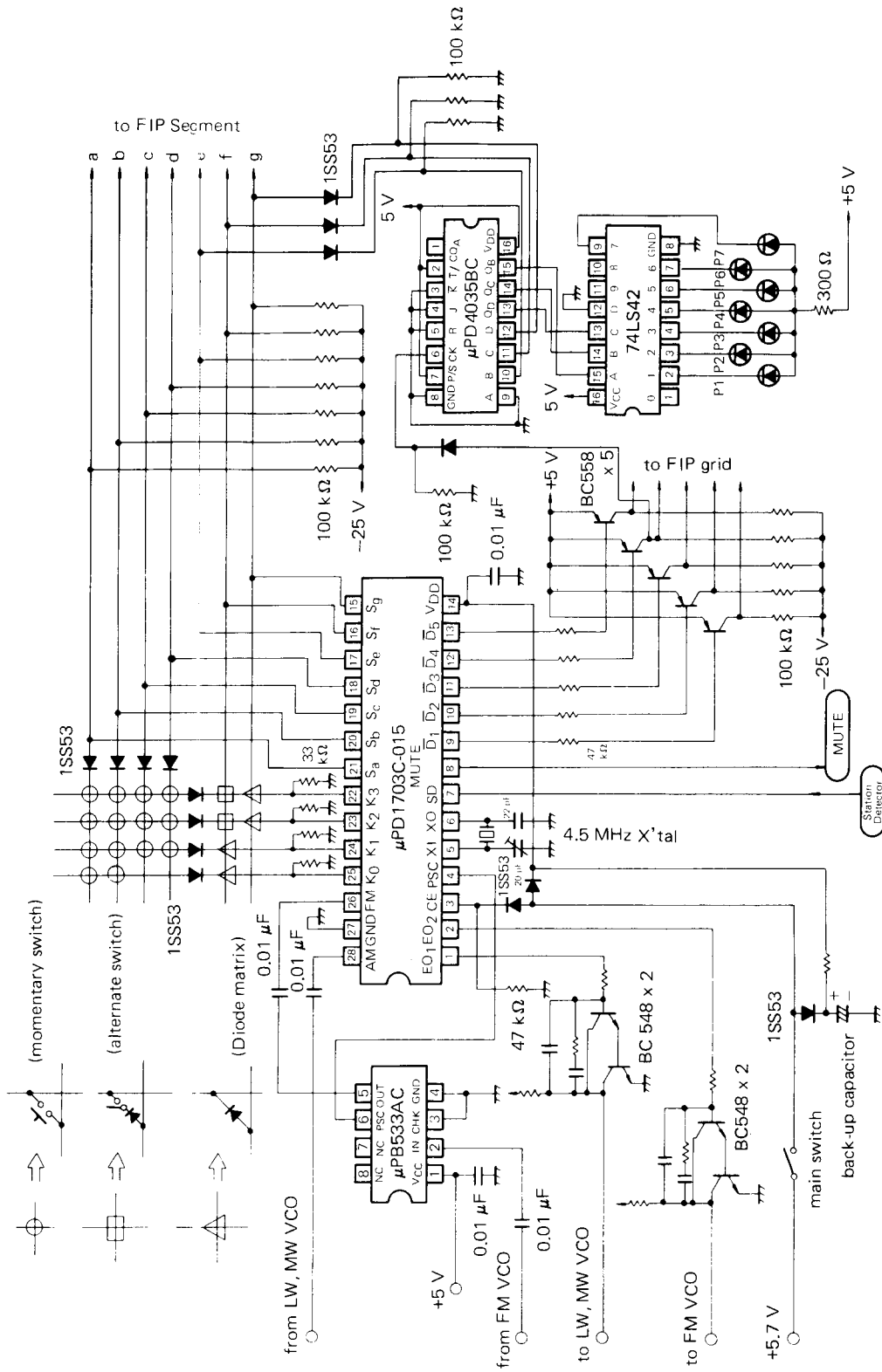
The applied circuits and circuit constants listed in this material are not intended for mass production design with deviations and temperature characteristics of component parts considered. Further, this company will not assume any responsibility as regards the patents on the circuits listed in this material.

8. ELECTRICAL CHARACTERISTICS

8.1 ABSOLUTE MAXIMUM RATINGS

Supply voltage	V_{DD}	−0.3 to +6.0	V
Input voltage	V_I	−0.3 to +V_{DD}	V
Output voltage	V_O	−0.3 to +V_{DD}	V
Output absorption current	I_O	10	mA
Operating temperature	T_{OPT}	−35 to +75	°C
Storage temperature	T_{stg}	−55 to +125	°C
Withstanding output voltage	V_{BDS}	S_a to S_g terminals −35 (Inter-drain source voltage)	V

8.2 RECOMMENDED OPERATING CONDITIONS

| CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Supply voltage	V_{DD}	4.5	5.0	5.5	V	
RAM retention voltage	V_{RAM}	2.5			V	CE terminal = 0
Withstanding output voltage	V_{BDS}			−30	V	S_a to S_g terminals (Inter-drain source voltage) $I_{OFF} = -5 \mu A$
Supply voltage rise time	T_{rise}			500	ms	$V_{DD} = 0 \rightarrow 4.5$ V

8.3 DC CHARACTERISTICS (V_{DD} = +4.5 to +5.5 V, T_a = −35 to +75 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
High level input voltage	V_{IH1}	0.8 V_{DD}		V_{DD}	V	SD terminal
High level input voltage	V_{IH2}	0.7 V_{DD}		V_{DD}	V	CE terminal
High level input voltage	V_{IH3}	0.6 V_{DD}		V_{DD}	V	K_0 to K_3 terminals
Low level input voltage	V_{IL1}	0		0.3 V_{DD}	V	CE terminal
Low level input voltage	V_{IL2}	0		0.2 V_{DD}	V	SD, K_0 to K_3 terminals
High level output voltage	V_{OH1}	4.0			V	PSC, MUTE, D_1 to D_5 terminals I_{OH}=−0.2 mA
High level output voltage	V_{OH2}	4.0			V	EO_1, EO_2 terminals I_{OH}=−0.5mA
High level output voltage	V_{OH3}	3.0			V	S_a to S_g terminals I_{OH}=−0.5mA
Low level output voltage	V_{OL1}			0.5	V	EO_1, EO_2 terminals I_{OL}=0.5 mA
Low level output voltage	V_{OL2}			0.5	V	MUTE, $\overline{D_1}$ to $\overline{D_5}$, PSC terminals I_{OL}=0.2 mA
High level input current	$+I_{IH1}$	5.0	25	100	μA	K_0 to K_3 terminals V_{IN}=V_{DD}=5.0 V
High level input current	$+I_{IH2}$		300		μA	X_I terminal V_{IN}=V_{DD}=5.0 V
Low level input current	$-I_{IL1}$		300		μA	AM, FM terminals V_{IN}=0 V, V_{DD}=5.0 V
Output leakage current	I_L		10^{-3}	1	μA	EO_1, EO_2 terminals V_O=V_{DD}=5.0 V
AC input voltage	V_{in}	1.0		V_{DD}	Vp-p	AM, FM terminals
Operating current	I_{DD1}		3		mA	Normal operation (excluding display current)
Operating current	I_{DD2}			10	μA	CE terminal = 0, T_a=25 °C, V_{DD}=5 V
RAM retention voltage	V_{RAM}	2.5			V	CE terminal = 0
Withstanding output voltage	V_{BDS}			−30	V	S_a to S_g terminals (Inter-drain source voltage), I_{OFF}=−5 μA

8.4 AC CHARACTERISTICS (V_{DD} = +4.5 to +5.5 V, T_a = −35 to +75 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Operating Frequency	f_{AM}	0.5		2.5	MHz	AM terminal V_{in}=1.0 V_{p-p} (MIN.), DC cut
Operating Frequency	f_{FM}	0.5		8.8	MHz	FM terminal, V_{in} = 0.8 V_{p-p} (MIN.), square wave, DC cut

9. PACKAGE DIMENSION (Unit: mm)
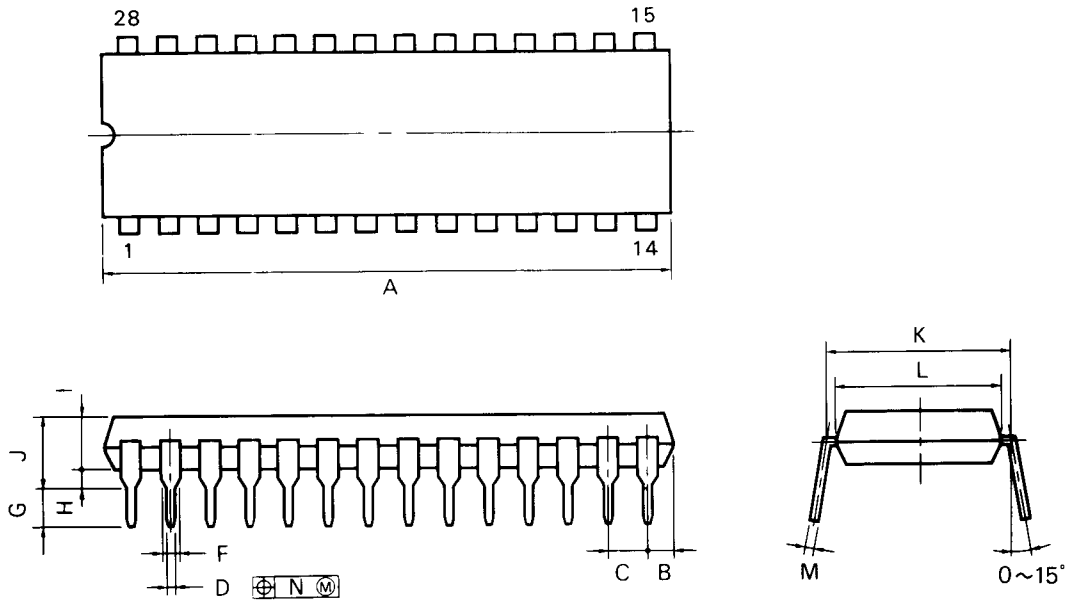
P28C-100-600A1

NOTES

1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	38.10 MAX.	1.500 MAX.
B	2.54 MAX.	0.100 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	$0.50^{+0.10}$	$0.020^{+0.004}_{-0.005}$
F	1.2 MIN.	0.047 MIN.
G	$3.6^{+0.3}$	$0.142^{\pm0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.72 MAX.	0.226 MAX.
K	15.24 (T.P.)	0.600 (T.P.)
L	13.2	0.520
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01