TOSHIBA CMOS Digital Integrated Circuit   Silicon Monolithic

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Octal D-Type Latch with 3-State Output

The TC7MH373FK is an advanced high speed CMOS octal latch with 3-state output fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent bipolar schottky TTL while marinating the CMOS low power dissipation.

This 8 bit D-type latch is controlled by a latch enable input (LE) and a output enable input ($\overline{OE}$).

When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

An input protection circuit ensures the 0 to 7 V can be applied to the input pins can be used to interface 5 V to 3 V systems and two supply systems such as battery back up.

This circuit prevents destruction due to mismatched supply and input voltages.
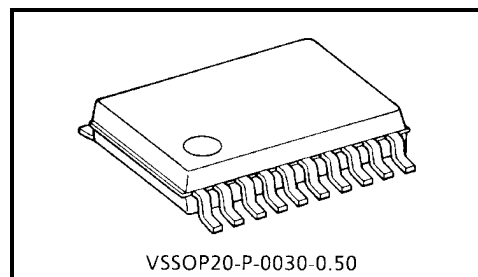
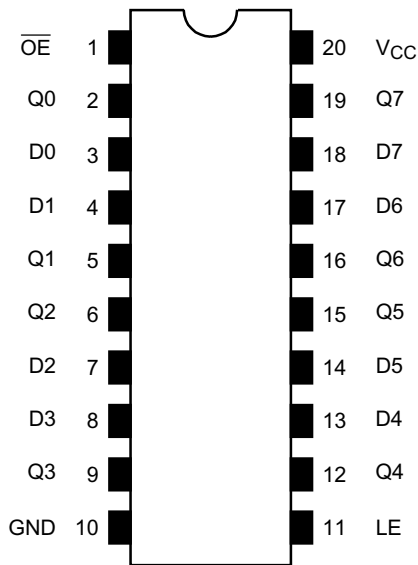VSSOP20-P-0030-0.50

Weight: 0.03 g (typ.)

Features

- High speed: t_{pd} = 5.0 ns (typ.) (V_{CC} = 5 V)
- Low power dissipation: I_{CC} = 4 μA (max) (Ta = 25°C)
- High noise immunity: V_{NIH} = V_{NIL} = 28% V_{CC} (min)
- Power down protection is provided on all inputs.
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range: $V_{CC\ (opr)}$ = 2~5.5 V
- Low noise: V_{OLP} = 0.8 (max)
- Pin and function compatible with 74ALS373

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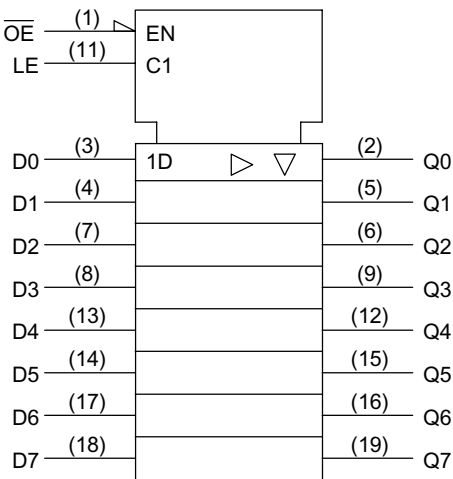
Pin Assignment (top view)

```
      OE   1          20   VCC
      Q0   2          19   Q7
      D0   3          18   D7
      D1   4          17   D6
      Q1   5          16   Q6
      Q2   6          15   Q5
      D2   7          14   D5
      D3   8          13   D4
      Q3   9          12   Q4
     GND  10          11   LE
```

IEC Logic Symbol

```
  OE  —(1)—▷ EN
  LE  —(11)— C1

  D0 —(3)—  1D  ▷  ▽  —(2)—  Q0
  D1 —(4)—                —(5)—  Q1
  D2 —(7)—                —(6)—  Q2
  D3 —(8)—                —(9)—  Q3
  D4 —(13)—               —(12)— Q4
  D5 —(14)—               —(15)— Q5
  D6 —(17)—               —(16)— Q6
  D7 —(18)—               —(19)— Q7
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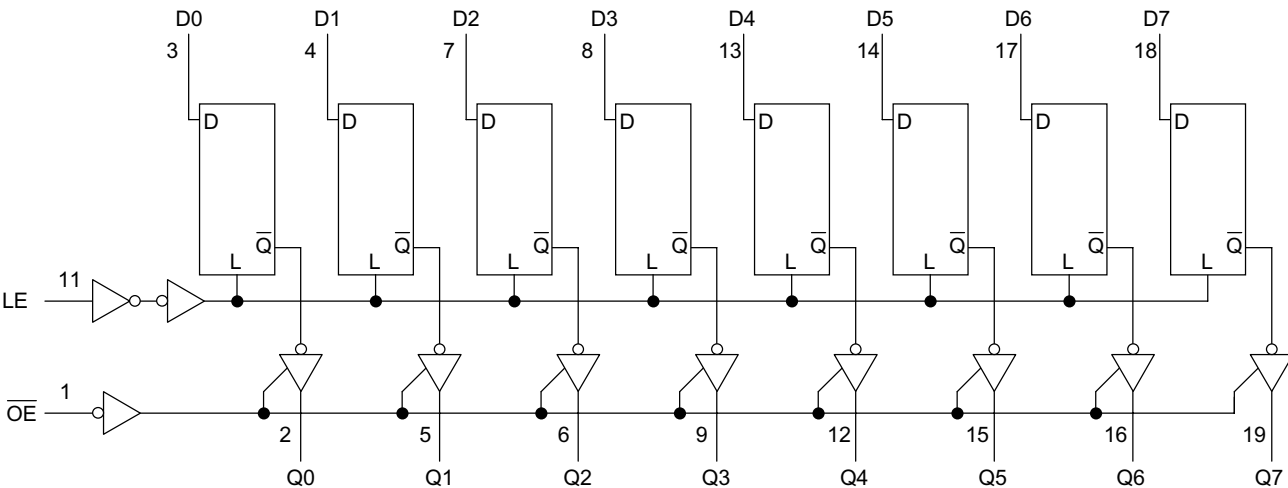
Truth Table

Inputs			Outputs
$\overline{OE}$	LE	D	
H	X	X	Z
L	L	X	Q_n
L	H	L	L
L	H	H	H

X: Don't care

Z: High impedance

Q_n: Q outputs are latched at the time when the LE input is taken to a low logic level.

System Diagram

Maximum Ratings

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	$-0.5 \sim 7.0$	V
DC input voltage	V_{IN}	$-0.5 \sim 7.0$	V
DC output voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
Input diode current	I_{IK}	-20	mA
Output diode current	I_{OK}	± 20	mA
DC output current	I_{OUT}	± 25	mA
DC V_{CC}/ground current	I_{CC}	± 75	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	$-65 \sim 150$	°C

Recommended Operating Conditions

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	$2.0 \sim 5.5$	V
Input voltage	V_{IN}	$0 \sim 5.5$	V
Output voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating temperature	T_{opr}	$-40 \sim 85$	°C
Input rise and fall time	dt/dv	$0 \sim 100$ ($V_{CC} = 3.3 \pm 0.3$ V) $0 \sim 20$ ($V_{CC} = 5 \pm 0.5$ V)	ns/V

Electrical Characteristics

DC Characteristics

Characteristics		Symbol	Test Condition		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		Unit
						Min	Typ.	Max	Min	Max	
Input voltage	High level	V_{IH}	—		2.0	1.50	—	—	1.50	—	V
					3.0~5.5	$V_{CC} \times 0.7$	—	—	$V_{CC} \times 0.7$	—	
	Low level	V_{IL}	—		2.0	—	—	0.50	—	0.50	
					3.0~5.5	—	—	$V_{CC} \times 0.3$	—	$V_{CC} \times 0.3$	
Output voltage	High level	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50$ μA	2.0	1.9	2.0	—	1.9	—	V
					3.0	2.9	3.0	—	2.9	—	
					4.5	4.4	4.5	—	4.4	—	
				$I_{OH} = -4$ mA	3.0	2.58	—	—	2.48	—	
				$I_{OH} = -8$ mA	4.5	3.94	—	—	3.80	—	
	Low level	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50$ μA	2.0	—	0	0.1	—	0.1	
					3.0	—	0	0.1	—	0.1	
					4.5	—	0	0.1	—	0.1	
				$I_{OL} = 4$ mA	3.0	—	—	0.36	—	0.44	
				$I_{OL} = 8$ mA	4.5	—	—	0.36	—	0.44	
3-state output off-state current		I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND		5.5	—	—	±0.25	—	±2.50	μA
Input leakage current		I_{IN}	$V_{IN} = 5.5$ V or GND		0~5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current		I_{CC}	$V_{IN} = V_{CC}$ or GND		5.5	—	—	4.0	—	40.0	μA

Timing Requirements (Input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Ta = 25°C Typ.	Ta = 25°C Limit	Ta = −40~85°C Limit	Unit
Minimum pulse width (LE)	$t_{w (H)}$	—	3.3 ± 0.3	—	5.0	5.0	ns
			5.0 ± 0.5	—	5.0	5.0	
Minimum set-up time	t_s	—	3.3 ± 0.3	—	4.0	4.0	ns
			5.0 ± 0.5	—	4.0	4.0	
Minimum hold time	t_h	—	3.3 ± 0.3	—	1.0	1.0	ns
			5.0 ± 0.5	—	1.0	1.0	

AC Characteristics (Input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition	V_{CC} (V)	C_L (pF)	Ta = 25°C Min	Ta = 25°C Typ.	Ta = 25°C Max	Ta = −40~85°C Min	Ta = −40~85°C Max	Unit
Propagation delay time (LE-Q)	t_{pLH} t_{pHL}	—	3.3 ± 0.3	15	—	7.0	11.0	1.0	13.0	ns
				50	—	9.5	14.5	1.0	16.5	
			5.0 ± 0.5	15	—	4.9	7.2	1.0	8.5	
				50	—	6.4	9.2	1.0	10.5	
Propagation delay time (D-Q)	t_{pLH} t_{pHL}	—	3.3 ± 0.3	15	—	7.3	11.4	1.0	13.5	ns
				50	—	9.8	14.9	1.0	17.0	
			5.0 ± 0.5	15	—	5.0	7.2	1.0	8.5	
				50	—	6.5	9.2	1.0	10.5	
3-state output enable time	t_{pZL} t_{pZH}	$R_L = 1$ kΩ	3.3 ± 0.3	15	—	7.3	11.4	1.0	13.5	ns
				50	—	9.8	14.9	1.0	17.0	
			5.0 ± 0.5	15	—	5.5	8.1	1.0	9.5	
				50	—	7.0	10.1	1.0	11.5	
3-state output disable time	t_{pLZ}	$R_L = 1$ kΩ	3.3 ± 0.3	50	—	9.5	13.2	1.0	15.0	ns
	t_{pHZ}		5.0 ± 0.5	50	—	6.5	9.2	1.0	10.5	
Output to output skew	t_{osLH}	(Note1)	3.3 ± 0.3	50	—	—	1.5	—	1.5	ns
	t_{osHL}		5.0 ± 0.5	50	—	—	1.0	—	1.0	
Input capacitance	C_{IN}	—			—	4	10	—	10	pF
Bus input capacitance	C_{OUT}	—			—	6	—	—	—	pF
Power dissipation capacitance	C_{PD}	(Note2)			—	27	—	—	—	pF

Note1: This parameter is guaranteed by design.

$t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

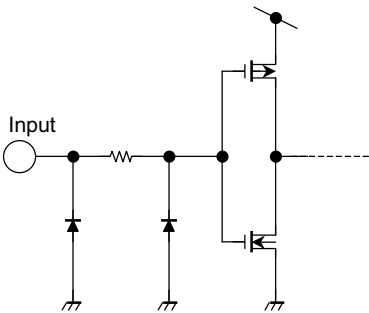$I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per latch)

And the total CPD when n pcs of latch operate can be gained by the following equation:

C_{PD} (total) $= 14 + 13 \cdot n$

Noise Characteristics (Input: $t_r = t_f = 3$ ns)

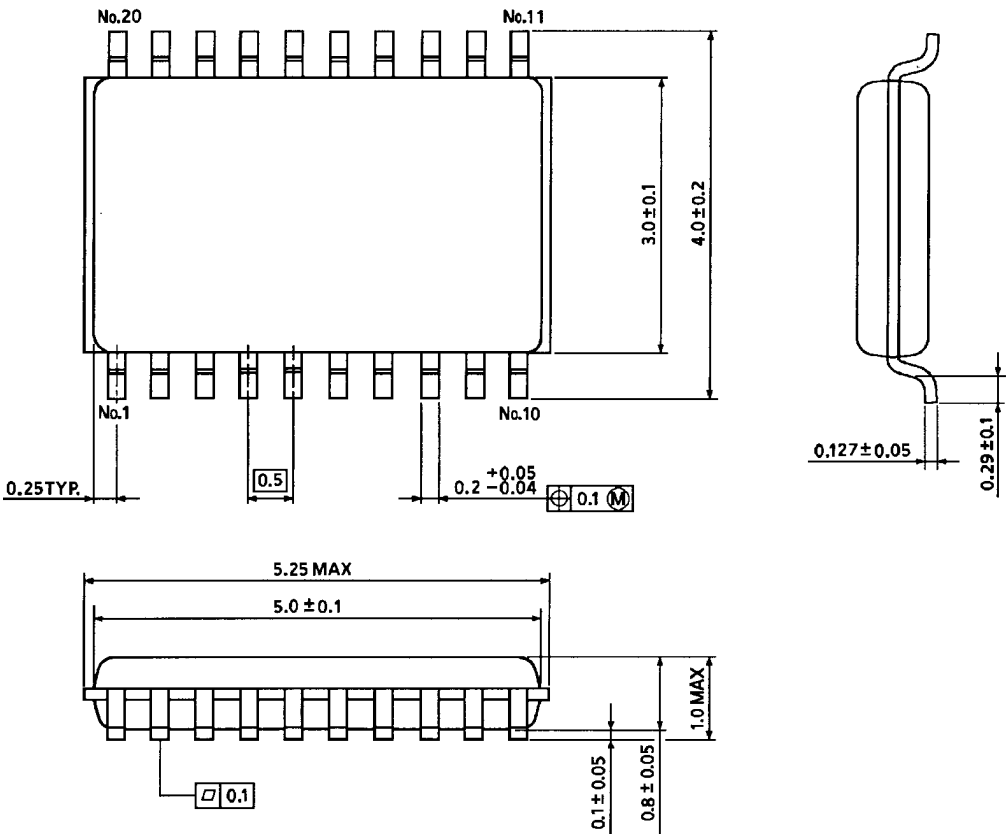| Characteristics	Symbol	Test Condition	V_{CC} (V)	Ta = 25°C Typ.	Limit	Unit
Quiet output maximum dynamic V_{OL}	V_{OLP}	$C_L = 50$ pF	5.0	0.5	0.8	V
Quiet output minimum dynamic V_{OL}	V_{OLV}	$C_L = 50$ pF	5.0	−0.5	−0.8	V
Minimum high level dynamic input voltage V_{IH}	V_{IHD}	$C_L = 50$ pF	5.0	—	3.5	V
Maximum low level dynamic input voltage V_{IL}	V_{ILD}	$C_L = 50$ pF	5.0	—	1.5	V

Input Equivalent Circuit

Package Dimensions

VSSOP20-P-0030-0.50   Unit : mm

No.20   No.11

3.0±0.1
4.0±0.2

No.1   No.10

0.25 TYP.   0.5   0.2 +0.05 −0.04   ⊕ 0.1 Ⓜ

0.127±0.05   0.29±0.1

5.25 MAX
5.0±0.1

1.0 MAX

▱ 0.1

0.1±0.05   0.8±0.05

Weight: 0.03 g (typ.)