8-Bit Latch/Register with Readback

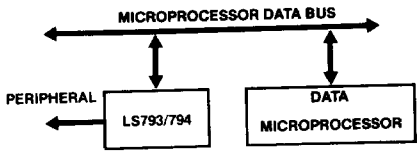
SN54/74LS793 SN54/74LS794

Features/Benefits

- **I/O port configuration enables output data back onto input bus**
- **8-bit data path matches byte boundaries**
- **Ideal for microprocessor interface**

Description

These 8-bit latches/registers are useful for I/O operations on a microprocessor bus. An image of the output data can be read back by the CPU. This operation is important in control algorithms which make decisions based on the previous status of output controls. Rather than storing a redundant copy of the output data in memory, simply reading the register as an I/O port allows the data to be retrieved from where it has been stored in an 'LS793/4, for verification and/or updating.



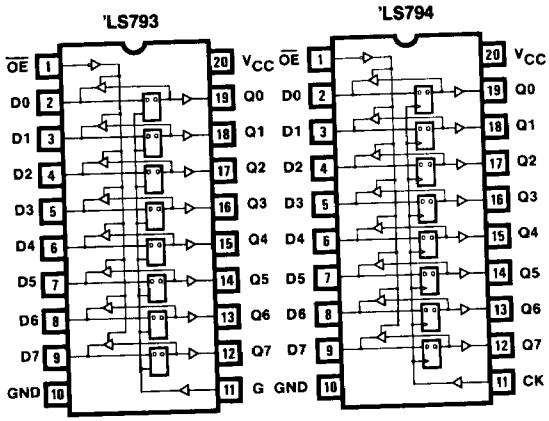
The data is loaded in the registers on the low-to-high transition of the clock (CK), for the 'LS794. The data is passed through the 'LS793 when the gate, (G), is High, and it is "latched" when G changes to Low. The output enable, $\overline{OE}$ is used to enable data on D7-D0. When $\overline{OE}$ is low the output of the latches/registers is enabled on D0-D7, enabling D as an output bus so that the host can perform a read operation. When $\overline{OE}$ is High, D7-D0 are inputs to the latches/registers configuring D as an input bus.

The output drive of these commercial parts for any output pin is I_{OL} = 24 mA.

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	TYPE	POWER
SN54LS793 SN74LS793	J,W,L, N,J,NL	Mil Com	Non-invert	Latch	LS
SN54LS794 SN74LS794	J,W,L, N,J,NL	Mil Com		Register	

Logic Symbols



'LS793 Function Table

G	$\overline{OE}$	Q	D
L	L	Q_0**	Output, Q
L	H	Q_0**	Input
H†	L	D*	Output, Q*
H	H	D	Input

* In this case the output of the latch feeds the input, and a "race" condition results.

** Q_0 represents the previous "latched" state.

† This transition is not a normal mode of operation and may produce hazards.

'LS794 Function Table

CK	$\overline{OE}$	Q	D
L or H or ↓	L	Q_0	Output, Q
L or H or ↓	H	Q_0	Input
↑	L	Q_0	Output, Q*
↑	H	D	Input

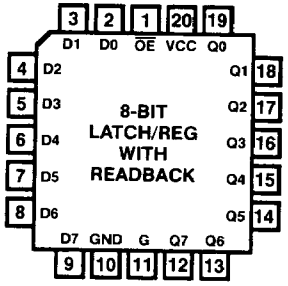
* In this case the output of the register is clocked to the inputs and the overall Q output is unchanged at Q_0.

TWX: 910-338-2376
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374

Monolithic Memories

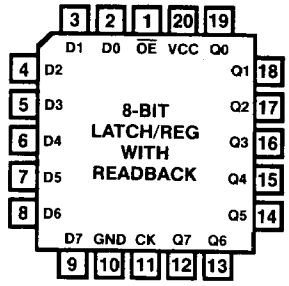
Pin Configurations

SN74LS793



Plastic Chip Carrier

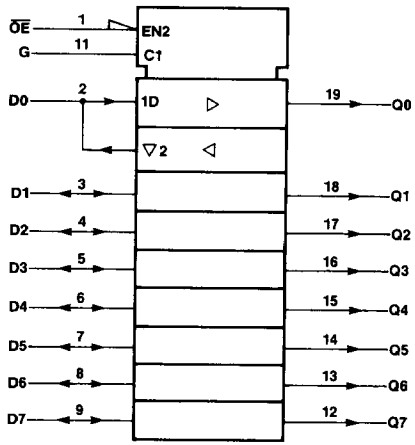
SN74LS794



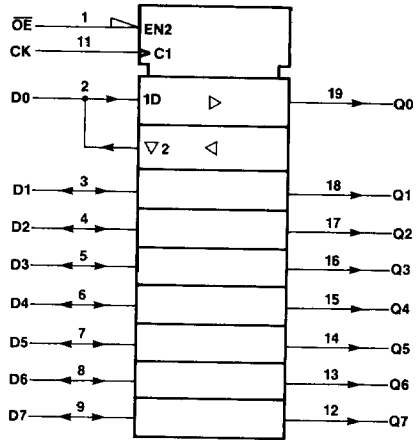
Plastic Chip Carrier

IEEE Symbols

'LS793



'LS794



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Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER			MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage			4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free air temperature			-55		125	0		75	°C
t_w	Width of Clock/Gate	High		15			15			ns
		Low ('LS794 only)		15			15			
t_{su}	Setup time		'LS793	15↓			10↓			ns
			'LS794	15↑			15↑			
t_h	Hold time		'LS793	10↓			10↓			
			'LS794	0↑			0↑			

↑ ↓ The arrow indicates the transition of the clock/gate input used for reference. ↑ for the low-to-high transitions, ↓ for the high-to-low transitions.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IH}	High-level input voltage				2			2			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = -18 mA			-1.5			-1.5	V
I_{IL}	Low-level input current		V_{CC} = MAX	V_I = 0.4 V			-250			-250	μA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.7 V			40			40	μA
I_I	Maximum input current	D or Q	V_{CC} = MAX	V_I = 5.5 V			0.1			0.1	mA
		All others		V_I = 7 V							
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OH} = -1 mA	2.4	3.4					V
				I_{OH} = -2.6 mA				2.4	3.1		
I_{OZL}	Off-state output current		V_{CC} = MAX, V_{IL} = MAX, V_{IH} = = 2 V	V_O = 0.4 V			-250			-250	μA
I_{OZH}				V_O = 2.7 V			40			40	
I_{OS}	Output short-circuit current*		V_{CC} = MAX		-30		-130	-30		-130	mA
I_{CC}	Supply current		V_{CC} = MAX, Outputs open	'LS793			120			120	mA
				'LS794			120			120	

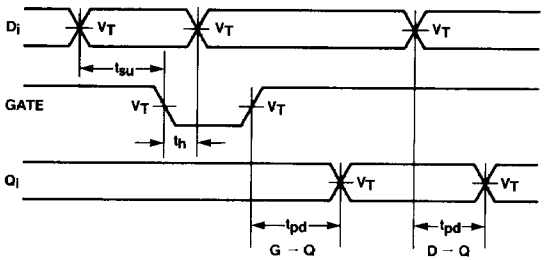
* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

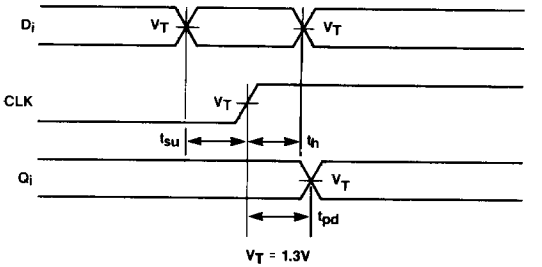
SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	'LS793 MIN	'LS793 TYP	'LS793 MAX	'LS794 MIN	'LS794 TYP	'LS794 MAX	UNIT
f_{MAX}	Maximum clock frequency	C_L = 45pF R_L = 280 Ω				35	50		MHz
t_{PLH}	Data to output delay			12	18				ns
t_{PHL}				12	18				ns
t_{PLH}	Clock/gate to output delay			17	25		9	20	ns
t_{PHL}				12	25		14	20	ns
t_{PZL}	Output enable delay†			15	20		15	20	ns
t_{PZH}				11	20		11	20	ns
t_{PLZ}	Output disable delay†	C_L = 5pF R_L = 280 Ω		8	20		8	20	ns
t_{PHZ}				9	20		9	20	ns

† For the 'LS793, G should remain LOW during these tests.

'LS793 Timing Diagrams



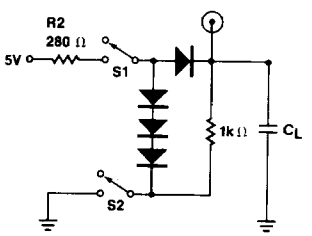
'LS794 Timing Diagrams



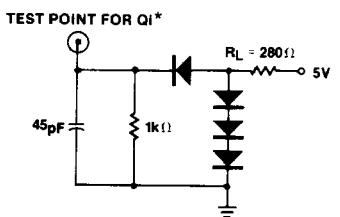
The case when gate is HIGH and data flows through the part is specified as Data to Output delay in the Switching Characteristics table. (V_T = 1.3V).

Test Loads

FOR D OUTPUTS-ENABLE AND DISABLE

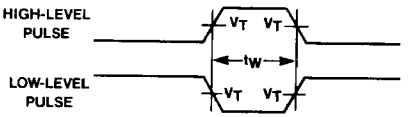


FOR Q OUTPUTS

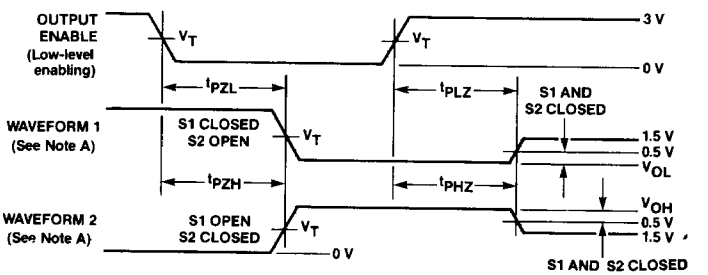


* The "TEST POINT" is drived by the output under test, and observed by instrumentation.

PULSE WIDTH



ENABLE AND DISABLE WAVEFORMS



For the 'LS793, the latch control "G" should be low while testing the enable and disable times, so that the output (Q) does not change. (V_T = 1.3V).

NOTES: A. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

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