Introduction

EG&G Reticon's D Series image sensors are high-speed, self-scanned, charge-coupled photodiode (CCPD) arrays. The D Series Family, consisting of the STANDARD-D, VALUE-D, FAST-D, and LOLIGHT-D image sensors, allows the designer to select just the right device for a particular application. Typical applications include optical character recognition, document scanning, inspection, pattern recognition, noncontact measurement, and other applications requiring high quality, broad spectral response image acquisitions.

Key Features

- Antiblooming
- Video data rates up to 30 MHz
- High photo sensitivity
- Wide dynamic range
- 256, 512, 1024, and 2048 elements
- 13 μm x 13 μm and 13 μm x 26 μm picture elements
- Low power consumption
- Wide spectral response (UV to near IR)

General Description

The D Series family of image sensors features the CCPD architecture which combines the best features of CCD and photodiode technology. The CCD read-out structure allows very high speed, low noise operation. The photodiode sensing elements provide superior light sensitivity, especially in the blue and near UV spectrum range.

The STANDARD-D device is the nominal component of the D Series family. It operates at data rates up to 20 MHz, has 13 μm x 13 μm pixels, and features very high dynamic range. The VALUE-D device is a lower cost version with all the same features as the STANDARD-D, but has a maximum data rate of 10 MHz and slightly reduced dynamic The FAST-D device is specified for operation at data rates up to 30 MHz. The LOLIGHT-D device is a wide-aperture version featuring 13 μm x 26 μm pixels for higher photo sensitivity.

Functional Description

The sensing elements for the D Series Linear CCPDs are a row of diffused p-n junction photodiodes spaced on 13 μm centers and interdigitated into a sensing aperture 13 μm wide (26 μm for LOLIGHT-D). The photodiode sensing elements provide very broad spectral response while the CCD readout registers and output buffer amplifiers allow very low-noise signal extraction. Figure 1 shows the pinout configuration and Figure 2 is a simplified schematic diagram. Figure 3 shows the aperture response function and sensor geometry. The dimensions shown in Figure 3 are as follows: the photodiode diffusion width a is 7 μm, the center-to-center spacing b is 13 μm and the aperture width c is 13 μm or 26 μm. Note that the
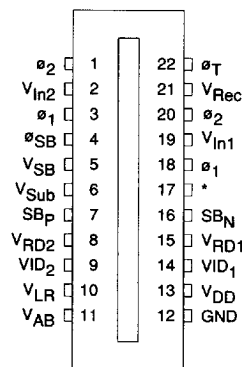
$\varnothing_2$	1	22	$\varnothing_T$
V_{In2}	2	21	V_{Rec}
$\varnothing_1$	3	20	$\varnothing_2$
$\varnothing_{SB}$	4	19	V_{In1}
V_{SB}	5	18	$\varnothing_1$
V_{Sub}	6	17	*
SB_P	7	16	SB_N
V_{RD2}	8	15	V_{RD1}
VID_2	9	14	VID_1
V_{LR}	10	13	V_{DD}
V_{AB}	11	12	GND

Figure 1. Pinout Configuration
* (Pin 17 is N/C for RL0256D, V_{Sub} for all other D Series devices)

entire 13 μm (dimension b) produces photocurrent which divides between the two diffusions, with most of the charge going to the pixel near the site of the photon absorption.

In addition, D Series Linear devices contain an antiblooming gate which can be used to either suppress blooming or to set the integration period independent of the line rate. That allows these devices to be used over the widest possible range of lighting conditions.

Light incident on the sensing aperture generates a photocurrent which is integrated and stored as a charge on the capacitance of each of the photodiodes. If the charge accumulated on any diode exceeds a saturation value, the excess is shunted to V_{AB} through the antiblooming gates, controlled by V_{LR}, to control blooming effects. Refer to Figure 2.

The antiblooming gate is biased at a DC potential which is below that of the junction barrier and transfer gate $\varnothing_T$ "low" barrier. When the signal charge reaches the level set by the antiblooming gate, the excess will be sunk into V_{AB}, thus preventing blooming.

At the end of each integration period, the charges on all the diodes are simultaneously switched through transfer gates, $\varnothing_T$, into one of two CCD analog shift registers for readout. The odd numbered diodes are switched into one register and the even diodes into the other. Immediately after this parallel transfer, a new integration period begins.

Readout is accomplished by clocking the CCD shift registers so that the charge packets are delivered sequentially into two on-chip charge-detection circuits. The registers deliver the
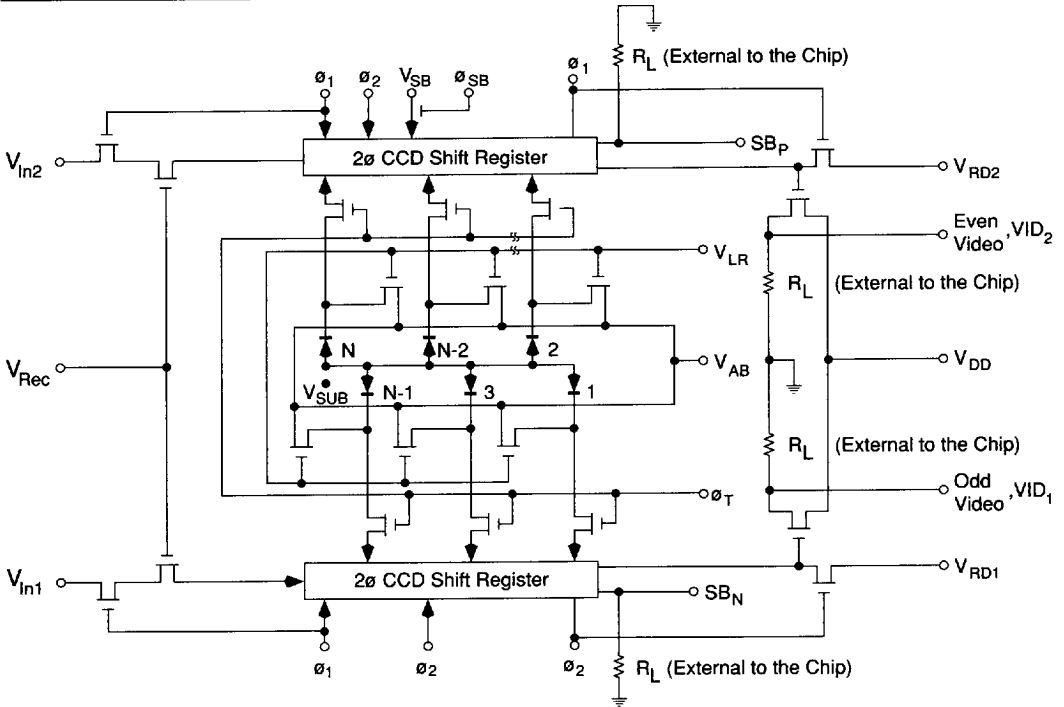
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Figure 2. Schematic of D Series Linear Devices
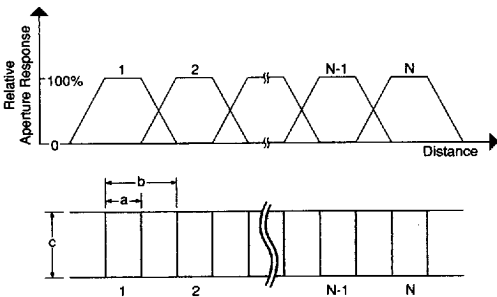

Figure 3. Sensor Geometry and Idealized Aperture

charge packets to their outputs on alternate clock phases, allowing the inactive charge detector to be reset to a fixed level, V_{RD}, while the opposite detector is active. The outputs of the two detectors may then be multiplexed off-chip if a single continuous video output is desired. Each video signal is developed across a 2-5KΩ resistor load, R_L.

Operation

D Series devices require two complimentary shift register clocks, $ø_1$ and $ø_2$, a transfer gate pulse, $ø_T$, for normal operation. An additional transfer pulse, $ø_{SB}$, is required if a scan buffer output is desired. The clocks and their timing relationships are shown in Figure 4. The video output and scan buffer output, $SB_P + SB_N$, are also shown in Figure 4.

The scan buffer output provides two marker bits; the first pulse coincides with the first video element, and the second with the last video element. The scan buffer output is obtained by differencing SB_P and SB_N through a differential amplifier. The circuit shown in Figure 6 will provide the required interface between the device's scan buffer output and its peripheral TTL circuit. Use of the scan buffer at higher speeds, greater than 10 MHz, is not recommended. It may be defeated by applying 0V to $ø_{SB}$.

The transfer pulse should swing between -3 and +5V and must have a width greater than 0.2 µsec. In order to transfer the charge from the photodiodes into the CCD register, the $ø_1$ clock must remain high during the blanking and transfer interval (see Figure 4). The odd and even video outputs are also shown in Figure 4. The odd and even output reset clocks, $ø_{RO}$ and $ø_{RE}$, are derived from the same sources as $ø_1$ and $ø_2$ and are nominally synchronous with them. Figure 10 shows the schematic of a typical voltage drive circuit for the D Series.

Antiblooming and line reset operation may be accomplished by applying a small positive voltage to the antiblooming gate, V_{LR}. The actual bias values vary from device to device.
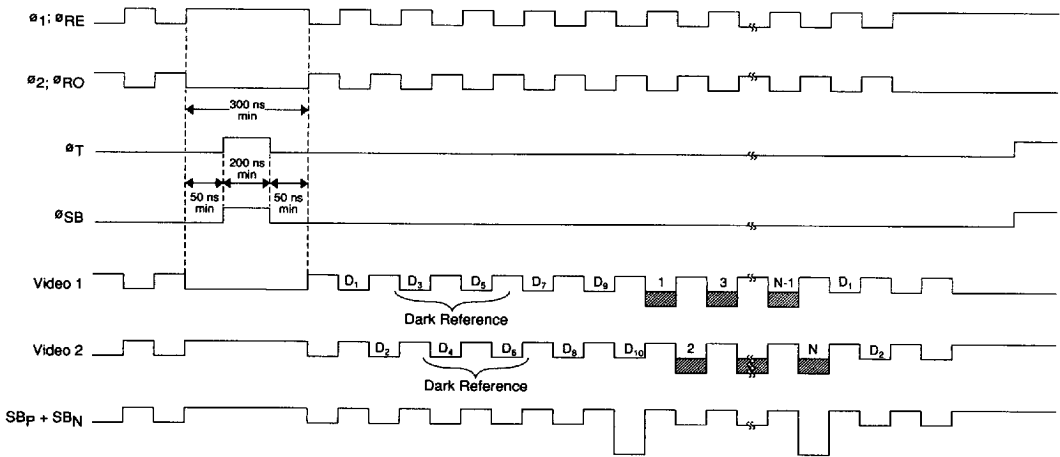
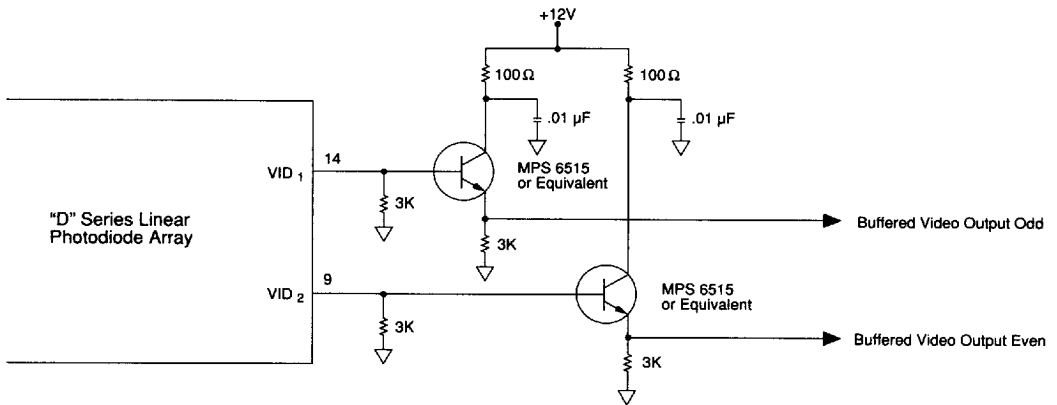**Figure 4. Timing Relationship of the Array's Clock Signals and Output**
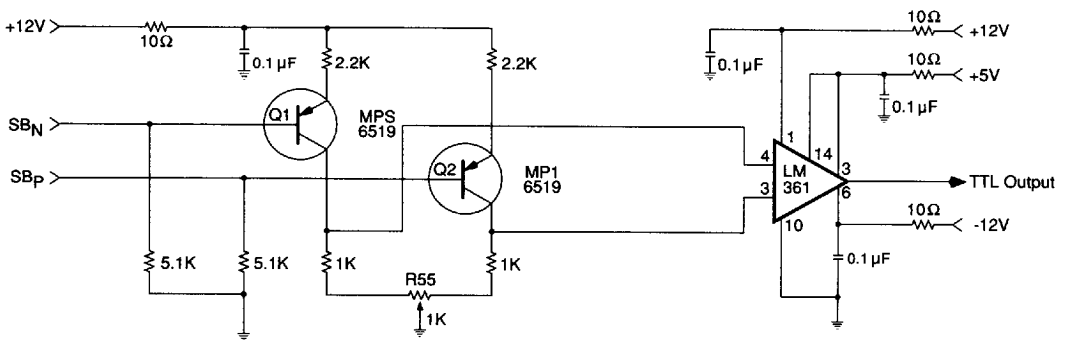

Figure 5. Recommended Output Circuit

Figure 6. Recommended Buffer Output Circuit

Antiblooming requires a DC bias of typically 1 - 3V. Line reset requires V_{LR} to be clocked to typically 2.5 - 4.5V for approximately 1 μs. Using the line reset may significantly increase nonuniformity.

Figure 9 shows typical video output waveforms as measured across a 3KΩ load resistor. Relative timing is indicated in relation to ø$_1$ and ø$_2$ clocks. The rise and fall times indicated are relative since they are affected by capacitive loading, including oscilloscope probe capacitance.

The high speed amplifier output circuit such as shown in Figure 5 is not required but is recommended to reduce the loading effects of external circuit capacitance. This will result in video rise and fall times of 50 ns or less.

Performance

Spectral response of the D Series devices covers the range from UV to the near IR. A ground and polished glass window is provided on the STANDARD-D, VLAUE-D, and FAST-D devices. A quartz window is provided on LOLIGHT-D devices. Relative spectral response is shown as a function of wavelength in Figure 7.

Since most applications for these devices (OCR, machine vision, etc.) use visible light, the responsivity and uniformity of response are specified using a light source with the spectral distribution shown by the dotted line in Figure 7. This spectral distribution is produced by filtering a 2870°K tungsten source with a Fish-Schurman HA-11 heat absorbing 1 mm thick filter.

Transfer characteristics showing the noise level and saturation output voltage can be seen in Figure 8. Since Reticon line scanners operate in the charge-storage mode, the charge output of each diode (below saturation) is proportional to exposure; i.e., the irradiance or light intensity multiplied by the integration time or the time interval between successive transfer pulses. Thus, there is a trade-off between scanning speed and required light intensity. Light intensity in watts needed to saturate a pixel at a particular integration time can be obtained by dividing saturation exposure by integration time. Thus, that longer integration times may be used to detect lower light levels. However, this approach is ultimately limited by dark leakage current which is integrated along with the photocurrent. At room temperature, dark current will typically contribute less than 0.1% of a saturated signal for integration times of 5 msec.

Drive Circuit

The circuit shown in Figure 10 will interface the TTL level control circuit to D Series CCPD devices. It will ensure that the ø$_1$ and ø$_2$ clock transitions cross at or above the midpoint; i.e., 50% clock crossing or higher. The supply voltages to the ø$_1$ and ø$_2$ clock drivers, devices 3 and 4, are as follows: V_{SS} = 0V or ground and V_{DD} = +12V.

The clock drivers, devices 1A and 2A, will provide voltage swings consistent with those given in the specification table. The supply voltages to device 1A are V_{DD} = +5V, pin 6, and V_{SS} = -4V. The supply voltages to device 2A are V_{DD} = +12V, pin 6, and V_{SS} = +5V. (Note: Both supply pins are positive to keep the minimum swing to +5V.)
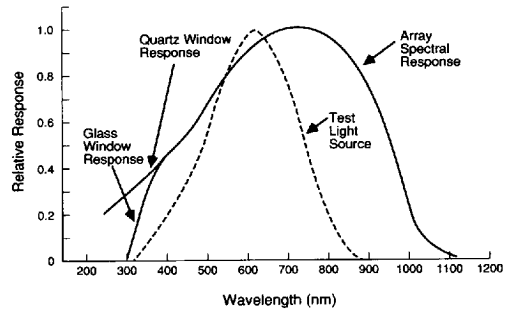

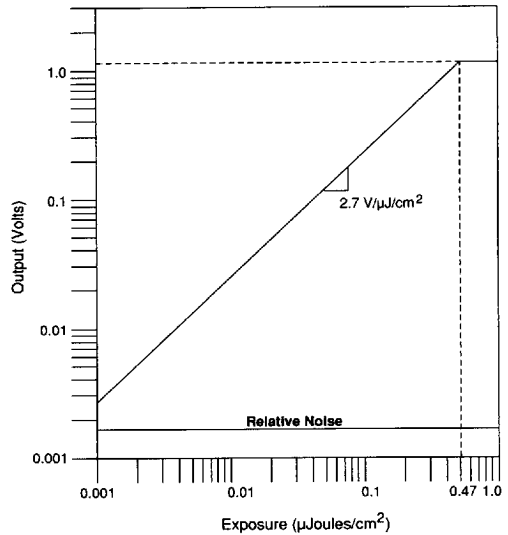**Figure 7. Relative Spectral Response as a Function of Wavelength**

Figure 8. Typical Transfer Characteristics

Evaluation Board

A complete evaluation circuit board (RC0730LNN) is available for the D Series and is recommended for first-time evaluation. The board contains all required logic and drive circuitry and has buffered outputs capable of operating data rates up to 20 MHz.
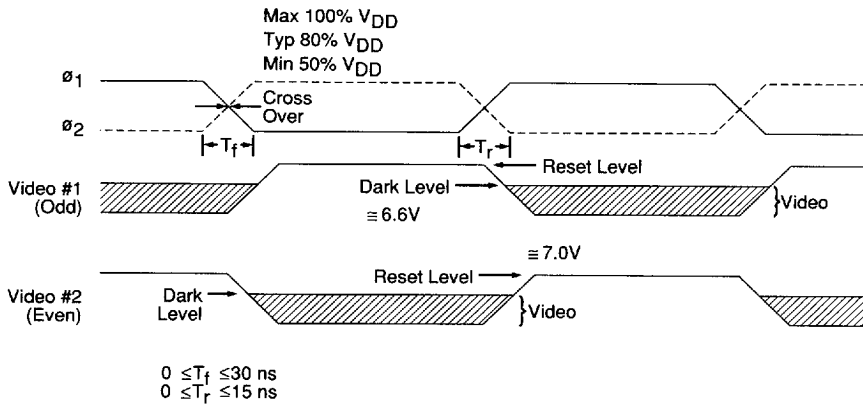
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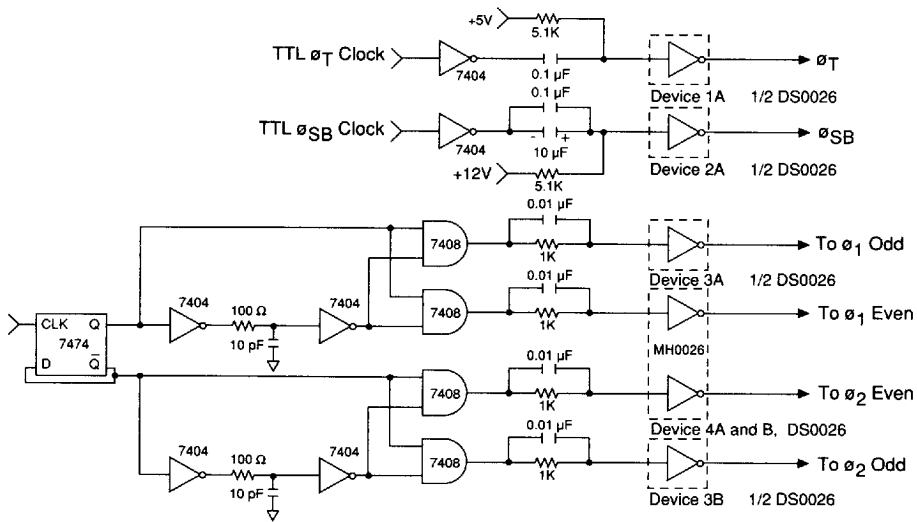
Figure 9. Clock Crossing and Video Output Relationship

Figure 10. Drive Circuit for D Series Linear Devices

Table 1. Array Bias and Clock Level Requirements

Symbol	Parameter	Min	Typ	Max	Units
V_{RD}	Reset drain bias	+11	+12	+13	V
V_{DD}	Output drain bias	+11	+12	+13	V
V_{IN}	Input bias	+11	+12	+13	V
V_{AB}	Antiblooming drain	+11	+12	+13	V
V_{LR}	Antiblooming gate				
	Disabled	-1	0	+1	V
	Antiblooming active	+1	+1.7	+2.5	V
	Line reset active	+2.5	+3.5	+4.5	V
V_{Sub}	Substrate bias	-6	-5	-4	V
ϕ_1, ϕ_2	CCD transport clock				
	High	+11	+12	+13	V
	Low	-1	0	+1	V
ϕ_T	Transfer clock				
	High	+4	+5	+6	V
	Low	-4	-3	-2	V
ϕ_{SB}	Transfer clock scan buffer				
	High	+11	+12	+13	V
	Low	+4	+5	+6	V
V_{REC}	Receiving gate	-1	0	+1	V
V_{SB}	DC input scanning	+11	+12	+13	V

"Min and Max values shown represent the allowable tolerance to maintain normal operation and are not absolute min and max values".

Table 2. Absolute Maximum Ratings
(Above Which Useful Life May Be Impaired)

Storage temperature	-25°C to 85°C
Operating temperature	-25°C to 55°C
Voltage on any pin with respect to substrate	-0.3V to 22V

Table 3. Linear D Series Array Capacitance Values [1]

		Typical Capacitance (pF)			
Pin No.	Symbol	RL2048D	RL1024D	RL0512D	RL0256D
1, 20	ϕ_2	280	135	80	40
3, 18	ϕ_1	280	135	80	40
4	ϕ_{SB}	25	13	8	6
7, 16	SB_P, SB_N	5	4	4	3
9, 14	VID_2, VID_1	5	4	4	3
10	V_{LR}	14	14	14	14
22	ϕ_T	65	31	18	12

Notes:

[1] Measured with respect to device substrate (pin 6) with a DC bias voltage of +12V

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Table 4. Array Performance Characteristics

Conditions: (unless otherwise specified)
$T_a = 25°C$, $f_{data} = 400$ KHz, $t_{int} = 10$ ms, R_L (at video output) = 3KΩ, $V_{LR} = 2V$, Light Source = 2870°K + Fish Schurman HA-11, 1 mm filter. All other operating voltages are nominal, as specified in Array Electrical Characteristics
First and last pixels of each video output are ignored

Symbol	Parameter	Min	Typ	Max	Units
DR_{P-P}	Dynamic range [1]				
	Standard-D, LoLight-D		2600:1	-	-
	Value-D, Fast-D		2000:1	-	-
DR_{rms}	Dynamic range [1]				
	Standard-D, LoLight-D	-	13000:1	-	-
	Value-D, Fast-D	-	10000:1	-	-
E_{NE}	P-to-P noise equivalent exposure	-	.18	-	nj/cm^2
	LoLight-D		.09		nj/cm^2
E_{SAT}	Saturation exposure	.30	.47	.63	μj/cm^2
	LoLight-D	.15	.24	.32	μj/cm^2
R	Responsivity	2.0	2.7	3.3	V/μj/cm^2
	LoLight-D	4.0	5.4	6.6	V/μj/cm^2
PRNU	Photoresponse nonuniformity [4, 6]				
0256	[2]	-	3	8	±%
0512	[2]	-	3	8	±%
1024	[2]	-	3	10	±%
2048	[2]	-	5	12	±%
V_{da}	Average dark signal [3,8]	-	.03	.25	%
V_{dm}	Maximum dark signal [4,8]	-	.06	.5	%
V_{SAT}	Saturation output voltage	0.8	1.3	1.6	V
P	DC Power dissipation [5]	-	126	-	mW
N_{P-P}	Peak-to-peak noise	-	0.5	-	mV
V_{DCR}	Output DC reset level [5]	-	7.0	-	V
V_{DCD}	Output DC dark level [5]	-	6.7	-	V
Z_{out}	Output impedance [6]	-	2	-	kΩ
V_{bal}	Video output balance [9]	-	30	80	mV
	Output DC drift [10]	-	10	-	mV/°C
f_{data}	Maximum guaranteed video data rate [7]				
	Value-D	10	-	-	MHz
	Standard and Lolight-D	20	-	-	MHz
	Fast-D	30	-	-	MHz

Notes:

[1] Dynamic range is defined as V_{SAT}/N_{P-P}, RMS noise is approximately $N_{P-P}/5$
[2] Measured at an exposure level of approximately $V_{SAT}/2$. PRNU is defined as $100*[(V_{max}-V_{min})/V_{avg}]$ where V_{max} is output of highest pixel (toward V_{sat}). V_{min} is output of lowest pixel (towards dark) and V_{avg} is the numerical average of all the pixels in the video line
[3] Measured at ambient temperatures Ta = 25°C, t_{int} = 2.5 ms. Defined as $100*(V_a/V_{sat})$ where V_a is the numerical average of the output of all pixels in dark and V_{sat} is the numerical average of all pixels in saturation.
[4] Measured at ambient temperature T_a = 25°C, t_{int} = 2.5 ms. Defined as $100*(V_m/V_{sat})$ where V_m is the pixel with the maximum output of all pixels in dark and V_{sat} is the numerical average of all of pixels in saturation
[5] Measured with device in the dark
[6] Measured with output current of 2 mA
[7] f_{data} is defined as 2 times f_{clock} where f_{clock} is the frequency of the ø$_1$ or ø$_2$ clock. The minimum frequency is limited by increases in dark signal.
[8] Dark signal approximately doubles for each 7-10°C increase in temperature
[9] Defined as the difference in DC dark level output (D_{dc}) between the two video outputs
[10] Defined as the thermal drift in the reset level (R_{dc})

Figure 11. Package Dimensions
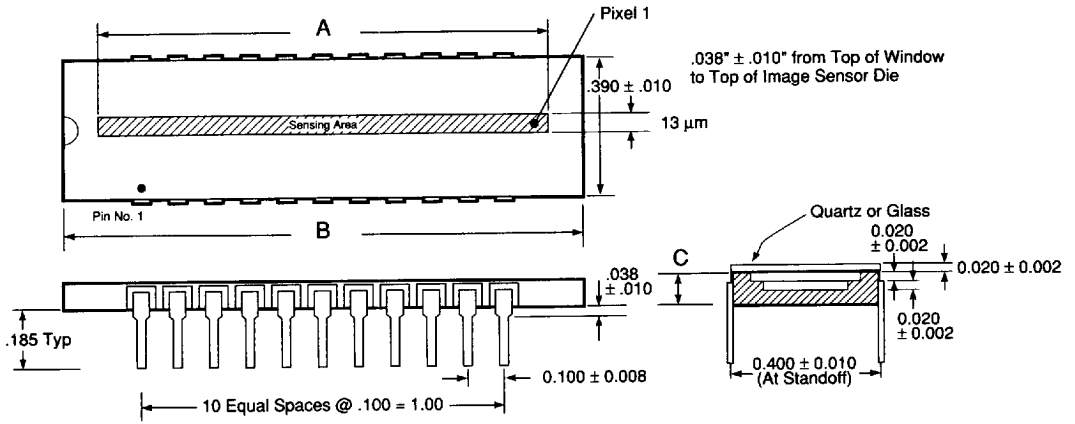
| | A | | B | C |
Device	inches	mm	inches	inches
RL0256D	.131	3.328	1.080 ±0.011	0.090 ±0.009
RL0512D	.262	6.656	1.080 ±0.011	0.080 ±0.008
RL1024D	.524	13.312	1.080 ±0.011	0.080 ±0.008
RL2048D	1.048	26.624	1.600 ±0.016	0.080 ±0.008

Ordering Information

Standard-D	Value-D	Fast-D	LoLight-D	Evaluation Board
RL0256DAG-011	RL0256DAG-020	RL0256DAG-021	RL0256DKQ-011	RC0730LNN-011
RL0512DAG-011	RL0512DAG-020	RL0512DAG-021	RL0512DKQ-011	RC0730LNN-011
RL1024DAG-011	RL1024DAG-020	RL1024DAG-021	RL1024DKQ-011	RC0730LNN-011
RL2048DAG-011	RL2048DAG-020	N/A	RL2048DKQ-011	RC0730LNN-011

The quartz window supplied standard on LoLight-D devices is available as an option for all D Series devices. For options, consult EG&G Reticon.

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