Voltage Output
PROGRAMMABLE SENSOR CONDITIONER

FEATURES

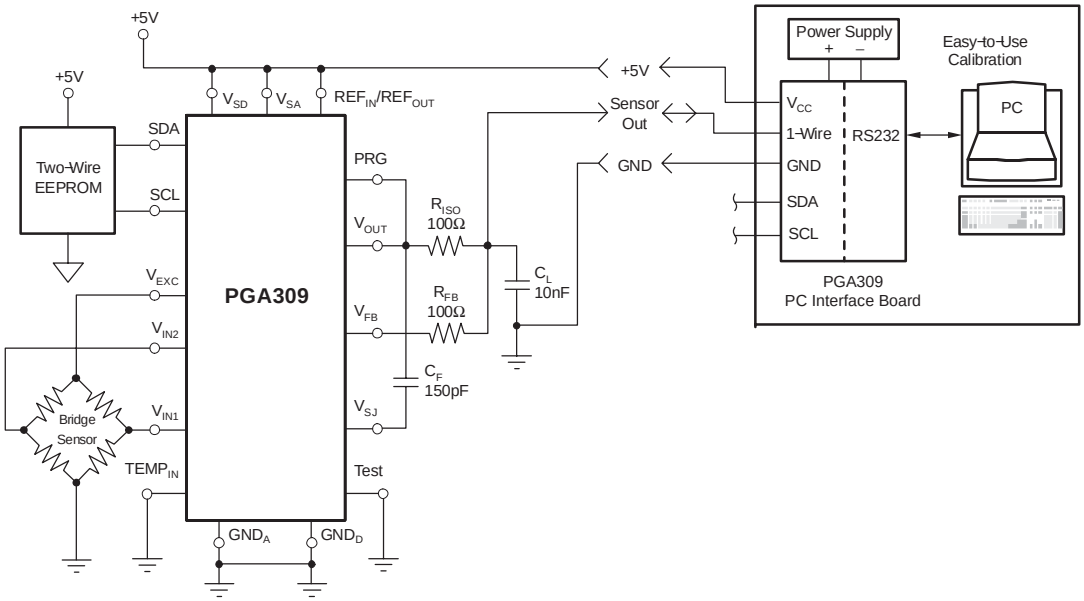
- COMPLETE BRIDGE SENSOR CONDITIONER
- VOLTAGE OUTPUT
  - Ratiometric or Absolute
- DIGITALLY CALIBRATED
  - One-Wire and Two-Wire Digital Interface
- SENSOR ERROR COMPENSATION
  - Span
  - Offset
  - Temperature Drift of Span and Offset
- ELIMINATES POTENTIOMETERS
- ELIMINATES SENSOR TRIMS
- LOW, TIME-STABLE, TOTAL ADJUSTED ERROR
- SENSOR LINEARIZATION CIRCUITRY
- TEMPERATURE SENSE SELECT
  - Internal/External
- CALIBRATION TABLE LOOKUP LOGIC
  - Includes Linear Interpolation Algorithm
- NONVOLATILE CALIBRATION CONSTANTS
  - External 1K EEPROM (SOT23-5)
- SMALL TSSOP-16 PACKAGE
- −40°C to +125°C OPERATION
- +2.7V TO +5.5V OPERATION

APPLICATIONS

- PRESSURE BRIDGE CONDITIONERS
  - With Digital Calibration
- SENSORS
- REMOTE 4-20mA TRANSMITTERS
- WEIGH SCALE BRIDGE TRANSMITTERS
- SCADA REMOTE DATA ACQUISITION
- INDUSTRIAL PROCESS CONTROL
- AUTOMOTIVE SENSORS

EVALUATION TOOLS

- HARDWARE DESIGNER'S KIT (PGA309DK)
  - Evaluate PGA309 and Sensor
  - Full Temperature Evaluation
- SOFTWARE CONTROL FOR DESIGNER'S KIT
  - Program PGA309 for Evaluation
  - Program PGA309 for First Production Run
  - Sensor Computation Analysis Tool



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PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE−LEAD	PACKAGE DRAWING	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
PGA309	TSSOP-16	PW	−40°C to +125°C	PGA309	PGA309AIPWR	Tape and Reel, 2500
					PGA309AIPWT	Tape and Reel, 250

(1) For the most current package and ordering information, refer to our web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range unless otherwise noted.

Supply Voltage, V_{SD}, V_{SD}	+7.0V
Input Voltage, V_{IN1}, V_{IN2}(2)	−0.3V to V_{SA} +0.3V
Input Current, V_{FB}, V_{OUT}	±150mA
Input Current	±10mA
Output Current Limit	50mA
Storage Temperature Range	−60°C to +150°C
Operating Temperature Range	−55°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
ESD Protection (Human Body Model)	4kV

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION

The PGA309 is a programmable analog signal conditioner designed for pressure bridge sensors. The analog signal path amplifies the sensor signal and provides digital calibration for zero, span, zero drift, span drift, and linearization errors. The calibration is done via a One-Wire digital serial interface or through a Two-Wire compatible connection. The calibration parameters are stored in external nonvolatile memory, to eliminate manual trimming and achieve long time stability.

The all-analog signal path contains a 2X2 input mux, auto-zeroed programmable-gain instrumentation amplifier, linearization circuit, voltage reference, internal oscillator, control logic, and an output amplifier. Programmable level shifting compensates for sensor DC offsets. Automatic reset is initiated when supply is lost.

The core of the PGA309 is the precision low-drift and low-noise front-end programmable gain amplifier (PGA). The overall gain of the PGA + output amplifier can be adjusted from +2.7V/V to +1152V/V. The polarity of the inputs can be switched through the Input multiplexer (mux) to accommodate sensors with unknown polarity output. The fault monitor circuit detects and signals sensor burnout, overload, and system fault conditions.

ELECTRICAL CHARACTERISTICS

BOLDFACE limits apply over the specified temperature range: **T_A = −40°C to +125°C**

T_A = +25°C, V_{SA} = V_{SD} = +5V (V_{SA} = $V_{SUPPLY\ ANALOG}$, V_{SD} = $V_{SUPPLY\ DIGITAL}$; V_{SA} must equal V_{SD}), GND_D = GND_A = 0, and V_{REF} = REF_{IN}/REF_{OUT} = +5V, unless otherwise noted.

PARAMETER	CONDITIONS	PGA309 MIN	PGA309 TYP	PGA309 MAX	UNITS
FRONT-END PGA + OUTPUT AMPLIFIER					
V_{OUT}/V_{IN} Differential Signal Gain Range(1)	Fine Gain Adjust = 1 Front-End PGA Gains: 4, 8, 16, 23, 27, 32, 42.67, 64, 128 Output Amplifier Gains: 2, 2.4, 3, 3.6, 4.5, 6, 9		8 to 1152		V/V
V_{OUT} Slew Rate			0.5		V/µs
V_{OUT} Settling Time (0.01%)	V_{OUT}/V_{IN} Differential Gain = 8, R_L = 5kΩ || 200pF		6		µs
V_{OUT} Settling Time (0.01%)	V_{OUT}/V_{IN} Differential Gain = 191, R_L = 5kΩ || 200pF		4.1		µs
V_{OUT} Nonlinearity			0.002		%FSR
External Sensor Output Sensitivity	V_{SA} = V_{SD} = V_{EXC} = +5V		1 to 245		mV/V
FRONT-END PGA					
Auto−Zero Internal Frequency			7		kHz
Offset Voltage (RTI)(2)	Coarse Offset Adjust Disabled		±3	±50	µV
vs Temperature			**±0.2**		**µV/°C**
vs Supply Voltage, V_{SA}			±2		µV/V
vs Common-Mode Voltage	G_F = Front-End PGA Gain		1500/G_F	6000/G_F	µV/V
Linear Input Voltage Range(3)		**0.2**		**V_{SA}−1.5**	**V**
Input Bias Current			0.1	1.5	nA
Input Impedance: Differential			30 || 6		GΩ || pF
Input Impedance: Common-Mode			50 || 20		GΩ || pF
Input Voltage Noise	0.1Hz to 10Hz, G_F = 128		4		$µV_{PP}$
PGA Gain(1)					
Gain Range Steps	4, 8, 16, 23.27, 32, 42.67, 64, 128		4 to 128		V/V
Initial Gain Error	G_F = 4 to 42		0.2	±1	%
	G_F = 64		0.25	±1.2	%
	G_F = 128		0.3	±1.6	%
vs Temperature			**10**		**ppm/°C**
Output Voltage Range			**0.05 to V_{SA} − 0.1**		**V**
Bandwidth	Gain = 4		400		kHz
	Gain = 128		15.5		kHz
COARSE OFFSET ADJUST (RTI OF FRONT-END PGA)					
Range	±(15)(V_{REF}/1250)	±56	±59.5	±64	mV
vs Temperature			**0.004**		**%/°C**
Resolution	±15 steps, 4-Bit + Sign		4		mV
FINE OFFSET ADJUST (ZERO DAC) (RTO of the Front-End PGA)(2)					
Programming Range		0		V_{REF}	V
Output Range		0.1		V_{SA}−0.1	V
Resolution	65,536 steps, 16-Bit DAC		73		µV
Integral Nonlinearity			20		LSB
Differential Nonlinearity			0.5		LSB
Gain Error			0.1		%
Gain Error Drift			10		ppm/°C
Offset			5		mV
Offset Drift			10		µV/°C
OUTPUT FINE GAIN ADJUST (GAIN DAC)					
Range			0.33 to 1		V/V
Resolution	65,536 steps, 16-Bit DAC		10		µV/V
Integral NonLinearity			20		LSB
Differential NonLinearity			0.5		LSB

ELECTRICAL CHARACTERISTICS (continued)

BOLDFACE limits apply over the specified temperature range: **T_A = −40°C to +125°C**

T_A = +25°C, V_{SA} = V_{SD} = +5V (V_{SA} = $V_{SUPPLY\ ANALOG}$, V_{SD} = $V_{SUPPLY\ DIGITAL}$; V_{SA} must equal V_{SD}), GND_D = GND_A = 0, and V_{REF} = REF_{IN}/REF_{OUT} = +5V, unless otherwise noted.

PARAMETER	CONDITIONS	PGA309 MIN	PGA309 TYP	PGA309 MAX	UNITS
OUTPUT AMPLIFIER					
Offset Voltage (RTI of Output Amplifier)(2)			3		mV
vs Temperature			**5**		**µV/°C**
vs Supply Voltage, V_{SA}			30		µV/V
Common-Mode Input Range		**0**		**V_{SA}−1.5**	**V**
Input Bias Current			100		pA
Amplifier Internal Gain					
Gain Range Steps	2, 2.4, 3, 3.6, 4.5, 6, 9		2 to 9		V/V
Initial Gain Error	2, 2.4, 3.6		0.25	±1	**%**
	4.5		0.3	±1.2	**%**
	6		0.4	±1.5	**%**
	9		0.6	±2.0	**%**
vs Temperature	**2, 2.4, 3.6**		**5**		**ppm/°C**
	4.5		**5**		**ppm/°C**
	6		**15**		**ppm/°C**
	9		**30**		**ppm/°C**
Output Voltage Range(4)	**R_L = 10kΩ**	**0.1**		**4.9**	**V**
OpenLoop Gain			115		dB
Gain-Bandwidth Product			2		MHz
Phase Margin	Gain = 1		45		Degrees
Output Resistance	AC Small-Signal, Open-Loop, f = 1MHz		675		Ω
OVER- AND UNDER-SCALE LIMITS	(V_{REF} = 4.096)				
Over-Scale Thresholds	Ratio of V_{REF}, Register 5—Bits D5, D4, D3 = '000'		0.9708		
	Ratio of V_{REF}, Register 5—Bits D5, D4, D3 = '001'		0.9610		
	Ratio of V_{REF}, Register 5—Bits D5, D4, D3 = '010'		0.9394		
	Ratio of V_{REF}, Register 5—Bits D5, D4, D3 = '011'		0.9160		
	Ratio of V_{REF}, Register 5—Bits D5, D4, D3 = '100'		0.9102		
	Ratio of V_{REF}, Register 5—Bits D5, D4, D3 = '101'		0.7324		
	Ratio of V_{REF}, Register 5—Bits D5, D4, D3 = '110'		0.5528		
Over-Scale Comparator Offset		+6	+60	+114	mV
Over-Scale Comparator Offset Drift			+0.37		mV/°C
Under-Scale Thresholds	Ratio of V_{REF}, Register 5—Bits D2, D1, D0 = '111'		0.0605		
	Ratio of V_{REF}, Register 5—Bits D2, D1, D0 = '110'		0.0547		
	Ratio of V_{REF}, Register 5—Bits D2, D1, D0 = '101'		0.0507		
	Ratio of V_{REF}, Register 5—Bits D2, D1, D0 = '100'		0.0449		
	Ratio of V_{REF}, Register 5—Bits D2, D1, D0 = '011'		0.0391		
	Ratio of V_{REF}, Register 5—Bits D2, D1, D0 = '010'		0.0352		
	Ratio of V_{REF}, Register 5—Bits D2, D1, D0 = '001'		0.0293		
	Ratio of V_{REF}, Register 5—Bits D2, D1, D0 = '000'		0.0254		
Under-Scale Comparator Offset		−7	−50	+93	mV
Under-Scale Comparator Offset Drift			−0.15		mV/°C
FAULT MONITOR CIRCUIT					
INP_HI, INN_HI Comparator Threshold	See Note 5		V_{SA}−1.2 or V_{EXC}−100		V
INP_LO, INN_LO Comparator Threshold		40	100		mV
A1SAT_HI, A2SAT_HI Comparator Threshold			V_{SA}−0.12		V
A1SAT_LO, A2SAT_LO Comparator Threshold			V_{SA}−0.12		V
A3_VCM Comparator Threshold			V_{SA}−1.2		V
Comparator Hysteresis			20		mV

ELECTRICAL CHARACTERISTICS (continued)

BOLDFACE limits apply over the specified temperature range: **T_A = −40°C to +125°C**

T_A = +25°C, V_{SA} = V_{SD} = +5V (V_{SA} = $V_{SUPPLY\ ANALOG}$, V_{SD} = $V_{SUPPLY\ DIGITAL}$; V_{SA} must equal V_{SD}), GND_D = GND_A = 0, and V_{REF} = REF_{IN}/REF_{OUT} = +5V, unless otherwise noted.

PARAMETER	CONDITIONS	PGA309 MIN	PGA309 TYP	PGA309 MAX	UNITS
INTERNAL VOLTAGE REFERENCE					
V_{REF1}	Register 3, Bit D9 = 1	2.46	2.5	2.53	V
V_{REF1} Drift vs Temperature			**+10**		**ppm/°C**
V_{REF2}	Register 3, Bit D9 = 0	4.0	4.096	4.14	V
V_{REF2} Drift vs Temperature			**+10**		**ppm/°C**
Input Current REF_{IN}/REF_{OUT}	Internal V_{REF} Disabled		100		µA
Output Current REF_{IN}/REF_{OUT}	V_{SA} > 2.7V for V_{REF} = 2.5V		1		mA
	V_{SA} > 4.3V for V_{REF} = 4.096V		1		mA
TEMPERATURE SENSE CIRCUITRY (ADC)					
Internal Temperature Measurement	Register 6, Bit D9 = 1				
Accuracy			±2		°C
Resolution	12-Bit + Sign, Two's Complement Data Format		±0.0625		°C
Temperature Measurement Range		−55		+150	°C
Conversion Rate	R_1, R_0 = '11', 12-Bit + Sign Resolution		24		ms
TEMPERATURE ADC					
External Temperature Mode	Temp PGA + Temp ADC				
Gain Range Steps	G_{PGA} = 1, 2, 4, 8		1 to 8		V/V
Analog Input Voltage Range		GND−0.2		V_{SA}+0.2	V
Temperature ADC Internal REF (2.048V)	Register 6, Bit D8 = 1				
Full-Scale Input Voltage	(+Input) − (−Input)		±2.048/G_{PGA}		V
Differential Input Impedance			2.8/G_{PGA}		MΩ
Common-Mode Input Impedance	G_{PGA} = 1		3.5		MΩ
	G_{PGA} = 2		3.5		MΩ
	G_{PGA} = 4		1.8		MΩ
	G_{PGA} = 8		0.9		MΩ
Resolution	R1, R0 = '00', ADC2X = '0', Conversion Time = 8ms		11		Bits + Sign
	R1, R0 = '01', ADC2X = '0', Conversion Time = 32ms		13		Bits + Sign
	R1, R0 = '10', ADC2X = '0', Conversion Time = 64ms		14		Bits + Sign
	R1, R0 = '11', ADC2X = '0', Conversion Time = 128ms		15		Bits + Sign
Integral Nonlinearity			0.004		%
Offset Error	G_{PGA} = 1		1.2		mV
	G_{PGA} = 2		0.7		mV
	G_{PGA} = 4		0.5		mV
	G_{PGA} = 8		0.4		mV
Offset Drift	G_{PGA} = 1		1.2		µV/°C
	G_{PGA} = 2		0.6		µV/°C
	G_{PGA} = 4		0.3		µV/°C
	G_{PGA} = 8		0.3		µV/°C
Offset vs V_{SA}	G_{PGA} = 1		800		µV/V
	G_{PGA} = 2		400		µV/V
	G_{PGA} = 4		200		µV/V
	G_{PGA} = 8		150		µV/V
Gain Error			0.05	0.50	%
Gain Error Drift			5	50	ppm/°C
Gain vs V_{SA}			80		ppm/V
Common-Mode Rejection	At DC and G_{PGA} = 8		105		dB
	At DC and G_{PGA} = 1		100		dB

ELECTRICAL CHARACTERISTICS (continued)

BOLDFACE limits apply over the specified temperature range: **T_A = −40°C to +125°C**

T_A = +25°C, V_{SA} = V_{SD} = +5V (V_{SA} = $V_{SUPPLY\ ANALOG}$, V_{SD} = $V_{SUPPLY\ DIGITAL}$; V_{SA} must equal V_{SD}), GND_D = GND_A = 0, and V_{REF} = REF_{IN}/REF_{OUT} = +5V, unless otherwise noted.

PARAMETER	CONDITIONS	PGA309 MIN	PGA309 TYP	PGA309 MAX	UNITS
TEMPERATURE ADC (CONTINUED)					
Temp ADC Ext. REF (V_{REFT} = V_{REF}, V_{EXC}, or V_{SA})	Register 6, Bit D8 = 0				
Full-Scale Input Voltage	(+Input) − (−Input)		$\pm V_{REFT}/G_{PGA}$		V
Differential Input Impedance			$2.4/G_{PGA}$		MΩ
Common-Mode Input Impedance	G_{PGA} = 1		8		MΩ
	G_{PGA} = 2		8		MΩ
	G_{PGA} = 4		8		MΩ
	G_{PGA} = 8		8		MΩ
Resolution	R1, R0 = '00', ADC2X = '0', Conversion Time = 6ms		11		Bits + Sign
	R1, R0 = '01', ADC2X = '0', Conversion Time = 24ms		13		Bits + Sign
	R1, R0 = '10', ADC2X = '0', Conversion Time = 50ms		14		Bits + Sign
	R1, R0 = '11', ADC2X = '0', Conversion Time = 100ms		15		Bits + Sign
Integral Nonlinearity			0.01		%
Offset Error	G_{PGA} = 1		2.5		mV
	G_{PGA} = 2		1.25		mV
	G_{PGA} = 4		0.7		mV
	G_{PGA} = 8		0.3		mV
Offset Drift	G_{PGA} = 1		1.5		µV/°C
	G_{PGA} = 2		1.0		µV/°C
	G_{PGA} = 4		0.7		µV/°C
	G_{PGA} = 8		0.6		µV/°C
Gain Error			−0.2		%
Gain Error Drift			2		ppm/°C
Gain vs V_{SA}			80		ppm/V
Common-Mode Rejection	At DC and G_{PGA} = 8		100		dB
	At DC and G_{PGA} = 1		85		dB
External Temperature Current Excitation I_{TEMP}	Register 6, Bit D11 = 1				
Current Excitation		5.8	7	8	µA
Temperature Drift			5		nA/°C
Voltage Compliance			V_{SA}−1.2		V
LINEARIZATION ADJUST AND EXCITATION VOLTAGE (V_{EXC})					
Range 1	Register 3, Bit D11 = 0				
Linearization DAC Range	With Respect to V_{FB}		−0.166 to +0.166		V/V
Linearization DAC Resolution	±128 Steps, 7-Bit + Sign		1.3		mV/V
V_{EXC} Gain	With Respect to V_{REF}		0.83		V/V
Gain Error Drift			25		ppm/°C
Range 2	Register 3, Bit D11 = 1				
Linearization DAC Range	With Respect to V_{FB}		−0.124 to +0.124		V/V
Linearization DAC Resolution	±128 Steps, 7-Bit + Sign		0.969		mV/V
V_{EXC} Gain	With Respect to V_{REF}		0.52		V/V
Gain Error Drift			25		ppm/°C
V_{EXC} Range Upper Limit	I_{EXC} = 5mA		V_{SA} − 0.5		V
$I_{EXC\ SHORT}$	Short-Circuit V_{EXC} Output Current		50		mA
DIGITAL INTERFACE					
Two-Wire Compatible	Bus Speed	1		400	kHz
One-Wire	Serial Speed Baud Rate	4.8K		38.4K	Bits/s
Maximum Lookup Table Size(6)			17 x 3 x 16		Bits
Two-Wire Data Rate	Communication Between PGA309 and EEPROM		65		kHz
LOGIC LEVELS					
Input Levels (SDA, SCL, PRG)	Low			$0.2 \bullet V_{SD}$	V
	High	$0.7 \bullet V_{SD}$			V
	Hysteresis		$0.1 \bullet V_{SD}$		V
Output LOW Level (SDA, SCL)	Open Drain w/90µA Internal Pull-Up to V_{SD}, I_{SINK} = 5mA			0.4	V
Output LOW Level (PRG)	Open Drain, I_{SINK} = 5mA			0.4	V

ELECTRICAL CHARACTERISTICS (continued)

BOLDFACE limits apply over the specified temperature range: **T_A = −40°C to +125°C**

T_A = +25°C, V_{SA} = V_{SD} = +5V (V_{SA} = $V_{SUPPLY\ ANALOG}$, V_{SD} = $V_{SUPPLY\ DIGITAL}$; V_{SA} must equal V_{SD}), GND_D = GND_A = 0, and V_{REF} = REF_{IN}/REF_{OUT} = +5V, unless otherwise noted.

PARAMETER	CONDITIONS	PGA309 MIN	PGA309 TYP	PGA309 MAX	UNITS
POWER SUPPLY					
V_{SA}, V_{SD}		2.7		5.5	V
I_{SA} + I_{SD}, Quiescent Current	V_{SA} = V_{SD} = +5V, without Bridge Load		1.2	1.6	mA
POWER-ON RESET					
Power-Up Threshold	**V_{SA} Rising**		**2.2**	**2.7**	**V**
Power-Down Threshold	V_{SA} Falling		1.7		V
TEMPERATURE RANGE					
Specified Performance		−40		+125	°C
Operational − Degraded Performance		−55		+150	°C

(1) PGA309 total differential gain from input (V_{IN1}−V_{IN2}) to output (V_{OUT}). V_{OUT} / (V_{IN1}−V_{IN2}) = (PGA front-end gain) (output amplifier gain) (fine gain adjust).

(2) RTI = referred to input. RTO = referred to output.

(3) Linear input range is the allowed min/max voltage on the V_{IN1} and V_{IN2} pins for the input PGA to continue to operate in a linear region. The allowed common-mode and differential voltage is dependent upon gain and offset settings. Refer to the Gain Scaling section for more information.

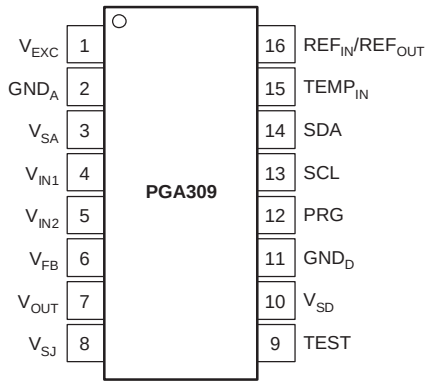
(4) Unless limited by over/under-scale setting.

(5) When V_{EXC} is enabled, a minimum reference selector circuit becomes the reference for the comparator threshold. This minimum reference selector circuit uses V_{EXC} − 100mV and V_{SA} − 1.2V and compares the V_{INX} pin to the lower of the two references. This ensures accurate fault monitoring in conditions where V_{EXC} might be higher or lower than the input CMR of the PGA input amplifier relative to V_{SA}.

(6) Lookup Table allows multislope compensation over temperature. Lookup Table has access to 17 calibration points consisting of 3 adjustment values (Tx, Temperature, ZMx, Zero DAC, GMx, Gain) that are stored in 16-bit data format (17x3x16 = Lookup Table size).

PIN CONFIGURATION

Top View **TSSOP**



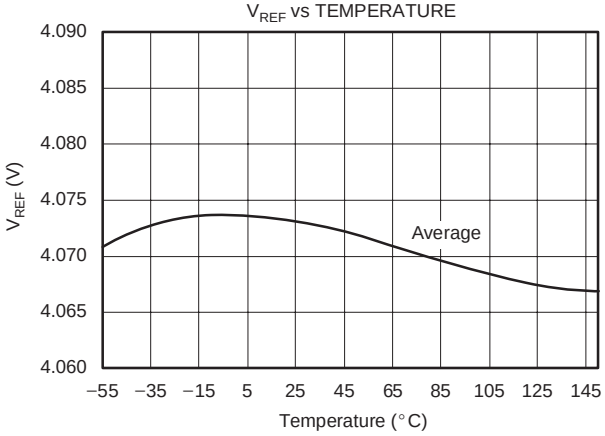
PIN DESCRIPTION

PIN	NAME	DESCRIPTION
1	V_{EXC}	Bridge sensor excitation. Connect to bridge if linearization and/or internal reference for bridge excitation is to be used.
2	GND_A	Analog ground. Connect to analog ground return path for V_{SA}. Should be same as GND_D.
3	V_{SA}	Analog voltage supply. Connect to analog voltage supply. To be within 200mV of V_{SD}.
4	V_{IN1}	Signal input voltage 1. Connect to + or – output of sensor bridge. Internal multiplexer can change connection internally to front-end PGA.
5	V_{IN2}	Signal input voltage 2. Connect to + or – output of sensor bridge. Internal multiplexer can change connection internally to front-end PGA.
6	V_{FB}	V_{OUT} feedback pin. Voltage feedback sense point for over/under-scale limit circuitry. When internal gain set resistors for the output amplifier are used, this is also the voltage feedback sense point for the output amplifier. V_{FB} in combination with V_{SJ} allows for ease of external filter and protection circuits without degrading the PGA309 V_{OUT} accuracy. V_{FB} must always be connected to either V_{OUT} or the point of feedback for V_{OUT}, if external protection is used.
7	V_{OUT}	Analog output voltage of conditioned sensor.
8	V_{SJ}	Output amplifier summing junction. Use for output amplifier compensation when driving large capacitive loads (> 100pF) and/or for using external gain setting resistors for the output amplifier.
9	TEST	Test/External Controller Mode pin. Pull to GND_D in normal mode.
10	V_{SD}	Digital voltage supply. Connect to digital voltage supply. To be within 200mV of V_{SA}.
11	GND_D	Digital ground. Connect to digital ground return path for V_{SD}. Should be same as GND_A.
12	PRG	Single-wire interface program pin. UART-type interface for digital calibration of the PGA309 over a single wire. Can be connected to V_{OUT} for a three-lead (V_S, GND, V_{OUT}) smart programmable sensor assembly.
13	SCL	Clock input/output for Two-Wire, industry-standard compatible interface for reading digital calibration and configuration from external EEPROM. Can also communicate directly to the registers in the PGA309 through the Two-Wire, industry-standard compatible interface.
14	SDA	Data input/output for Two-Wire, industry-standard compatible interface for reading digital calibration and configuration from external EEPROM. Can also communicate directly to the registers in the PGA309 through the Two-Wire, industry-standard compatible interface.
15	$TEMP_{IN}$	External temperature signal input. PGA309 can be configured to read a bridge current sense resistor as an indicator of bridge temperature, or an external temperature sensing device such as diode junction, or RTD, or thermistor. This input can be gained up internally by X1, X2, X4, or X8. In addition, this input can be read differentially with respect to V_{GNDA}, V_{EXC}, or the internal V_{REF}. There is also an internal, register-selectable, 7μA current source (I_{TEMP}) that can be connected to $TEMP_{IN}$ as an RTD, thermistor, or diode excitation source.
16	REF_{IN}/REF_{OUT}	Reference input/output pin. As an output, the internal reference (selectable as 2.5V or 4.096V) is available for system use on this pin. As an input, the internal reference may be disabled and an external reference can then be applied as the reference for the PGA309.

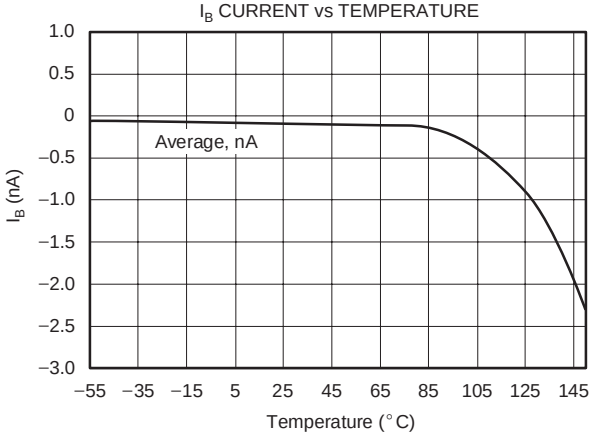
TYPICAL CHARACTERISTICS

T_A = +25°C, V_{SA} = V_{SD} = +5V (V_{SA} = $V_{SUPPLY\ ANALOG}$, V_{SD} = $V_{SUPPLY\ DIGITAL}$, V_{SA} must equal V_{SD}), GND_D = GND_A = 0, and V_{REF} = REF_{IN}/REF_{OUT} = +5V, unless otherwise noted.

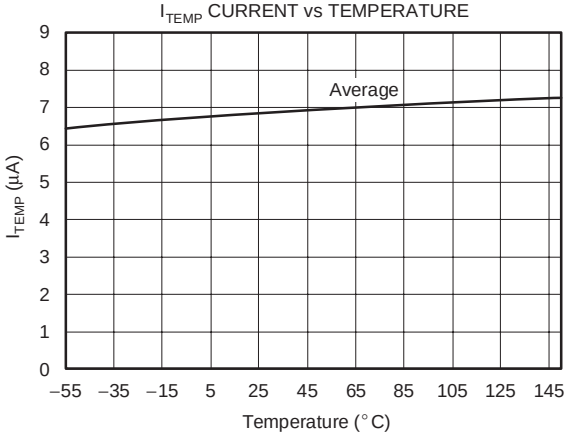
V_{REF} vs TEMPERATURE



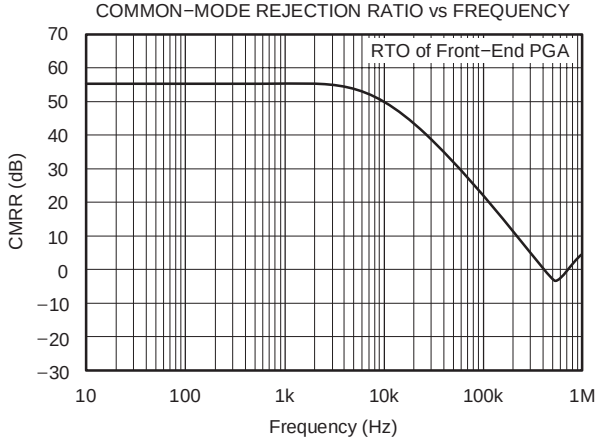
I_B CURRENT vs TEMPERATURE



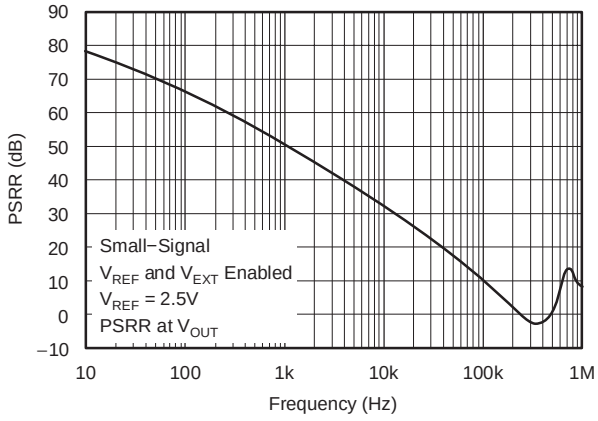
I_{TEMP} CURRENT vs TEMPERATURE



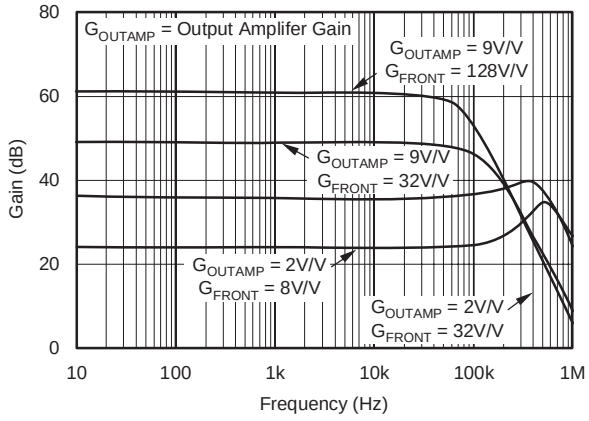
COMMON−MODE REJECTION RATIO vs FREQUENCY



POWER−SUPPLY REJECTION RATIO vs FREQUENCY



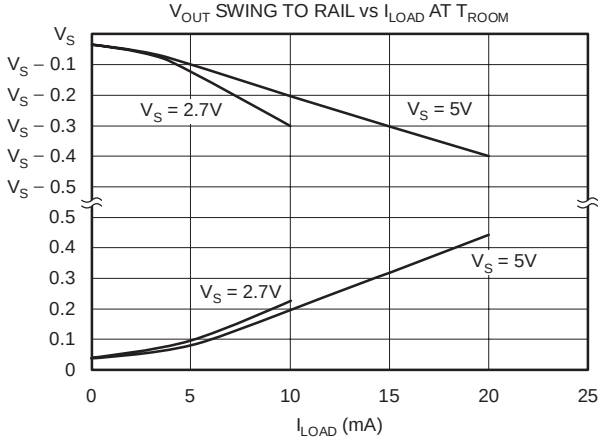
CLOSED−LOOP GAIN vs FREQUENCY



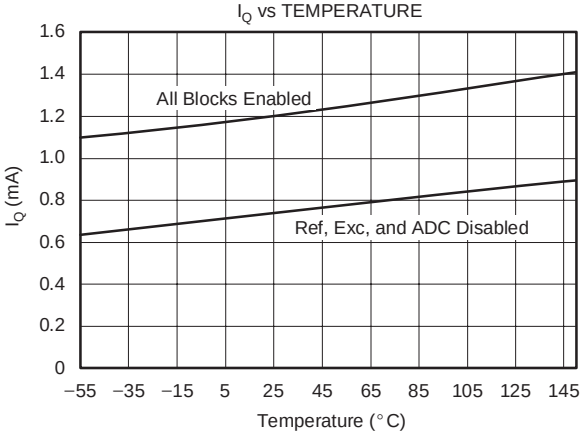
TYPICAL CHARACTERISTICS (Cont.)

T_A = +25°C, V_{SA} = V_{SD} = +5V (V_{SA} = $V_{SUPPLY\ ANALOG}$, V_{SD} = $V_{SUPPLY\ DIGITAL}$, V_{SA} must equal V_{SD}), GND_D = GND_A = 0, and V_{REF} = REF_{IN}/REF_{OUT} = +5V, unless otherwise noted.

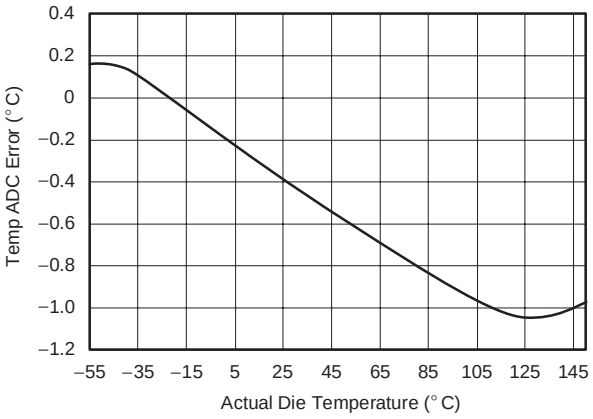
V_{OUT} SWING TO RAIL vs I_{LOAD} AT T_{ROOM}



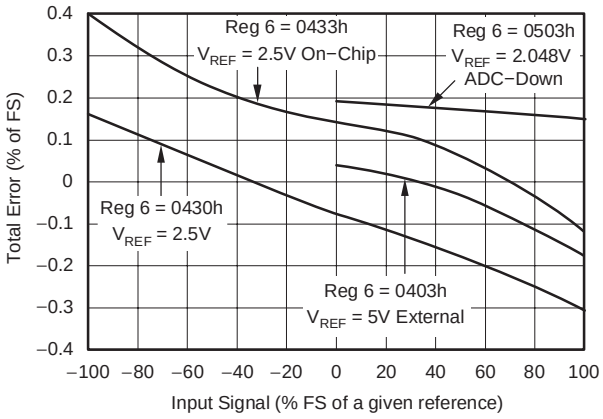
I_Q vs TEMPERATURE



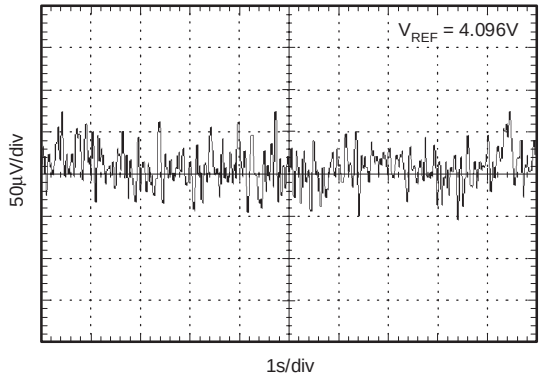
TEMPERATURE ADC INTERNAL MODE



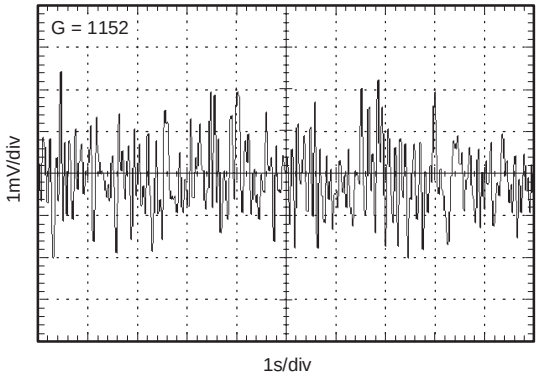
TEMPERATURE ADC EXTERNAL MODES



0.1Hz TO 10Hz V_{REF} NOISE



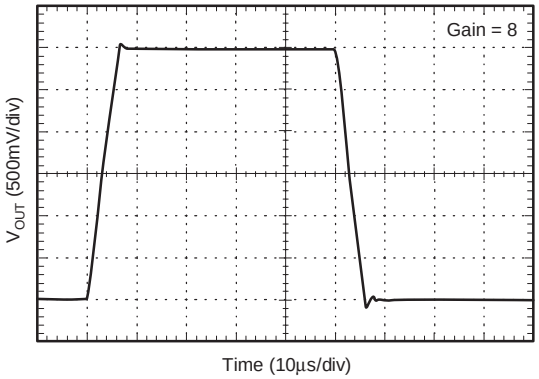
PGA V_{OUT} OUTPUT
0.1Hz TO 10Hz PEAK−TO−PEAK NOISE



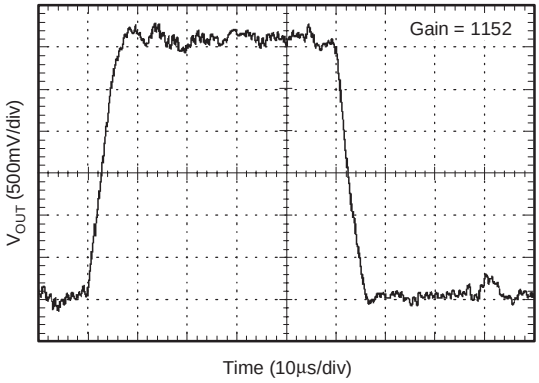
TYPICAL CHARACTERISTICS (Cont.)

T_A = +25°C, V_{SA} = V_{SD} = +5V (V_{SA} = $V_{SUPPLY\ ANALOG}$, V_{SD} = $V_{SUPPLY\ DIGITAL}$, V_{SA} must equal V_{SD}), GND_D = GND_A = 0, and V_{REF} = REF_{IN}/REF_{OUT} = +5V, unless otherwise noted.

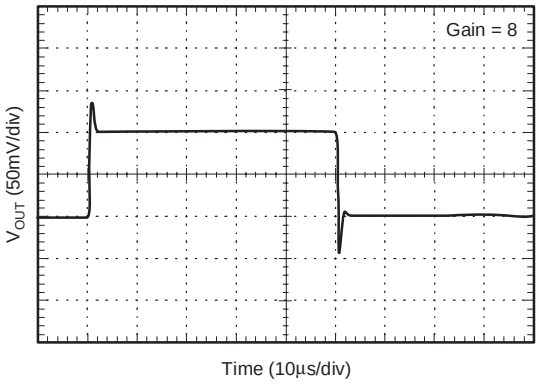
LARGE−SIGNAL STEP RESPONSE



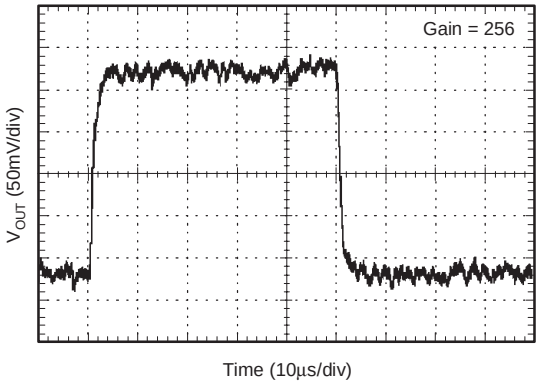
LARGE−SIGNAL STEP RESPONSE



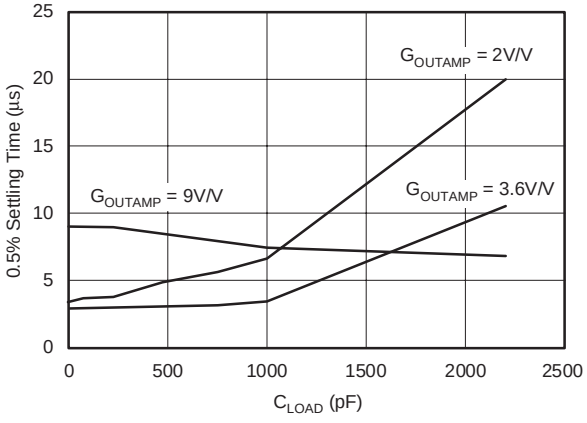
SMALL−SIGNAL STEP RESPONSE



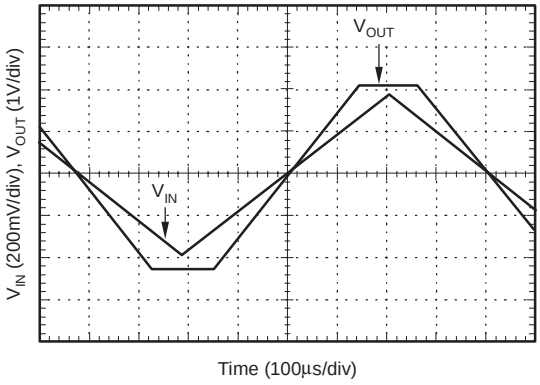
SMALL−SIGNAL STEP RESPONSE



CAPACITIVE LOAD DRIVE



OVERVOLTAGE RECOVERY



FUNCTIONAL DESCRIPTION

The PGA309 is a smart programmable analog signal conditioner designed for resistive bridge sensor applications. It is a complete signal conditioner with bridge excitation, initial span and offset adjustment, temperature adjustment of span and offset, internal/external temperature measurement capability, output over-scale and under-scale limiting, fault detection, and digital calibration. The PGA309, in a calibrated sensor module, can reduce errors to the level approaching the bridge sensor repeatability. Figure 1 shows a block diagram of the PGA309. Following is a brief overview of each major function.

SENSOR ERROR ADJUSTMENT RANGE

The adjustment capability of the PGA309 is summarized in Table 1.

FSS (full-scale sensitivity)	1mV/V to 245mV/V
Span TC	Over ±3300ppmFS/°C(1)
Span TC nonlinearity	≥ 10%
Zero offset	±200%FS(2)
Zero offset TC	Over ±3000ppmFS/°C(2)
Zero offset TC nonlinearity	≥ 10%
Sensor impedance	Down to 200Ω(3)

(1) Depends on the temperature sensing scheme
(2) Combined coarse and fine offset adjust
(3) Lower impedance possible by using a dropping resistor in series with the bridge

Table 1. PGA309 Adjustment Capability

GAIN SCALING

The core of the PGA309 is the precision low-drift and no 1/f noise front-end PGA. The overall gain of the front-end PGA + Output Amplifier can be adjusted from 2.7V/V to 1152V/V. The polarity of the inputs can be switched through the 2X2 input mux to accommodate sensors with unknown polarity output.

The front-end PGA provides initial coarse signal gain using a no 1/f noise, auto-zero instrumentation amplifier. The fine gain adjust is accomplished by the 16-bit attenuating gain digital-to-analog converter (DAC). The Gain DAC is controlled by the data in the Temperature Compensation Lookup Table driven by the temperature analog-to-digital converter (Temp ADC). In order to compensate for second-order drift nonlinearity, the span drift can be fitted to piecewise linear curves during calibration with the coefficients stored in an external nonvolatile EEPROM lookup table.

Following the fine gain adjust stage is the output amplifier that provides additional programmable gain. Two key output amplifier connections, V_{FB} and V_{SJ}, are brought out on the PGA309 for application flexibility. These connections allow for an accurate conditioned signal voltage while also providing a means for PGA309 output overvoltage and large capacitive loads for RFI/EMI filtering required in many end applications.

OFFSET ADJUSTMENT

The sensor offset adjustment is performed in two stages. The input referred Coarse Offset Adjust DAC has approximately a ±60mV offset adjustment range for a selected V_{REF} of 5V. The fine offset and the offset drift are canceled by the 16-bit Zero DAC that sums the signal with the output of the front-end instrumentation amplifier. Similar to the Gain DAC, the input digital values of the Zero DAC are controlled by the data in the Temperature Compensation Lookup Table, stored in external EEPROM, driven by the Temp ADC. The range of the Zero DAC is 0 to V_{REF}.

VOLTAGE REFERENCE

The PGA309 contains a precision low-drift voltage reference (selectable for 2.5V or 4.096V) that can be used for external circuitry through the REF_{IN}/REF_{OUT} pin. This same reference is used for the Coarse Offset Adjust DAC, Zero DAC, over/under-scale limits and sensor excitation and linearization through the V_{EXC} pin. When the internal reference is disabled, the REF_{IN}/REF_{OUT} pin should be connected to an external reference or to V_{SA} for ratiometric-scaled systems.

SENSOR EXCITATION AND LINEARIZATION

A dedicated circuit with a 7-bit + sign DAC for sensor voltage excitation and linearization is provided on the PGA309. This block scales the reference voltage and sums it with a portion of the PGA309 output to compensate the positive or negative bow-shaped nonlinearity exhibited by many sensors over their applied pressure range. Sensors not requiring linearization can be connected directly to the supply (V_{SA}) or the voltage reference pin (REF_{IN}/REF_{OUT}).

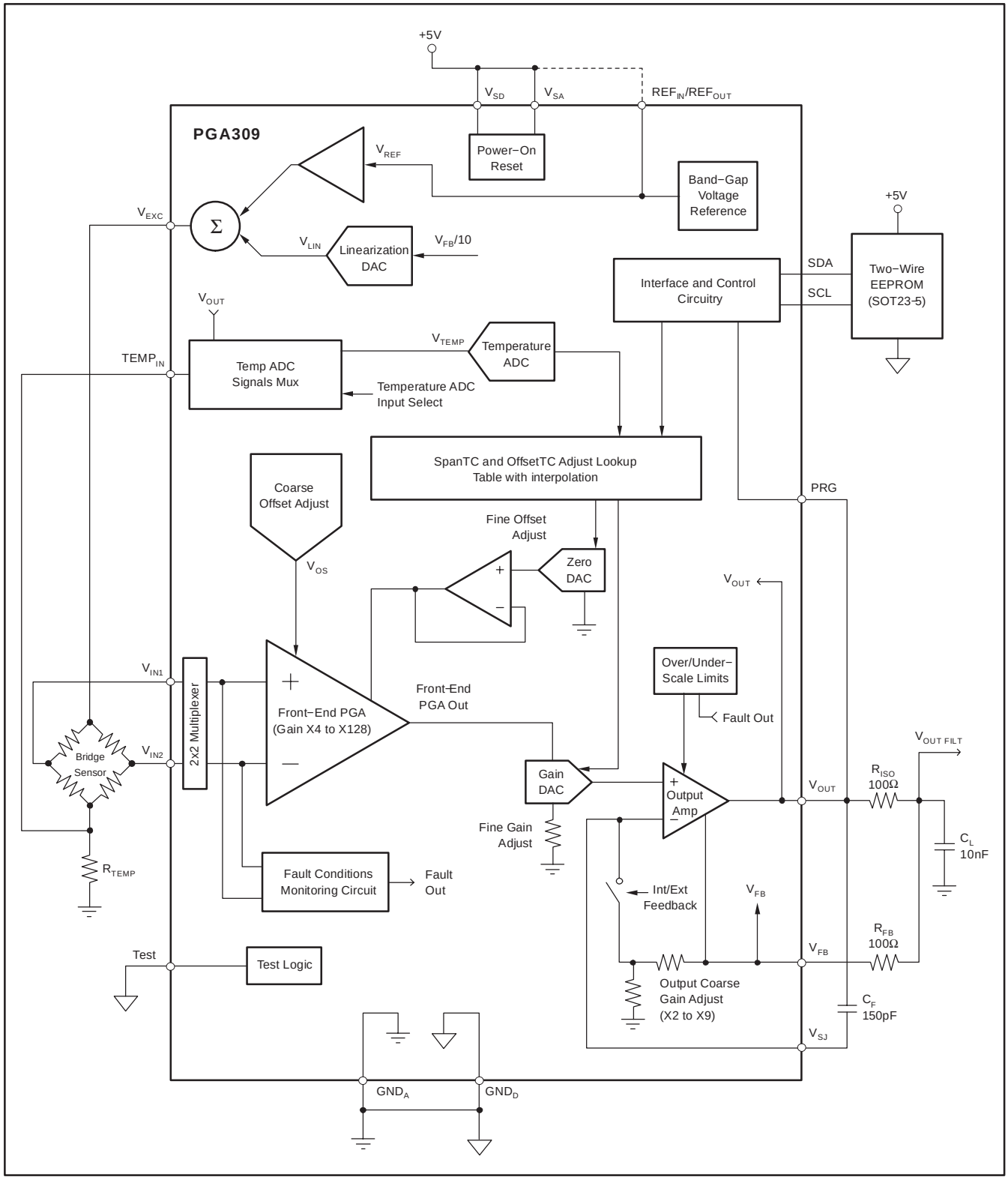


Figure 1. Simplified Diagram of the PGA309

ADC FOR TEMPERATURE SENSING

The compensation for the sensor span and offset drifts is driven by the temperature sense circuitry. Either internal or external temperature sensing is possible. The temperature can be sensed in one of the following ways:

- Bridge impedance change (excitation current sense, in the positive or negative part of the bridge), for sensors with large temperature coefficient of resistance (TCR > 0.1%/°C)
- On-chip PGA309 temperature, when the chip is located sufficiently close to the sensor
- External diode, thermistor, or RTD placed on the sensor membrane.

The temperature signal is digitized by the onboard Temp ADC. The output of the Temp ADC is used by the control digital circuit to pull the data from the Lookup Table in an external EEPROM, and set the output of the Gain DAC and the Zero DAC to the calibrated values as temperature changes.

An additional function provided through the Temp ADC is the ability to read the V_{OUT} pin back through the Temp ADC input mux. This provides flexibility for a digital output through either One-Wire or Two-Wire interface, as well as the possibility for an external microcontroller to perform real-time custom calibration of the PGA309.

EXTERNAL EEPROM AND TEMPERATURE COEFFICIENTS

The PGA309 uses an industry-standard Two-Wire external 256 to 1K-bit EEPROM (typically, a SOT23-5 package). The PGA309 has been tested to operate with EEPROM parts Microchip 24LCxx and 24AAxx.

The first part of the external EEPROM contains the configuration data for the PGA309, with settings for:

- Register 3—Reference Control and Linearization
- Register 4—PGA Coarse Offset and Gain/Output Amplifier Gain
- Register 5—PGA Configuration and Over/Under-Scale Limit
- Register 6—Temp ADC Control

This section of the EEPROM contains its own individual checksum (Checksum1).

The second part of the external EEPROM contains up to 17 temperature index values and corresponding temperature coefficients for the Zero DAC and Gain DAC adjustments with measured temperature and contains its own checksum (Checksum2). The PGA309 lookup logic contains a linear interpolation algorithm for accurate DAC adjustments between stored temperature indexes. This approach allows for a piecewise linear temperature compensation of up to 17 temperature indexes and associated temperature coefficients.

If either Checksum1, Checksum2, or both are incorrect, the output of the PGA309 is set to high-impedance.

FAULT MONITOR

To detect sensor burnout or short, a set of four comparators are connected to the inputs of the front-end PGA. If any of the inputs are taken to within 40mV of ground or V_{EXC}, or violate the input CMR of the front-end PGA, then the corresponding comparator sets a sensor fault flag that causes the PGA309 V_{OUT} to be driven within 100mV of either V_{SA} or ground, depending upon the alarm configuration setting (Register 5—PGA Configuration and Over/Under-Scale Limit). This will be well above the set over-scale limit level or well below the set under-scale limit level. The state of the fault condition can be read in digital form in Register 8—Alarm Status Register. If the over/under-scale limiting is disabled, the PGA309 output voltage will still be driven within 100mV of either V_{SA} or ground, depending upon the alarm configuration setting.

There are five other fault detect comparators that help detect subtle PGA309 front-end violations that could result in linear voltages at V_{OUT} and be interpreted as valid states. These are especially useful during factory calibration and setup and are configured through Register 5—PGA Configuration and Over/Under-Scale Limit. Their status can also be read back through Register 8—Alarm Status Register.

OVER-SCALE AND UNDER-SCALE LIMITS

The over-scale and under-scale limit circuitry combined with the fault monitor circuitry provides a means for system diagnostics. A typical sensor-conditioned output may be scaled for 10% to 90% of the system ADC range for the sensor normal operating range. If the conditioned pressure sensor is below 4%, it is considered under-pressure; if over 96%, it is considered over-pressure.

The PGA309 over/under-scale limit circuit can be programmed individually for under-scale and over-scale that clip or limit the PGA309 output. From a system diagnostic view, it is known that 10% to 90% of ADC range is normal operation, < 4% is under-pressure, and > 96% is over-pressure. If the fault detect circuitry is used, a detected fault will cause the PGA309 output to be driven to positive or negative saturation. If this fault flag is programmed for high, then > 97% ADC range will be a fault; if programmed for low, then < 3% ADC range will be a fault. Now the system software can be used to distinguish between over- or under-pressure condition, which indicates an out-of-control process, and a sensor fault.

POWER-UP AND NORMAL OPERATION

The PGA309 has circuitry to detect when the power supply is applied to the PGA309, and reset the internal registers and circuitry to an initial state. This reset also occurs when the supply is detected to be invalid, so that the PGA309 is in a known state when the supply becomes valid again. The threshold for this circuit is approximately +1.5V to +2.5V. After the power supply becomes valid, the PGA309 waits for approximately 25ms and then attempts to read the configuration data from the external EEPROM device.

If the EEPROM has the proper flag set in address location 0 and 1, then the PGA309 continues reading the EEPROM, otherwise, the PGA309 waits for one second before trying again. If the PGA309 detects no response from the EEPROM, the PGA309 waits for one second and tries again; otherwise, the PGA309 tries to free the bus and waits for 25ms before trying to read the EEPROM again. If successful (including valid checksum data), the PGA309 triggers the Temp ADC to measure temperature. For 16-bit resolution results the converter takes approximately 125ms to complete a conversion. Once the conversion is complete, the PGA309 begins reading the Lookup Table information from the EEPROM to calculate the settings for the Gain DAC and Zero DAC.

The PGA309 reads the entire Lookup Table so that it can determine if the checksum for the Lookup Table is correct. Each entry in the Lookup Table requires approximately 500µs to read from the EEPROM. Once the checksum is determined to be valid, the calculated values for the Gain and Zero DACs are updated into their respective registers, and the output amplifier is enabled. The PGA309 then begins looping through this entire procedure, starting with reading the EEPROM configuration registers, then starting a new conversion on the Temp ADC, which then triggers reading the Lookup Table data from the EEPROM. This loop continues indefinitely.

DIGITAL INTERFACE

There are two digital interfaces on the PGA309. The PRG pin uses a One-Wire, UART-compatible interface with bit rates from 4.8Kbits/s to 38.4Kbits/s. The SDA and SCL pins together form an industry standard Two-Wire interface at clock rates from 1kHz to 400kHz. The external EEPROM uses the Two-Wire interface. Communication to the PGA309 internal registers, as well as to the external EEPROM, for programming and readback can be conducted through either digital interface.

It is also possible to connect the One-Wire communication pin, PRG, to the V_{OUT} pin in true three-wire sensor modules and still allow for programming. In this mode, the PGA309 output amplifier may be enabled for a set time period and then disabled again to allow sharing of the PRG pin with the V_{OUT} connection. This allows for both digital calibration and analog readback during sensor calibration in a three-wire sensor module.

The Two-Wire interface has timeout mechanisms to prevent bus lockup from occurring. The Two-Wire master controller in the PGA309 has a mode that attempts to free up a stuck-at-zero SDA line by issuing SCL pulses, even when the bus is not indicated as idle after the timeout period has expired. The timeout will only apply when the master portion of the PGA309 is attempting to initiate a Two-Wire communication.

DETAILED DESCRIPTION

GAIN SCALING

The PGA309 contains three main gain blocks for scaling differential input bridge sensor signals, as shown in Figure 2. The front-end PGA contains the highest gain selection to allow for the highest signal-to-noise ratio by applying the largest gain at the front of the signal chain before the addition of other noise sources. The Front-end PGA gain select has eight settings (x4, x8, x16, x23.27, x32, x42.67, x64, x128) and is set by Register 4 bits (11:8). Bit 11 selects the polarity of the input mux.

The front-end PGA is followed by the Gain DAC. The fine gain adjust is controlled by the 16-bit Gain DAC and is adjustable from x0.3333 to x1. Register 2 is used only for the Gain DAC setting.

Final signal gain is applied through the output amplifier, which has an internal gain select of seven settings (x2, x2.4, x3, x3.6, x4.5, x6, x9). The output amplifier has a selection to disable the internal gain and allow user-supplied external resistors to set the output amplifier gain. Register 4 bits (14:12) select the internal output amplifier gains, except when programmed with '111' when the internal feedback is disabled. The combined gain blocks allow for a V_{OUT}/V_{DIFF} signal gain of x2.666 (400kHz bandwidth) to x1152 (15.5kHz bandwidth).

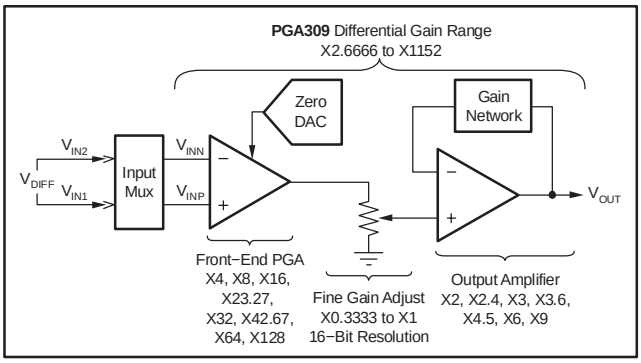


Figure 2. Gain Blocks of the PGA309

Example: Solving for Gain Settings

An example bridge sensor application will be used to examine internal nodes of the PGA309 that are related to the gain blocks (refer to Figure 3 and Figure 4).

Given:
- FSS = 20mV/V
- V_{OS} =0mV
- V_{REF} = +5V
- V_{EXC} = +5V
- V_{SA} = +5V
- R_{BRG} = 2kΩ
- $VOUT_{MIN}$ = +0.5V
- $VOUT_{MIAX}$= +4.5V

Find:
- Front-End PGA Gain
- Gain DAC Setting
- Zero DAC Setting
- Over Amplifier Gain

Solution:

1. Maximum Sensor Output:
   $V_{BRmax} = (FSS)(V_{EXC})$
   $V_{BRmax} = (20mV/V)(5V) = 100mV$
2. Total Gain:
   $GT = (VOUT_{MAX} - VOUT_{MIN})(V_{BRmax})$
   $GT = (4.5V - 0.5V)(100mV) = 40$
3. Partition the Gain:
   Front-End PGA Gain = X23.27
   Output Amplifier Gain = X2
   Fine Gain (Gain DAC) = X0.859475719
   GT = (Front-End PGA Gain)(Fine Gain)(Output Amp Gain)
   GT = (23.27)(0.859475719)(2) = 40
4. Calculate exact DAC Gain value:
   1LSB = (1.000000000 − 0.333333333)/65536
   $= 1.0172526 \times 10^{-5}$V/V
   Decimal # counts
   = (Desired Gain − 0.333333333)/$(1.0172526 \times 10^{-5})$
   Decimal # counts
   = (0.859475719 − 0.333333333)/(1LSB)
   = 51,721.90133
4. Calculate exact DAC Gain value, *continued*:
   Use 51,722 counts→
   0xCA0A→1100 1010 0000 1010 →X0.859475571
5. Calculate Zero DAC value:
   $V_{ZERO\ DAC}$
   $= (VOUT_{MIN})/[(Gain\ DAC)(Output\ Amplifier\ Gain)]$
   $V_{ZERO\ DAC}$
   = (0.5V)/[(X0.859475571)(2)] = 0.29087505V
   Decimal # counts = $V_{ZERO\ DAC}/(V_{REF}/65536)$
   Decimal # counts
   = 0.29087505/(5/65536) = 3812.55746
   Use 3813 counts→
   0x0EE5→0000 1110 1110 0101 →0.290908813V
6. Calculate V_{CM} and V_{DIFF} for Maximum Sensor Output (see Figure 3):
   $V_{DIFF} = V_{INP} - V_{INN}$
   V_{DIFF} = 2.550 − 2.450
   = 100mV
   $V_{CM} = (V_{INP} + V_{INN})/2$
   V_{CM} = (2.550V + 2.450V)/2
   = 2.5V

The front-end PGA of the PGA309 is a three op amp instrumentation amplifier for optimum rejection of common-mode voltages. This instrumentation amplifier is constructed using op amps with auto-zero front-ends to virtually eliminate 1/f noise.

As with any instrumentation amplifier there are limitations on the output voltage swing and input common-mode voltage range. The circuit in Figure 3 is representative of the front-end PGA inside of the PGA309 and is used to evaluate critical internal node voltages to ensure that output voltage swing and common-mode limits are not violated. It is possible to violate the limits of these internal nodes and still have apparently valid output voltages at V_{OUT} of the PGA309. There are internal comparators that can be set to monitor these internal nodes to indicate an out-of-limit condition during sensor calibration (see Fault Monitor section).

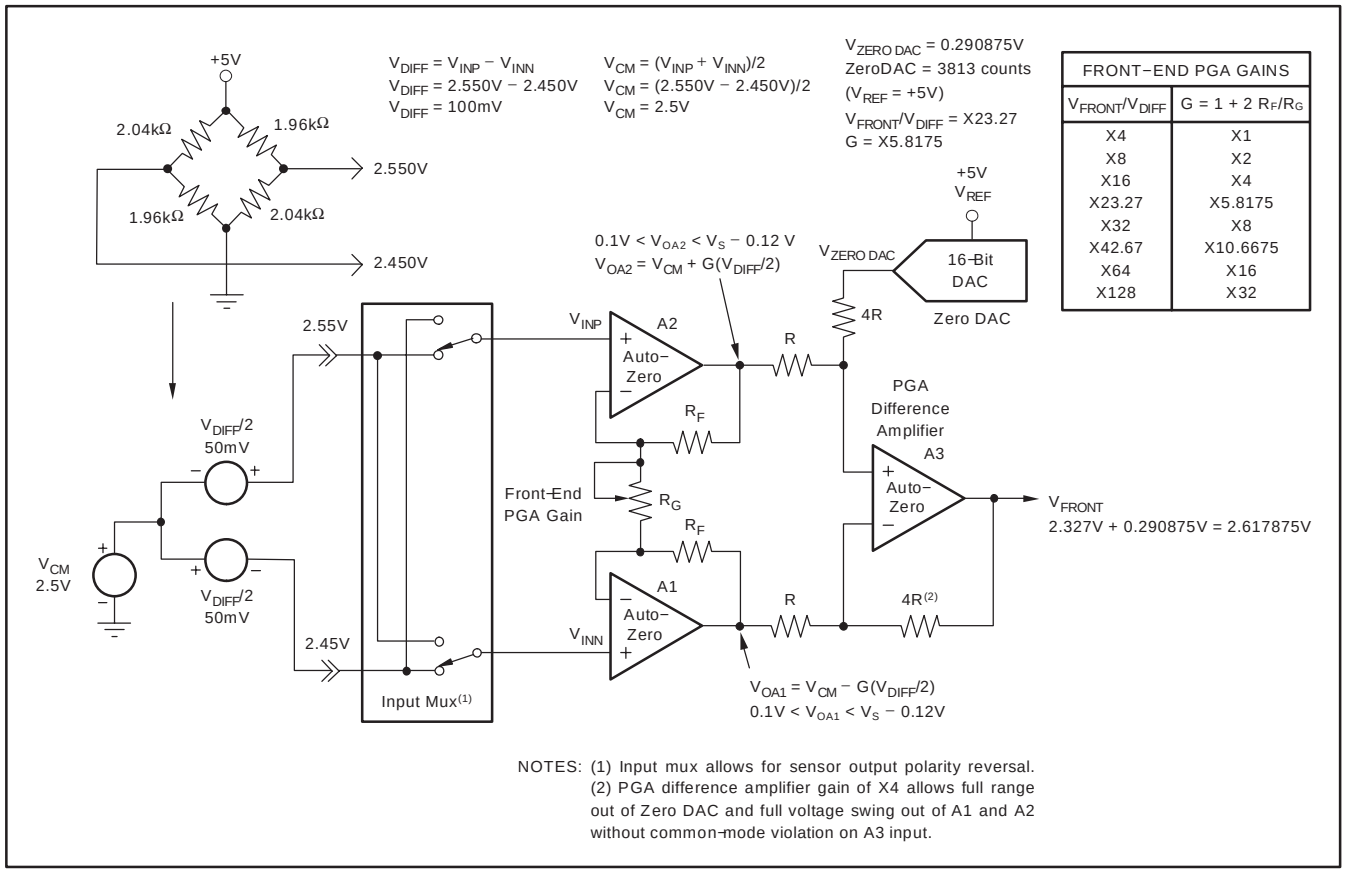
After appropriate scaling for the PGA309 gain blocks are chosen, a simple hand analysis can check for internal node limit violations. It is key to convert the input voltages to the PGA309 (V_{INP}, V_{INN}) to common-mode and differential components for the maximum sensor output, V_{BRmax}. The model for this conversion is illustrated in Figure 3. The front-end PGA must have a gain of 4 in difference amplifier A3. To analyze important internal nodes V_{OA1} and V_{OA2}, it is necessary to assign the proper gain factor (G) to op amps A1 and A2. This is detailed in Figure 3 with the respective equations for the output voltages shown at the appropriate nodes. For V_{BRmax}, V_{OA1} and V_{OA2} are within the allowed voltage swing of:

$$0.1V < (V_{OA1} \text{ or } V_{OA2}) < V_S - 0.12$$

Or for this example:

$$0.1V < (V_{OA1} \text{ or } V_{OA2}) < 4.88V$$

Other applications may yield different results that require different gain scaling or a resistor in the positive or negative leg of the sensor excitation path to adjust the common-mode input voltage of the PGA309. The input voltage range of the PGA309 is specified as $0.2V < IVR < V_{SA} - 1.5V$, which for this application translates to $0.2V < IVR < 3.5V$. In Figure 3 we see $V_{INP} = 2.550V$ and $V_{INN} = 2.450V$, which is within the acceptable input voltage range specification.



FRONT−END PGA GAINS	
V_{FRONT}/V_{DIFF}	$G = 1 + 2\ R_F/R_G$
X4	X1
X8	X2
X16	X4
X23.27	X5.8175
X32	X8
X42.67	X10.6675
X64	X16
X128	X32

NOTES: (1) Input mux allows for sensor output polarity reversal.
(2) PGA difference amplifier gain of X4 allows full range out of Zero DAC and full voltage swing out of A1 and A2 without common−mode violation on A3 input.

Figure 3. Front-End PGA Gain

The output (V_{FRONT}) of difference amplifier A3 has a gain of 4 in it for voltages out of A2 and A1, but a gain of 1 for voltages out of the Zero DAC. V_{FRONT} is shown with the contribution from V_{DIFF} times the front-end PGA gain plus the Zero DAC output voltage. The V_{FRONT} signal is further processed through the Gain DAC and output amplifier gain blocks.

Figure 4 depicts the Gain DAC and Output Amplifier gain blocks inside the PGA309. For this example the Gain DAC was set to x0.859475571 and the output amplifer to X2. As shown in Figure 4, the net output voltage, V_{OUT}, is 4.5V for the maximum sensor output, V_{BRmax}.

For the sensor output of zero volts:

$$VOUT_{MIN} = V_{ZERO\ DAC}\ [(Gain\ DAC)(Output\ Amplifier\ Gain)]$$

For this example:

$$VOUT_{MIN} = 0.290908813V\ [(0.859475571)(2)] = 0.5000V$$

The output amplifier has external connections, which allow the end-user maximum flexibility in output amplifier configurations for a variety of applications. The use of the V_{FB} and V_{SJ} pins, are described in the Output Amplifier section.

OFFSET SCALING

The coarse offset adjust is implemented before the front-end PGA gain to allow for maximum dynamic range. Many bridge sensors have initial offsets comparable to their maximum scale outputs. The coarse offset adjust can be applied as positive or negative. It is implemented in a 4-bit DAC + sign and contains 14 positive selections, 14 negative selections, and zero.

The resolution in either the positive or negative range is $V_{REF}/1200$. For a +5V reference, this translates to 4.2mV steps. Figure 5 depicts the PGA309 with the gain settings used for the example bridge sensor application detailed in the Gain Scaling section.

The conversion of the bridge initial differential offset plus its common-mode to the differential plus common-mode voltage source model is shown in Figure 5 for an initial bridge sensor offset of −34mV ($V_{INP} - V_{INN}$). Conceptually, this divides into two 17mV offset voltages with polarities as shown. If the coarse offset adjust is set for +34mV offset ($V_{INP} - V_{INN}$), then the initial bridge offset is cancelled exactly. Any residual initial bridge offset not cancelled by the coarse offset adjust will be gained up by the front-end PGA gain and needs to be accounted for when setting the fine offset adjust by using the Zero DAC.

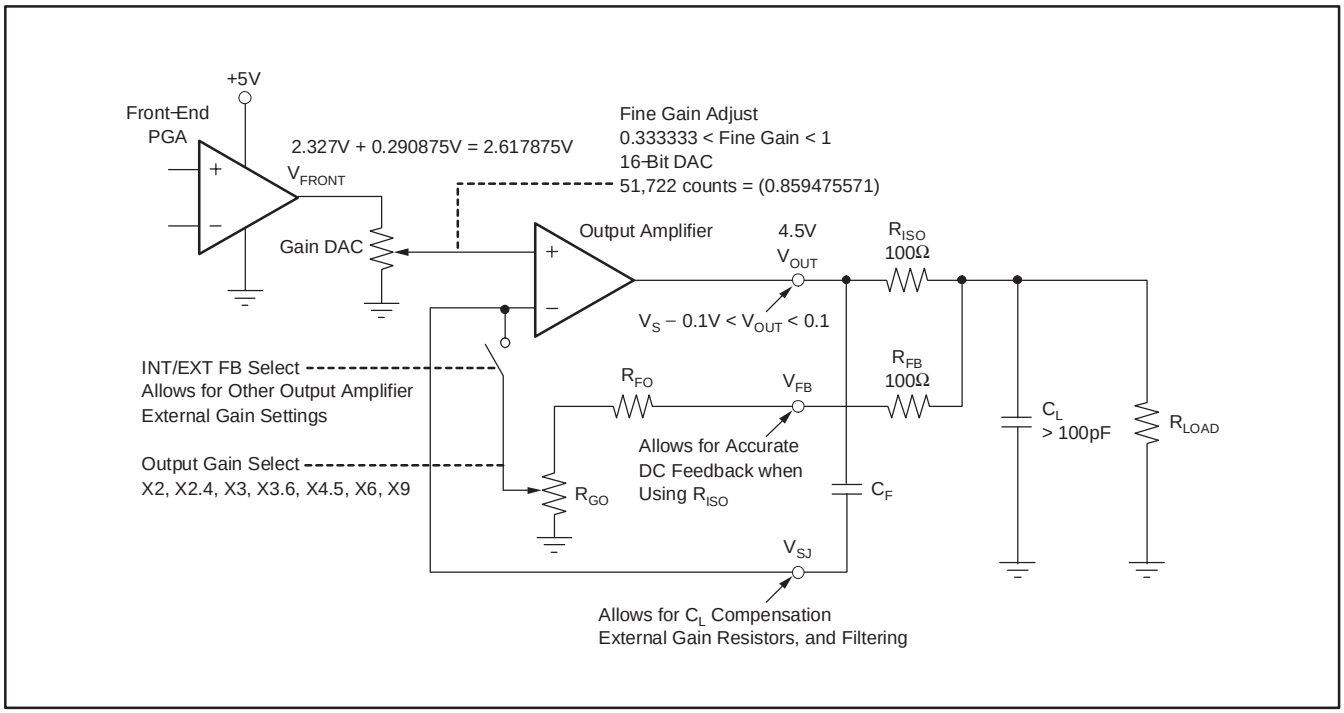


Figure 4. Fine Gain Adjust of the PGA309

The coarse offset adjust is set by Register 4 bits (4:0), with bit 4 determining the coarse offset polarity as negative for a '1' and positive for a '0'. The internal architecture of the coarse offset adjust does yield duplicate digital codes for $-7(V_{REF}/1200)$ and $+7(V_{REF}/1200)$. See the Register Description section under Register 4 for a complete mapping of the coarse offset adjust settings.

The fine offset adjust is set by the Zero DAC. RTO (referred-to-output), the Zero DAC setting is gained by the Gain DAC (fine gain adjust) and the output amplifier gain. The Zero DAC is a unipolar, 16-bit DAC, with its reference being the V_{REF} setting of the PGA309. The range of the Zero DAC is ensured to be linear from $2\%V_{REF}$ to $98\%V_{REF}$. The data format is 16-bit unsigned. Register 1 bits (15:0) are used for the Zero DAC setting.

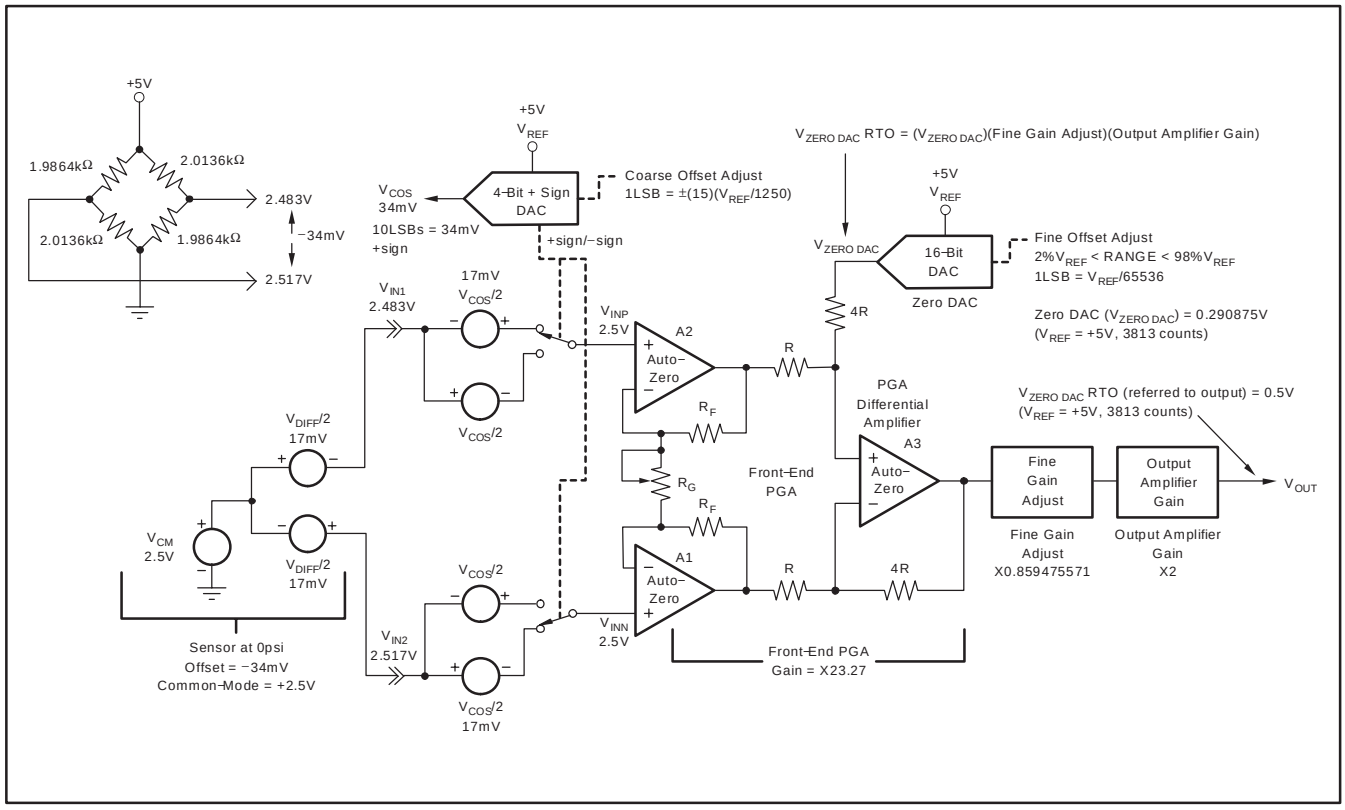


Figure 5. Coarse and Fine Offset Adjust

NOISE AND COARSE OFFSET ADJUST

The PGA309 front-end PGA contains auto-zero operational amplifiers that allow precision, low-noise measurements free from flicker, or 1/f noise, that is typically present in regular low-voltage CMOS op amps.

This auto-zero topology operates by canceling amplifier low-frequency noise and offset each clock cycle of an internal oscillator. This flattens the low-frequency noise voltage spectrum of the PGA309, leaving only a small residual clock feedthrough component at ~7kHz and its multiples. Figure 6 details the PGA309 output voltage noise spectrum for coarse offset adjust = 0mV. The advantage of this auto-zero method is that by filtering the output of the PGA309 proportionally, higher precision can be achieved, unlike conventional CMOS operational amplifiers where averaging does not improve the signal-to-noise ratio in the 1/f noise, region. In addition, the auto-zero technique allows the PGA309 input offset voltage to achieve very good temperature and time stability.

The PGA309 low-frequency voltage noise density (RTI) is ~210nV/$\sqrt{Hz}$. To convert this to a peak-to-peak amplitude for oscilloscope measurements, the following equation is supplied:

$$V_{NPP} = (e_{ND})(\sqrt{BW})(\text{crest factor})$$

where: V_{NPP} = voltage noise peak-to-peak (nV_{PP})

e_{ND} = voltage noise density (nV/$\sqrt{Hz}$)

BW = bandwidth of interest (Hz)

Crest Factor = probability factor for conversion of rms noise to peak-to-peak noise (crest factor of 6 reduces probability of seeing a larger peak-to-peak amplitude to < 0.3%).

PGA309 peak-to-peak noise, RTI, BW = 10Hz:

$$V_{NPP} = (210nV/\sqrt{Hz})(\sqrt{10Hz})(6) = 3984nV_{PP}$$
$$= 3.98\mu V_{PP}$$

To compensate for bridge sensors with a large initial offset, the input stages of the PGA309 front-end PGA incorporate a patented circuit for the coarse offset adjust based on the auto-zero topology. For each clock cycle of the internal auto-zero oscillator, the offsets and noise of the input amplifier stages are subtracted from the input signal, and the result is summed with a small voltage produced by the Coarse Offset Adjust DAC. This resulting value becomes the input-referred offset of the PGA309. This value can be positive or negative as described in the Offset Scaling section of this data sheet. This operation does not increase the low frequency 1/f noise of the PGA309. However, the mismatches of internal elements in the Coarse Offset DAC can produce temperature and long-term stability errors on the same order as regular, traditional CMOS op amps (that is, temperature drift of input offset voltage of up to 10µV/°C).

To produce a value that is temperature- and time-stable, the Coarse Offset DAC circuitry incorporates a chopping circuit that rotates internal components, averaging the mismatch error on the output of the Coarse Offset Adjust DAC. This produces a very time- and temperature-stable coarse offset adjust.

The design compromise of the Coarse Offset DAC chopping technique is a clock feed−through glitch that can be seen at V_{OUT}, the output of the PGA309, due to the rotating elements. With the Coarse Offset Adjust set to 0mV the clock feed-through components are practically negligible on the V_{OUT} signal of the PGA309, as shown in Figure 7.

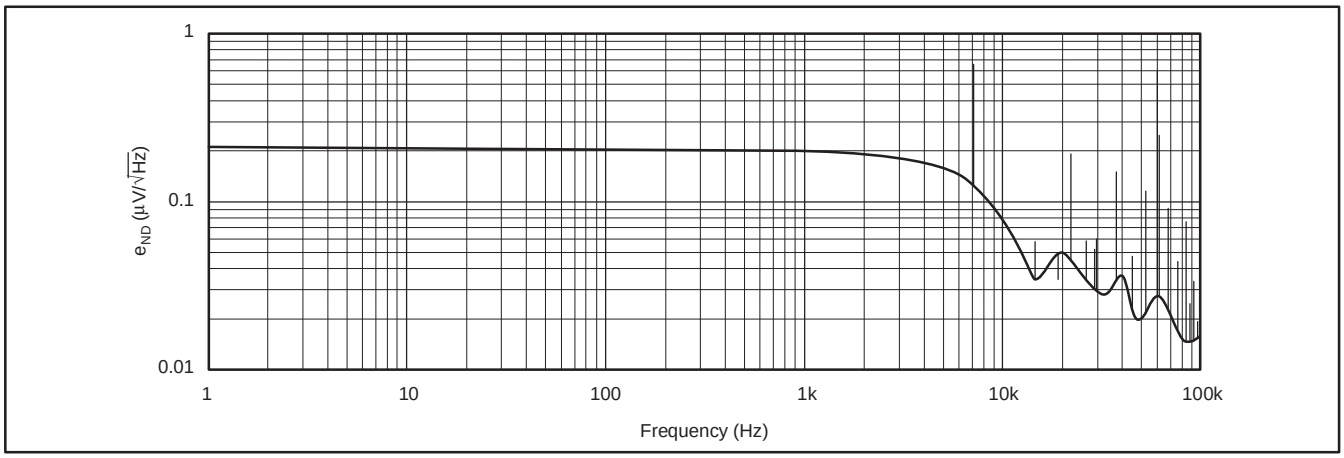


Figure 6. V_{OUT} Noise Power Spectrum for Coarse Offset Adjust = 0mV, Gain = 1152, CLK_CFG = ‘00’ (default).

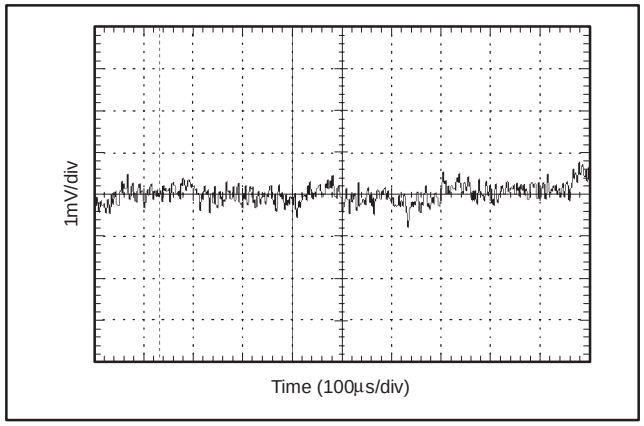


Figure 7. V_{OUT} Clock Feedthrough for Coarse Offset Adjust = 0mV, Gain = 1152, CLK_CFG = '00' (default).

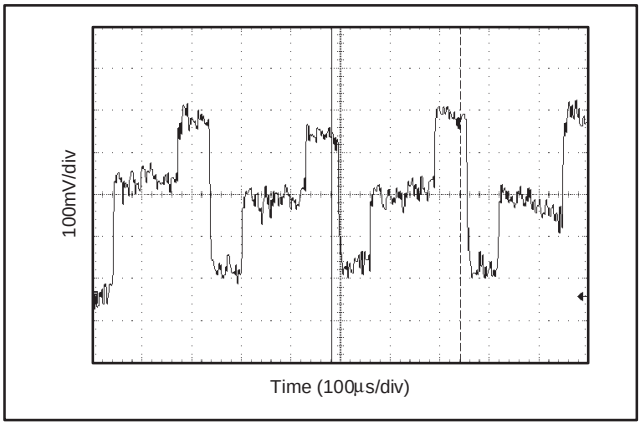


Figure 8. V_{OUT} Clock Feedthrough Glitch, Coarse Offset Adjust = 59mV, Gain = 1152, CLK_CFG = '00' (default). V_{OUT} Glitch (RTI) = 347μV_{PP}.

As the Coarse Offset Adjust DAC value increases the amplitude of the clock, feedthrough glitch also increases. For V_{REF} = +5V and a full-scale Coarse Offset DAC value of 56mV, the clock feedthrough glitch is shown in Figure 8. This scope photo is for the PGA309 set in its maximum internal gain of x1152, with the Coarse Offset Adjust DAC set to −59mV and V_{IN} set to +61mV. Referred back to the input, this V_{OUT} glitch is only 347μV_{PP} (0.4V_{PP}/1152). This glitch occurs at half of the internal auto-zero clock; typically, 3.5kHz. This glitch does not reflect back into the low-frequency range and can be filtered out if the signal of interest is at or below 1kHz. Figure 9 is a scope photo of V_{OUT} peak-to-peak noise for the previous case. Figure 10 shows the V_{OUT} noise spectrum for the case where the Coarse Offset Adjust DAC is set to −59mV and V_{IN} = +61mV. In Figure 10, the baseband noise is about the same as when the coarse offset adjust was set to zero, as in Figure 10, but with an additional spike at about 3.5kHz.

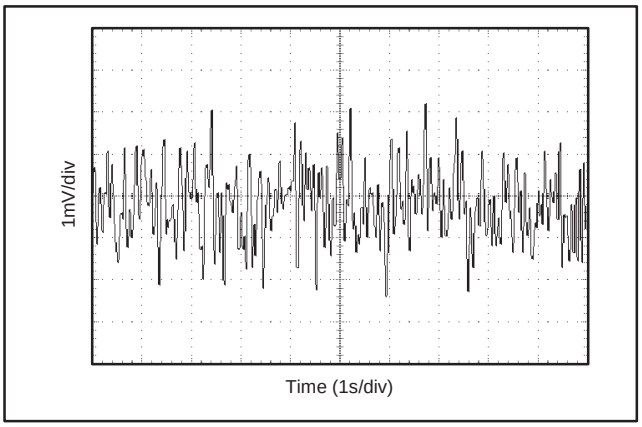


Figure 9. 0.1Hz to 10Hz V_{OUT} Peak-to-Peak Noise for Coarse Offset Adjust = −59mV, Gain = 1152, V_{IN} = +61mV.

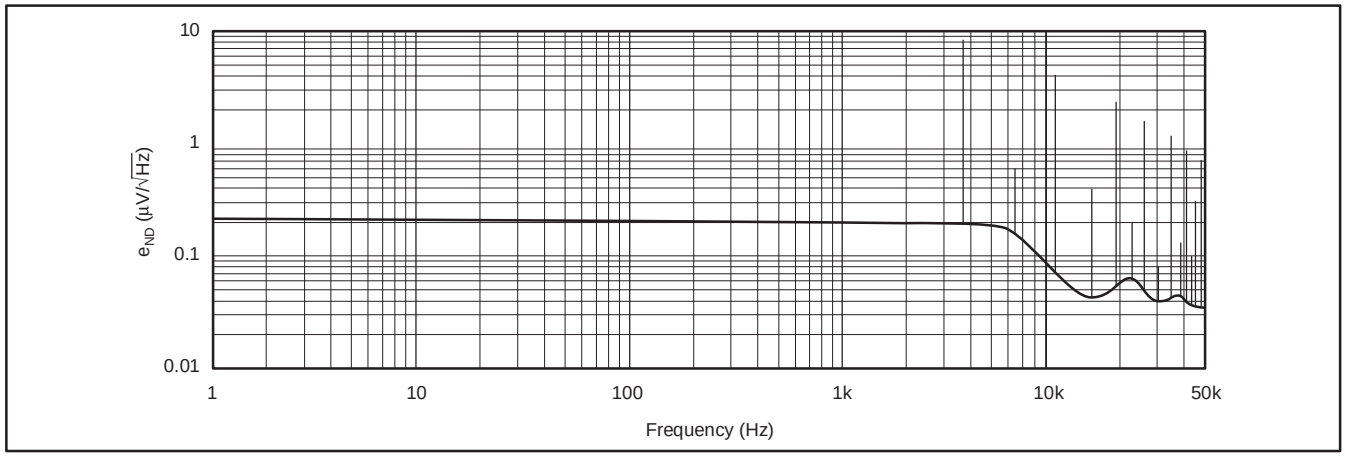


Figure 10. V_{OUT} Noise Spectrum for Coarse Offset Adjust = −56mV, Gain = 1152, CLK_CFG = '00' (default).

For applications where the clock feedthrough glitch from the Coarse Offset Adjust DAC chopping circuitry is an issue, there are alternate modes that can be selected for the Coarse Offset DAC clocking and the auto-zero clocking of the front-end PGA. Register 5 bits (13:12) are referenced as CLK_CFG1 and CLK_CFG0, respectively. Table 2 outlines the clocking schemes available using these bits. Up to this point, CLK_CFG = '00' has been discussed.

CLK_CFG MODE	CLK_CFG1 BIT D13	CLK_CFG1 BIT D13	AUTO-ZERO PGA FRONT-END	CHOPPING COARSE OFFSET DAC
00 (default)	0	0	7kHz typical	3.5kHz typical
01	0	1	7kHz typical	Off (none)
10	1	0	7kHz typical, Random Clocking	3.5kHz typical, Random Clocking
11	1	1	7kHz typical	3.5kHz typical, Random Clocking

Table 2. PGA309 Clocking Schemes

In the CLK_CFG = '01' mode, the Coarse Offset Adjust DAC chopping is turned off. The clock feedthrough glitch is no longer present (see Figure 11 for 0Hz to 10Hz V_{OUT} peak-to-peak noise) and the V_{OUT} noise spectrum is clean (see Figure 11). However, the input Coarse Offset Adjust DAC is no longer temperature-stable. Typical span drift is generally linear with temperature and may be acceptable in applications where the PGA309 is located close to the bridge sensor and they are both calibrated together. The drift of the Coarse Offset Adjust DAC simply sums with the bridge sensor offset drift and they are both calibrated out.

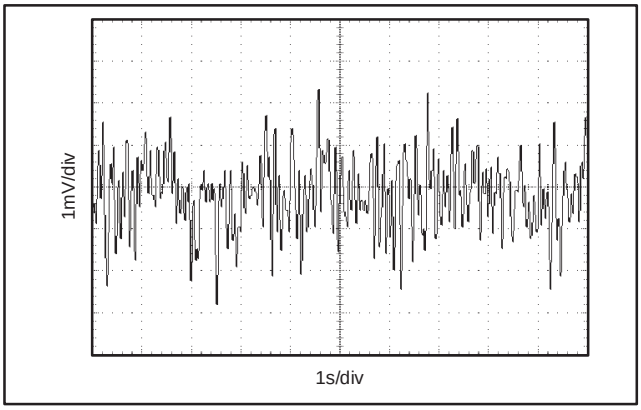


Figure 11. 0.1Hz to 10Hz V_{OUT} Peak-to-Peak Noise for Coarse Offset Adjust = −56mV, Gain = 1152, V_{IN} = +57mV, CLK_CFG = '01', V_{NPP} (RTI) = 4.44µV_{PP}.

CLK_CFG = '10' mode and CLK_CFG = '11' mode turn on different clock randomization schemes for the front-end PGA auto-zero and Coarse Offset DAC chopping. Although this does not reduce the amplitude of the clock feedthrough glitch (see Figure 8), it does spread the glitch energy over a wider frequency range. This removes the fixed spike at half of the input auto-zero clock frequency, but raises the noise floor in the lower frequency range, thus increasing the baseband noise. CLK_CFG = '11' mode simply *whitens* the peak-to-peak noise in from the 1Hz region to about the 7kHz region by modulating both the auto-zero and chopping clocks. In CLK_CFG = '10' mode, the Coarse Offset DAC chopping clock is modulated but not the auto-zero clock. The results of these modes are shown in both voltage noise spectrum and peak-to-peak noise plots in Figure 13, Figure 14, Figure 15, and Figure 16.

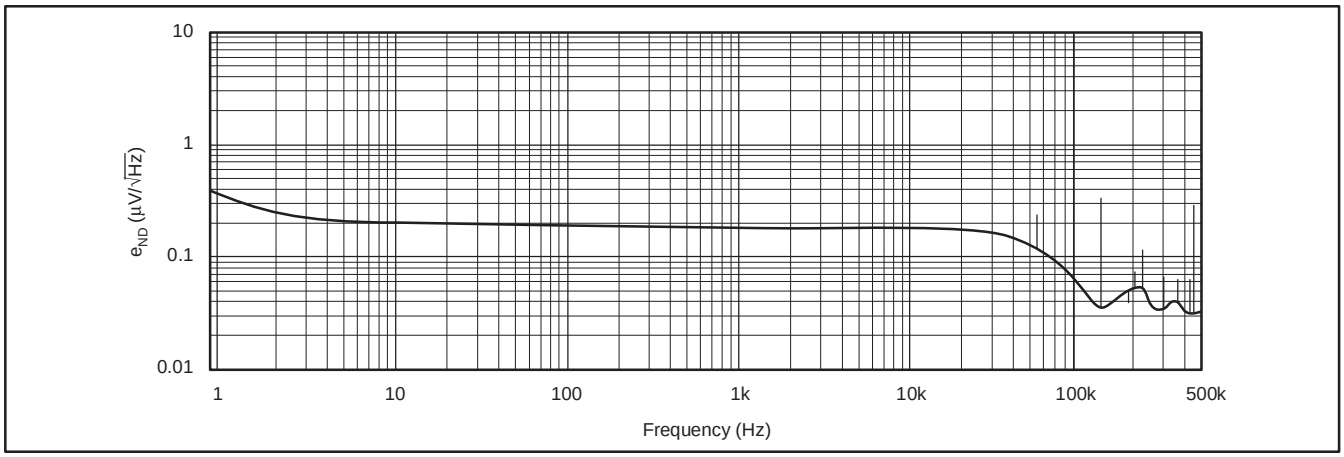


Figure 12. V_{OUT} Noise Spectrum for Coarse Offset Adjust = −56mV, Gain = 1152, V_{IN} = +57mV, CLK_CFG = '01'.

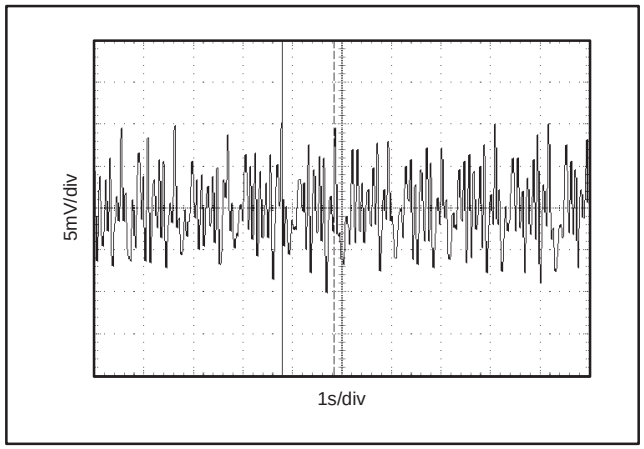


Figure 13. 0.1Hz to 10Hz V_{OUT} Peak-to-Peak Noise for Coarse Offset Adjust = −56mV, Gain = 1152, V_{IN} = +57mV, CLK_CFG = '10', V_{NPP} (RTI) = 18.4µV_{PP}.

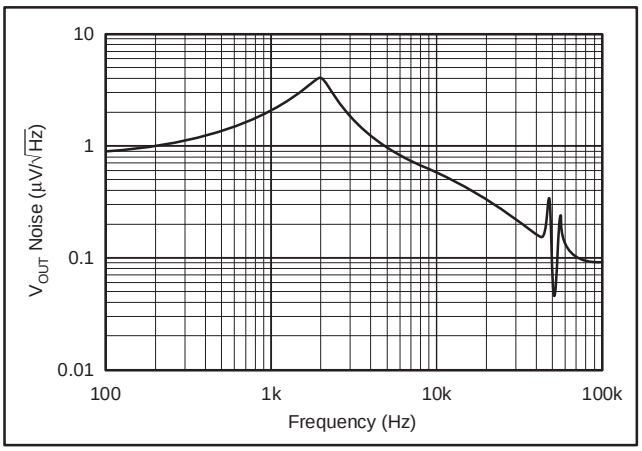


Figure 15. V_{OUT} Noise Spectrum for Coarse Offset Adjust = −56mV, Gain = 1152, V_{IN} = +57mV, CLK_CFG = '10'.

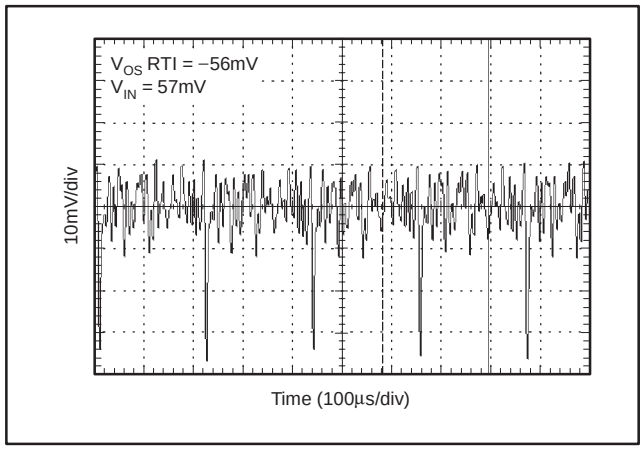


Figure 14. 0.1Hz to 10Hz V_{OUT} Peak-to-Peak Noise for Coarse Offset Adjust = −56mV, Gain = 1152, V_{IN} = +57mV, CLK_CFG = '11', V_{NPP} (RTI) = 42µV_{PP}.

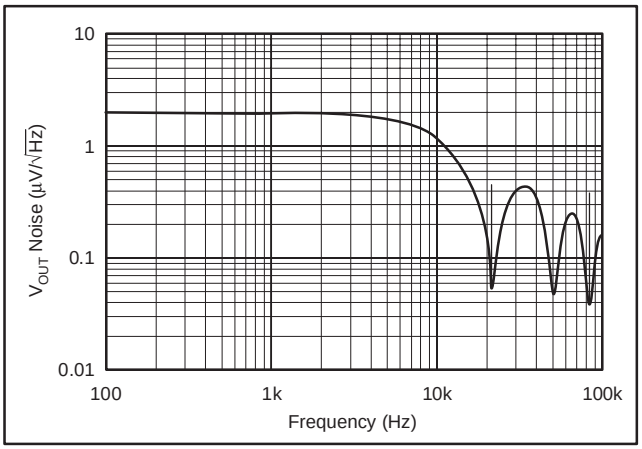


Figure 16. V_{OUT} Noise Spectrum for Coarse Offset Adjust = −56mV, Gain = 1152, V_{IN} = +57mV, CLK_CFG = '11'.

REFERENCE VOLTAGE

The PGA309 can be configured for use with an internal or external voltage reference. The reference voltage selected is used by the Zero DAC, Over/Under-Scale Limit, Coarse Offset Adjust DAC, Temp ADC, and Bridge Excitation Linearization Loop. Figure 17 depicts the PGA309 reference circuit. If internal reference is selected, either 2.5V or 4.096V can be chosen. In this mode, a typically better than 2% initial accuracy, low drift, ±10ppm/°C reference is available for internal and external use. Up to 5mA can be supplied out through the REF_{IN}/REF_{OUT} pin in internal mode. If external reference mode is chosen, then an external reference from +2.5V to $+V_{SA}$ may be applied to the REF_{IN}/REF_{OUT} pin. During power-on, the external reference mode is selected. Table 3 details the Register 3 bits (9:8) used for the reference mode selections.

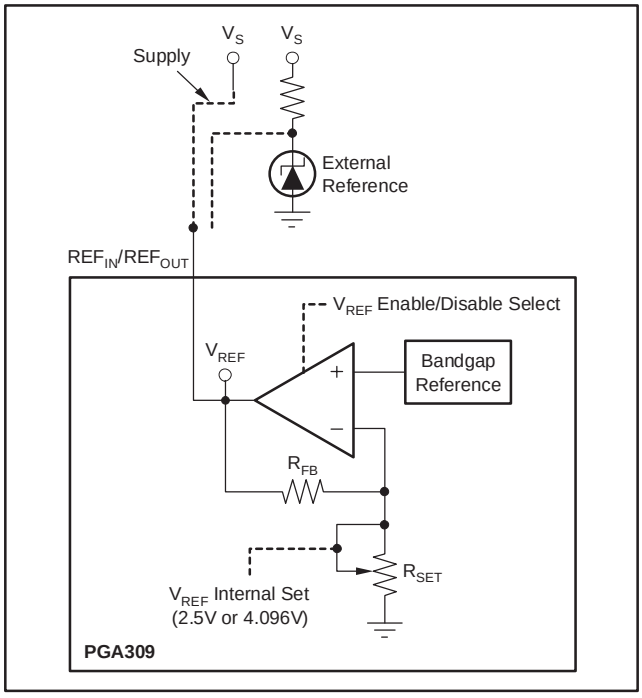


Figure 17. PGA309 Reference Circuit

D9 RS	D8 REN	V_{REF}	REFERNCE CONFIGURATION
X	0	REF_{IN}/REF_{OUT}	External Reference (disable internal reference)
0	1	4.096V	Internal Reference
1	1	2.5V	Internal Reference

Table 3. Register 3 Reference Control Bits

EEPROM CONTENT AND TEMPERATURE LOOKUP TABLE CALCULATION

The PGA309 has been tested to operate with EEPROM parts Microchip 24LCxx and 24AAxx.

The first 16 bytes of the external EEPROM contain the programmed EEPROM flag and PGA309 configuration data for registers 3, 4, 5, and 6. The word at address 14 contains the checksum for this section, Checksum1.

Table 4 details the EEPROM content.

EEPROM ADDRESS	CONTENT (ALL 2-BYTE VALUES)
0	Hex 5449 = 'TI': EEPROM Programmed Flag
2	Not used, but included in the Checksum1; available for user data.
4	Not used, but included in the Checksum1; available for user data.
6	Value for Register 3, Reference Control and Linearization
8	Value for Register 4: PGA Coarse Offset and Gain/Output Amplifier Gain
10	Value for Register 5: PGA Configuration and Over/Under-Scale Limit
12	Value for Register 6: Temp ADC Control
14	Checksum1= *0xFFFF − SUM(Addr0 to Addr12)*, 16-bit wide, carryover bits are ignored
16 to 21	Begin Lookup Table: T0; Z0; G0
—	Up to 16 more Lookup Table entries with slope coefficients: T_i; ZM_i; GM_i; optional
—	End of Lookup Table, 3 words: hex 7FFF; 0000; Checksum2 Checksum2 = *0xFFFF − SUM(Addr16 to Current address)*, includes 7FFF and 0000; 16-bit words; carryover bits are ignored

Table 4. EEPROM Content Table

Addresses 16 and higher of the EEPROM contain the temperature coefficient Lookup Table for the Zero DAC (Fine Offset Adjust) and Gain DAC (Fine Gain Adjust). There can be up to 17 temperature index values with corresponding scale factors for the Gain DAC and Zero DAC. The values in the lookup table represent the points on the piecewise linear curves that compensate sensor span and offset drifts. The DAC values are linearly interpolated between the points.

T0, T1, T2 … Tx (where $x \leq 16$) are the temperature index values in the lookup table. These are output results from the Temp ADC. The values must be monotonically increasing from minimum to maximum for the lookup table to function correctly. Note that this does not necessarily correspond to increasing temperature. For example, if a diode voltage is being measured by the Temp ADC, its readings will be

decreasing with temperature. However, the Lookup Table must still be built from minimum Temp ADC reading to the maximum. The data format for Tx is 16-bit data with a format dependent upon which Temp ADC mode is selected (see Register 6, Temperature ADC Control Register, for a detailed register description).

Z0 is the value of the Zero DAC setting for temperatures T0 and below. Z0 data format is unsigned 16-bit data. The equation for the Zero DAC value is:

$$Z_i = \left(\frac{V_{Zdesired}}{V_{REF}}\right) \cdot 65,536$$

G0 is the value of the Gain DAC setting for temperatures T0 and below. G0 data format is unsigned 16−bit data. The equation for the Gain DAC value is:

$$G_i = \left(Gain_{desired} - \frac{1}{3}\right) \cdot \frac{3}{2} \cdot 65,536$$

ZM1, ZM2 … ZMx are multiplying slope factors for each piecewise linear segment for the Zero Adjustment DAC. They are calculated based on the desired values Z1, Z2 … Zx (calculated same as Z0) of the Zero DAC for T1, T2 … Tx respectively. The equation for calculating the ZM_i slope factors is:

$$ZM_i = 256\frac{(Z_i - Z_{i-1})}{(T_i - T_{i-1})}$$

The ZMx scale factor of 256 is to format the decimal value for PGA309 internal binary arithmetic. These numbers are 16-bit, Two's Complement data format. See Table 5 for an example of the lookup table.

GM1, GM2 … GMx are multiplying slope factors for each piecewise linear segment for the Gain Adjustment DAC. The equation for calculating the GM_i slope factors is:

$$GM_i = 256\frac{(G_i - G_{i-1})}{(T_i - T_{i-1})}$$

The end of the Lookup Table is flagged by temperature index value T_{END} = 0x7FFF in the temperature index data. The ZME value of this entry is ignored but is included in the checksum. The ZME value should be set to zero. The GME value of this entry becomes Checksum2, the checksum for the second part of the EEPROM.

Table 5 shows an example Lookup Table and details the calculation of its values.

Figure 18 illustrates the concept of the Gain DAC temperature coefficients stored in the EEPROM according to Table 5. G0−G7 are exact desired settings at T0−T7, respectively, for the Gain DAC. GM1−GM7 are the slopes of the piecewise linear curves that connect G0−G1, G1−G2, G2−G3, G3−G4, G4−G5, G5−G6, and G6−G7. For this example, we wish to see how the lookup logic with interpolation algorithm of the PGA309 will accurately calculate the setting for the Gain DAC at T_{READ} = 25°C, which does not fall on an exact data point (Tx, Gx).

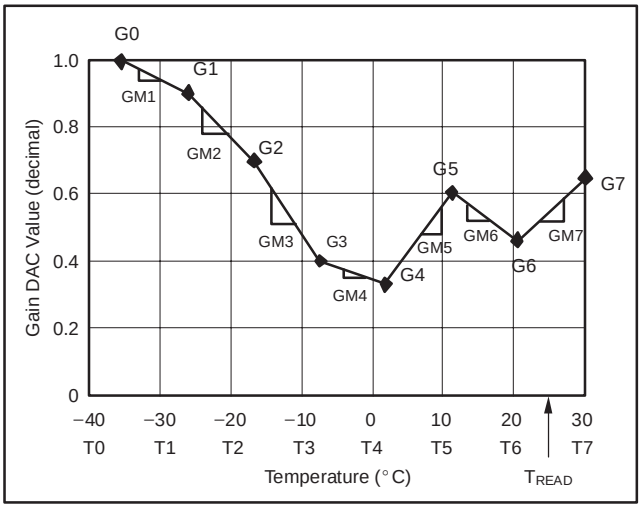


Figure 18. Gain DAC Temperature Coefficients—Definition Example

DESIRED VALUES IN LOOKUP TABLE				LOOKUP TABLE (DECIMAL)			LOOKUP TABLE (HEX)		
POINT#	TEMP (°C)	VZERO (V)	GFINE (V/V)	ADC OUT	ZERO COEF	GAIN COEF	TEMP	ZM	GM
0	−40	0.1	1	−640	1311	65535	FD80	051F	FFFF
1	−30	0.2	0.9	−480	2096	−15726	FE20	0830	C292
2	−20	1	0.7	−320	16778	−31458	FEC0	418A	851E
3	−10	1	0.4	−160	0	−47186	FF60	0000	47AE
4	0	2	0.33333	0	20971	−10486	0000	51EB	D70A
5	10	1.5	0.6	160	−10485	41942	00A0	D70B	A3D6
6	20	1	0.4756	320	−10486	−19566	0140	D70A	B392
7	30	2	0.6543	480	20971	28107	01E0	51EB	6DCB
End	…	…	…	32767	0	Checksum	7FFF	0	B622

Table 5. Lookup Table Example: V_{REF} = 5V, Internal Temperature Sensing Mode

Table 6 outlines the algorithm used inside the PGA309 for linear interpolation and calculation of the Gain DAC setting for T_{READ} = 25°C. Table 5 shows example calculations for GM1−GM7 at T1−T7 given values for G1−G7. The starting values (T0 and G0) are also defined. From the plot in Figure 18, it is shown that at the currently read temperature (T_{READ} = 25°C), there should be a mathematical value of 0.56495 for the Gain DAC setting if the PGA309 lookup logic with interpolation algorithm is working correctly. Each time the Temp ADC does a conversion, it reads the entire external EEPROM. The first half, as described previously, is dedicated to fixed setup parameters for the PGA309 that do not change with temperature. As the PGA309 reads the second half of the EEPROM, it begins a running calculation of the Gain DAC setting with temperature (the PGA309 runs a similar calculation for the Zero DAC setting). This model includes an accumulator named GAC (G Accumulator). When the PGA309 reads T0, the initial Gain DAC setting (G0) is stored in GAC0 (GAC at T0 read). Next, T1 is read and slope GM1 is multiplied by the difference between T1 and T0 and added to GAC0 to form the new accumulator value, GAC1 (GAC at T1 read). This process continues in a sequential fashion as the PGA309 reads through the entire Lookup Table. As each temperature index value (Tx) is read, it is compared against ADC_{READ}, the current Temp ADC conversion result. If Tx > T_{READ}, it is known that T_{READ} is between Tx and T(x−1). In this example, it occurs as T7 is read. The accumulator contents, GAC6 (GAC at T6), are modified by the addition of (T_{READ} − T6)(GM7). The resulting GAC_ADC_{READ} is the linearly interpolated setting for the Gain DAC at T_{READ} = 25°C. The rest of the EEPROM is still read for error checking with Checksum2 at the end of the Lookup Table.

The Zero DAC ZMx multiplying scale factors for temperature correction are computed the same as those discussed for the Gain DAC. The internal PGA309 lookup logic with interpolation algorithm calculates the Zero DAC setting for T_{READ} in the same manner as outlined for the Gain DAC.

Please note that the values of the Gain DAC and Zero DAC must always be in their respective ranges to produce correct results:

$$2\%V_{REF} \le ZeroDAC \le 98\%\ V_{REF}$$

$$0.33333\ (V/V) \le GainDAC \le 1\ (V/V)$$

FAULT MONITOR

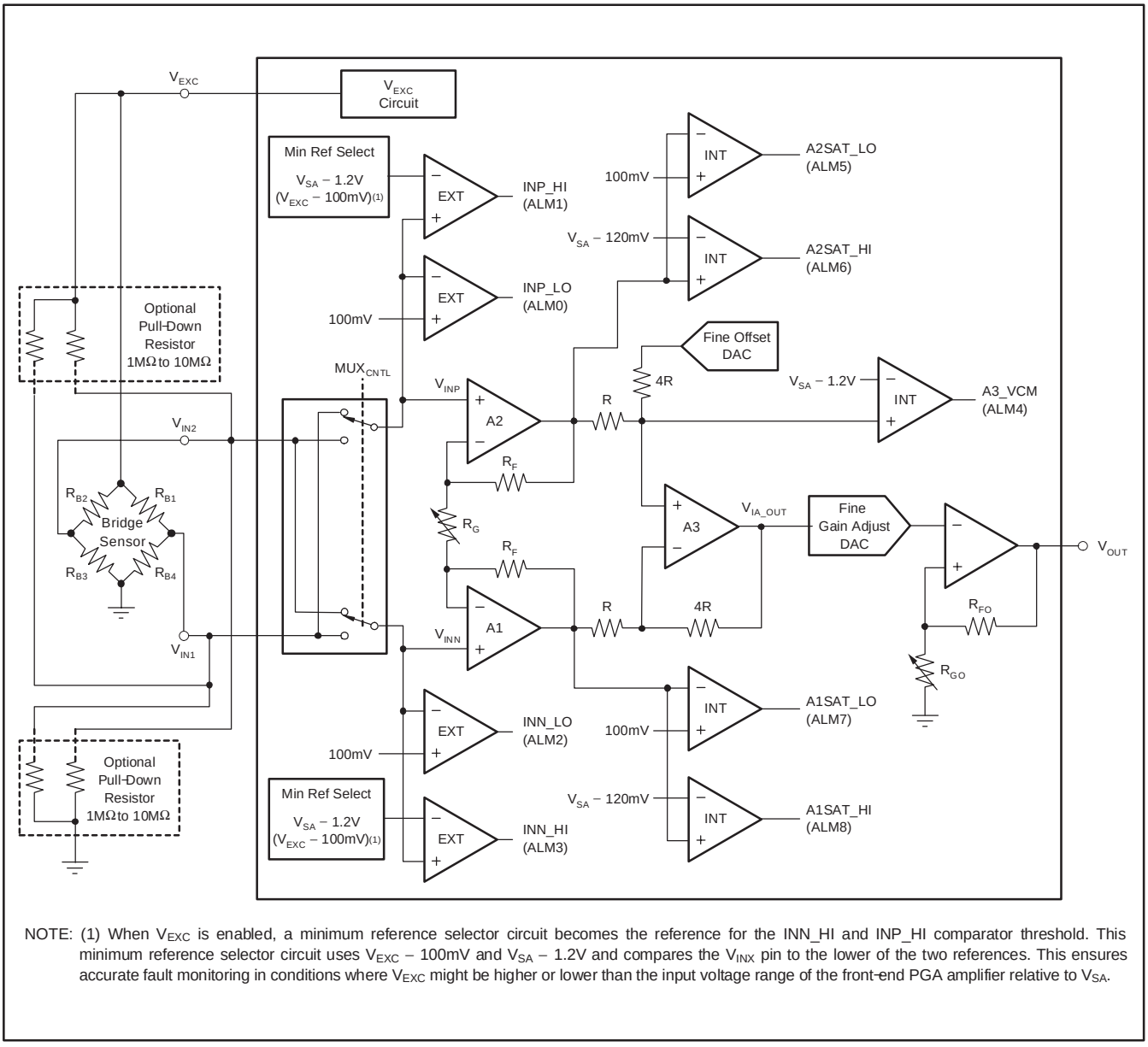
Monitoring of fault condition sensors is provided on the PGA309 through nine internal comparators. Refer to Figure 19. These comparators are grouped into two sets: Internal Fault Comparators and External Fault Comparators. In Figure 19, these are denoted as EXT for those in the External Fault Comparator group and by INT for those in the Internal Fault Comparator group.

The external fault comparators are used to monitor proper operation of the bridge sensor and report input fault conditions. Table 7 enumerates the possible fault cases for a bridge sensor and the associated fault comparator outputs for each fault condition. Due to the extremely low input bias currents of the PGA309, if fault detection of floating inputs (sensor disconnected entirely from one or both of the PGA309 inputs) is to be accurately reported,

CALCULATION ALGORITHM FOR GAIN VALUE AT T = 25°C (TEMP ADC = 0X0190 → 400 DECIMAL)					
POINT#	**TEMP INDEX (DECIMAL)**	**GAIN INDEX (DECIMAL)**	**GAC CALCULATION**	**RUNNING GAC VALUE (DECIMAL)**	**ACTUAL DAC GAIN (V/V)**
0	−639	65535	GAC0 = G0	65535	0.99999
1	−479	−15725	GAC1 = GAC0 + GM1(T1 − T0)	55707	0.90001
2	−319	−31457	GAC2 = GAC1 + GM2(T2 − T1)	36046	0.70001
3	−159	18350	GAC3 = GAC2 + GM3(T3 − T2)	47515	0.81668
4	0	−10485	GAC4 = GAC3 + GM4(T4 − T3)	41003	0.75044
5	160	−23593	GAC5 = GAC4 + GM5(T5 − T4)	26257	0.60043
6	320	−19565	GAC6 = GAC5 + GM6(T6 − T5)	14029	0.47604
7	480	28107	*T7 > ADC_{READ} → YES!* $GACT_{READ}$ = GAC6 + GM7(ADC_{READ} − T6)	**22812**	**0.56539**
end	32767	The Lookup Table is read to the end to verify Checksum2			
NOTE: GAC = G Accumulator: running total that is computed starting with G0, at T0, every time the Temp ADC converts a new value, which causes a new calculation update cycle to occur by reading the EEPROM from beginning to end.					

Table 6. Gain DAC Temperature Coefficients—Calculation Example

it is necessary to add either pull-up or pull-down resistors to each of these inputs (V_{IN1} and V_{IN2}), shown in Figure 19 as optional. The value of these resistors can be between 1MΩ and 10MΩ in order to minimize signal loading of the bridge sensor's output. Offset and other errors from these optional resistors will be cancelled out during the PGA309 + sensor calibration. Table 8 itemizes the special cases for floating inputs on the PGA309 when using pull-up resistors. Table 9 lists the special cases for floating inputs on the PGA309 when using pull-down resistors. All other fault cases not listed as special cases are the same as those detailed in Table 7.



NOTE: (1) When V_{EXC} is enabled, a minimum reference selector circuit becomes the reference for the INN_HI and INP_HI comparator threshold. This minimum reference selector circuit uses V_{EXC} − 100mV and V_{SA} − 1.2V and compares the V_{INX} pin to the lower of the two references. This ensures accurate fault monitoring in conditions where V_{EXC} might be higher or lower than the input voltage range of the front-end PGA amplifier relative to V_{SA}.

Figure 19. PGA309 Fault Monitor Circuitry

CASE	V_{IN2} (V_{INN}) (V)	V_{IN1} (V_{INP}) (V)	V_{IA_OUT} (V)	LOGIC LEVEL OUTPUTS				COMMENTS
				INN_HI (ALM3)	INN_LO (ALM2)	INP_HI (ALM1)	INP_LO (ALM0)	
Normal	1.7	1.7	Linear	0	0	0	0	
RB1 Open	1.7	0	~0	0	0	0	1	
RB2 Open	0	1.7	$\sim V_{SA}$	0	1	0	0	
RB3 Open	3.4	1.7	~0	1	0	0	0	
RB4 Open	1.7	3.4	$\sim V_{SA}$	0	0	1	0	
RB1 Short	1.7	3.4	$\sim V_{SA}$	0	0	1	0	
RB2 Short	3.4	1.7	~0	1	0	0	0	
RB3 Short	0	1.7	?	0	1	0	0	
RB4 Short	1.7	0	~0	0	0	0	1	
Open Sensor GND	3.4	3.4	~0	1	0	1	0	
Open Sensor V_{EXC}	0	0	~0	0	1	0	1	
VEXC Short GND	0	0	~0	1(1)	1	1(1)	1	
V_{IN1} (V_{INP}) Open(2)	1.7	$\sim V_{SA}-0.7$	$\sim V_{SA}$	0	0	0	0	Under-scale limit on V_{OUT}, no fault detect—Int or Ext
V_{IN2} (V_{INN}) Open(2)	$\sim V_{SA}-0.7$	1.7	~0	0	0	0	0	Over-scale limit on V_{OUT}, no fault detect—Int or Ext
V_{IN1} (V_{INP}) Short GND	1.7	0	~0	0	0	0	1	
V_{IN2} (V_{INN}) Short GND	0	1.7	$\sim V_{SA}$	0	1	0	0	
V_{IN1} (V_{INP}) Short V_{EXC}	1.7	3.4	$\sim V_{SA}$	0	0	1	0	
V_{IN2} (V_{INN}) Short V_{EXC}	3.4	1.7	~0	1	0	0	0	
V_{IN1} (V_{INP}), V_{IN2} (V_{INN}) Open(2)	$\sim V_{SA}-0.7$	$\sim V_{SA}-0.7$	Linear?	0	0	0	0	Typically drifts to over-scale limit slowly; no Ext Faultdetect (ALM7), Int Fault set = A1 Sat Low
V_{IN1} (V_{INP}), V_{IN2} (V_{INN}) Short GND	0	0	$\sim V_{SA}$	0	1	0	1	
V_{IN1} (V_{INP}), V_{IN2} (V_{INN}) Short V_{EXC}	3.4	3.4	~0	1	0	1	0	

NOTE: V_{SA} = +5V, V_{REF} = +4.096V, K_{EXC} = 0.83, K_{LIN} = 0, and V_{EXC} = 3.4V.
(1) Typically, a logic 1, but not guaranteed by design and nature of fault.
(2) Accurate detection of these faults requires a pull-up or pull-down resistor on each input (V_{IN1} and V_{IN2}).

Table 7. Bridge Sensor Faults and Fault Comparator States—V_{IN1} and V_{IN2}: no pull-up or pull-down resistors

SPECIAL CASE(1)	V_{IN2} (V_{INN}) (V)	V_{IN1} (V_{INP}) (V)	V_{IA_OUT} (V)	LOGIC LEVEL OUTPUTS			
				INN_HI (ALM3)	INN_LO (ALM2)	INP_HI (ALM1)	INP_LO (ALM0)
V_{IN1} (V_{INP}) Open	1.7	V_{EXC}	$\sim V_{SA}$	0	0	1	0
V_{IN2} (V_{INN}) Open	V_{EXC}	1.7	~0	1	0	0	0
V_{IN1} (V_{INP}), V_{IN2} (V_{INN}) Open	V_{EXC}	V_{EXC}	~0	1	0	1	0

NOTE: V_{SA} = +5V, V_{REF} = +4.096V, K_{EXC} = 0.83, K_{LIN} = 0, and V_{EXC} = 3.4V.
(1) All other cases not listed are the same as those for Table 7.

Table 8. Bridge Sensor Faults and Fault Comparator States—V_{IN1} and V_{IN2}: 10MΩ pull-up resistors to V_{EXC}

SPECIAL CASE(1)	V_{IN2} (V_{INN}) (V)	V_{IN1} (V_{INP}) (V)	V_{IA_OUT} (V)	LOGIC LEVEL OUTPUTS			
				INN_HI (ALM3)	INN_LO (ALM2)	INP_HI (ALM1)	INP_LO (ALM0)
V_{IN1} (V_{INP}) Open	1.7	~0	$\sim V_{SA}$	0	0	0	1
V_{IN2} (V_{INN}) Open	~0	1.7	~0	0	1	0	0
V_{IN1} (V_{INP}), V_{IN2} (V_{INN}) Open	~0	~0	~0	0	1	0	1

NOTE: V_{SA} = +5V, V_{REF} = +4.096V, K_{EXC} = 0.83, K_{LIN} = 0, and V_{EXC} = 3.4V.
(1) All other cases not listed are the same as those for Table 7.

Table 9. Bridge Sensor Faults and Fault Comparator States—V_{IN1} and V_{IN2}: 10MΩ pull-down resistors to GND

When V_{EXC} is enabled, external fault comparators INP_HI and INP_LO have a minimum reference selector circuit that selects between a typical trip point of either V_{EXC} – 100mV or V_{SA} – 1.2V. This ensures accurate fault monitoring in conditions where the linearization circuitry increases V_{EXC}, and the bridge sensor has fault conditions that violate the input voltage range, relative to V_{SA}, of the front-end PGA in the PGA309. If V_{EXC} is disabled, these comparators default to the V_{SA} – 1.2V threshold.

The internal fault comparators are used to monitor the front-end PGA internal nodes of the PGA309 (see Figure 19). When PGA309 + Sensor calibration is in process, it is crucial to have the internal comparator group enabled because it can alert the user to an internal node violation. Such a violation may still yield a voltage within the expected linear output range, but it will not be an accurate one. Each of the front-end amplifiers, A1 and A2, of the front-end PGA have their outputs monitored for both saturation to the positive supply or to ground. If either of these comparators trips during calibration, it is an indication of an out-of-range scaling condition either due to the incorrect front-end PGA gain select or coarse offset adjust. The A3 amplifier in the front-end PGA is also monitored for common-mode violations as can occur if the Zero DAC is combined incorrectly with the front-end PGA gain select.

Each individual internal and external fault comparator can be read through one of the digital interfaces: Two-Wire or One-Wire. The current results are stored in Register 8—Alarm Status Register. When the PGA309 output is enabled, the value of the Alarm Status Register reflects the current state of the fault comparators. When V_{OUT} is disabled, the value in the register is the comparator status immediately before the output was disabled. This allows for easier identification and debugging of the Three-Wire mode (PRG shorted to V_{OUT}). See the *One-Wire Operation with PRG Shorted to V_{OUT}* section for details. In addition, each group of comparators, internal fault and external fault, can be programmed such that if any comparator in their respective group is logic high, indicating a fault, the PGA309 output (V_{OUT}) will be forced to a fault indicating voltage level of either positive (V_{SA} − 0.1V max with a 10kΩ load) or negative (0.1V max with a 10kΩ load). The logic for this is shown in Figure 20.

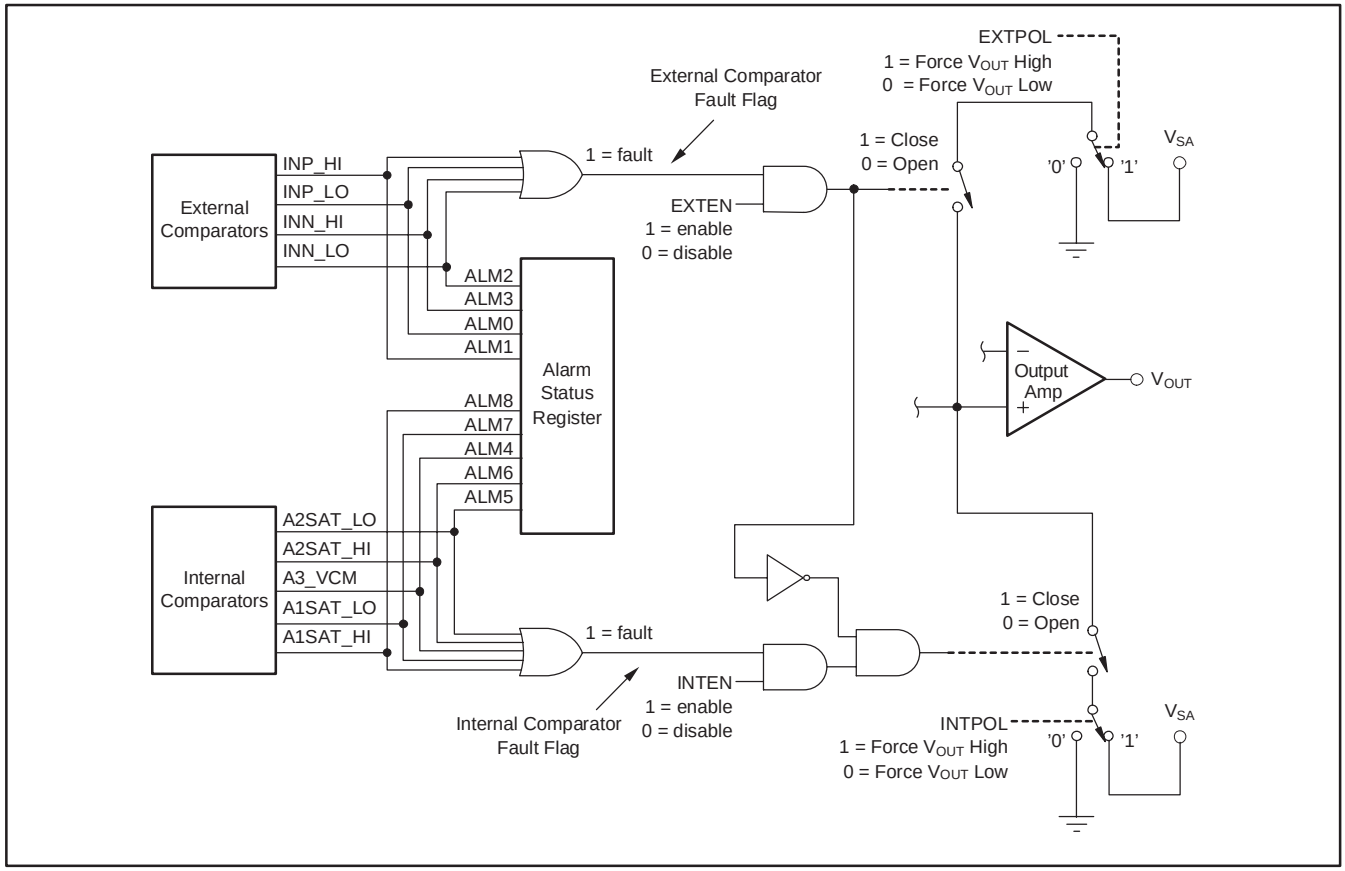


Figure 20. Fault Monitor Comparator Logic

Configuration for the fault monitor comparator logic is provided in Register 5—PGA Configuration and Over/Under Scale Limit. The individual comparator outputs in each group are combined to generate an Internal Comparator Fault flag and an External Comparator Fault flag. For the External Comparator group (EXTEN), Register 5 (bit 11) enables or disables whether the External Comparator Fault flag will be sent forward to force V_{OUT} to a fault indication state. For the Internal Comparator group (INTEN), Register 5 (bit 10), enables or disables whether the Internal Comparator Fault flag will be sent forward to force V_{OUT} to a fault indication state. For each of the comparator groups, there is programmability of the fault indication state on V_{OUT} (either V_{SA} or GND). INTPOL, Register 5 (bit 8), selects this state for the Internal Comparator group and EXTPOL, Register 5 (bit 9) selects for the External Comparator group. The External Comparator Fault flag has priority over the Internal Comparator Fault flag, as shown in Figure 20. For example, if the Internal Fault Comparator group is set to force V_{OUT} low and the External Fault Comparator group is set to force V_{OUT} high, and both groups detect a fault (which is possible if both are enabled), then the External Fault Comparator group prevails and V_{OUT} is forced high. This is to ensure that for most real-world applications, a critical sensor fault would be reported as priority over an internal node violation. Assuming there is a valid linear output on V_{OUT} at the time of a detected fault, the fault logic always prevails (if enabled), and will override the linear output to indicate a fault on V_{OUT} as positive or negative V_{OUT} saturation.

OVER/UNDER SCALE

The Over-Scale and Under-Scale Limit circuit provides a programmable upper and lower clip limit for the PGA309 output voltage. This circuit can be enabled by setting Register 5, bit D6 to D1. When combined with the Fault Monitor circuitry, system diagnostics can be performed to determine if a conditioned sensor is defective or if the process being monitored by the sensor is out of range. Figure 21 details the key sections of the Over-Scale and Under-Scale Limit circuit. The selected PGA309 V_{REF} is divided down by a precision resistor string to form the over-scale and under-scale thresholds, as shown in Table 10 and Table 11. Register 5 bits [5:0] set the desired thresholds. These resistor ratios are extremely accurate and produce no significant initial or temperature errors. As shown in Figure 21, there are two separate comparators: over-scale and under-scale, which use the over-scale or under-scale threshold, respectively, and determine where the PGA309 output (V_{OUT}) will be clipped. The dominant errors in the Over-Scale and Under-Scale Limit circuit are in the comparator offsets and offset temperature drifts.

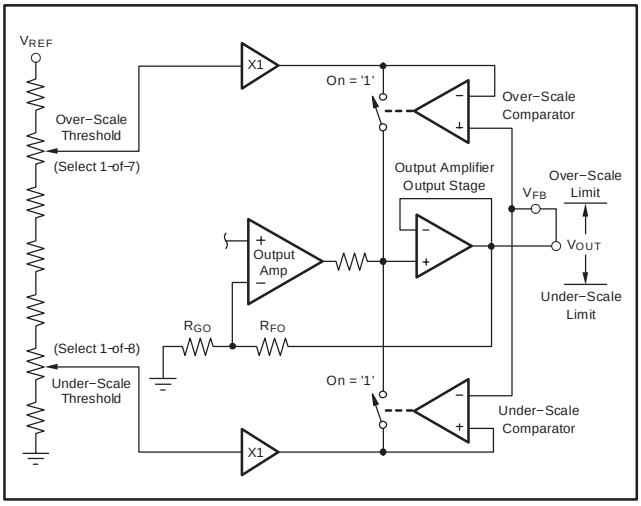


Figure 21. Over-Scale and Under-Scale Limit Circuit

HL2 [5]	HL1 [4]	HL0 [3]	OVER-SCALE THRESHOLD (V)	OVER-SCALE THRESHOLD
0	0	0	4.854	0.9708 V_{REF}
0	0	1	4.805	0.9610 V_{REF}
0	1	0	4.698	0.9394 V_{REF}
0	1	1	4.580	0.9160 V_{REF}
1	0	0	4.551	0.9102 V_{REF}
1	0	1	3.662	0.7324 V_{REF}
1	1	0	2.764	0.5528 V_{REF}
1	1	1	Reserved	—

Table 10. Under−Scale Threshold Selections (Register 5 Bits [5:0]). V_{REF} = +5V.

LL2 [2]	LL1 [1]	LL0 [0]	UNDER-SCALE THRESHOLD (V)	UNDER-SCALE THRESHOLD
0	0	0	0.127	0.02540 V_{REF}
0	0	1	0.147	0.02930 V_{REF}
0	1	0	0.176	0.03516 V_{REF}
0	1	1	0.196	0.03906 V_{REF}
1	0	0	0.225	0.04492 V_{REF}
1	0	1	0.254	0.05078 V_{REF}
1	1	0	0.274	0.05468 V_{REF}
1	1	1	0.303	0.06054 V_{REF}

Table 11. Over−Scale Threshold Selections (Register 5 Bits [5:0]). V_{REF} = +5V.

The design considerations in using the Over-Scale and Under-Scale Limit circuit are best understood through a definition by example.

Example: Over/Under-Scale Calculation

Given: Absolute Scale System—PGA309 connected to a system ADC (see Figure 22)
System ADC Reference: V_{REF} ADC = 4.096V
PGA309 Reference: V_{REF} = 4.096V (use internal reference)
Operating Temperature Range: −40°C to +125°C
PGA309 V_{SA}, V_{SD} = +5V
External Fault Monitor; Trip High when Fault Detected

Find: Recommended levels to allow for Over−Scale and Under−Scale Limits as well as Fault Detection.
A) Over−Scale Limit
B) Under−Scale Limit
C) Useable Linear PGA309 Output Range
D) System ADC Trip Points:
Over-Scale
Under-Scale
Fault Detect

Solution:

1. Analyze the worst case offset errors on the over-scale and under-scale comparators over the operating temperature range. Table 12 contains key electrical characteristics needed for this computation.

Over-Scale Comparator Offset Calculation:

Over-Scale Temperature Drift:
−40°C to 25°C: −24.05mV = (+0.37mV/°C)(−40°C − 25°C)
25°C to +125°C: +37.00mV = (+0.37mV/°C)(+125°C − 25°C)

Over-Scale Offset Min and Max:
V_{OS} min = +6mV −24.05mV = −18.05mV
V_{OS} max = +114mV + 37.00mV = +151.00mV

Under-Scale Comparator Offset Calculation:

Under-Scale Temperature Drift:
−40°C to 25°C: +9.75mV = (−0.15mV/°C)(−40°C − 25°C)
25°C to +125°C: −15.00mV = (−0.15mV/°C)(+125°C − 25°C)

Under-Scale Offset Min and Max:
V_{US} min = −7mV + 9.75mV = −2.75mV
V_{US} max = −93mV −15.00mV = −108mV

2. Analyze the worst-case change in V_{REF} over the operating temperature range.

V_{REF} Temperature Drift:
−40°C to +125°C: [($\pm$10ppm/°C)/(1e6)](+125°C− −40°C)V_{REF} = $\pm$0.00165 V_{REF}

V_{REF} Min and Max:
V_{REF} min = 4.00V – (0.00165)(4.00V) = 3.9934V
V_{REF} max = 4.14V + (0.00165)(4.00V) = 4.1466

3. Calculate the over-scale and under-scale min and max trip points over the operating temperature range for each over-scale and under-scale threshold (refer to Table 13).

Over-Scale Min and Max Trip Points:
OS min = V_{REF} min (OS ratio) − V_{OS} min
OS max = V_{REF} max (OS ratio) + V_{OS} max

Under-Scale Min and Max Trip Points:
US min = V_{REF} min (US ratio) − V_{US} min
US max = V_{REF} max (US ratio) + V_{US} max

4. From the over-scale and under-scale min and max trip point calculations, choose the best selection that will allow for the optimum system ADC range budget (see Figure 23). For this example, the PGA309 is scalable for a linear output of 8% to 92% of the system ADC reference. In addition, we can set reasonable trip points for detecting over-scale limit, under-scale limit, and fault detect.

5. Check that the PGA309 V_{OUT} can support the voltage swings defined in the SystemADC range budget. Table 14 confirms that for our example the PGA309 V_{OUT} can meet the limiting conditions for our desired scaling.

Since the PGA309 + sensor is usually calibrated together as a system, the over-scale and under-scale limits can be measured per device at the operating temperature extremes, and the final limits adjusted as desired for optimum scaling. In a ratiometric scaled system, the reference error will not need to be included in the over-scale and under-scale trip point calculations.

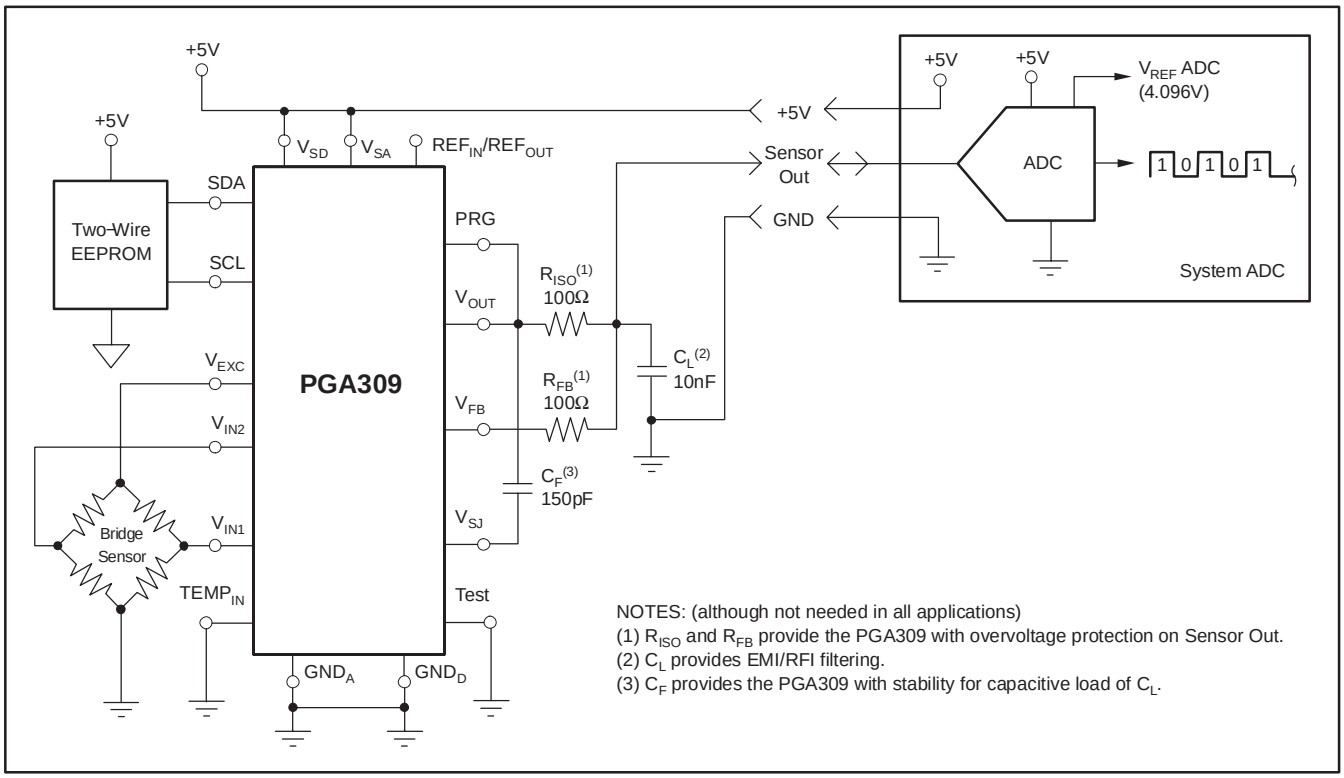


Figure 22. Absolute Scale System—PGA309 Connected to a System ADC

PARAMETER	MIN	TYP	MAX	UNITS
Over-Scale Comparator Offset	+6	+60	+114	mV
Over-Scale Comparator Offset Drift		+0.37		mV/°C
Under-Scale Comparator Offset	−7	−50	−93	mV
Under-Scale Comparator Offset Drift		−0.15		mV/°C
V_{REF2}	4.00	4.096	4.14	V
V_{REF2} Drift		+10		ppm/°C

Table 12. Electrical Characteristics for Over-Scale and Under-Scale Comparators and V_{REF}

THRESHOLD U = UNDER-SCALE O = OVER-SCALE	THRESHOLD RATIO TO V_{REF}	MIN TRIP (V)	MIN TRIP (%V_{REF} ADC)	MAX TRIP (V)	MAX TRIP (%V_{REF} ADC)	TYP TRIP (V)	TYP TRIP (%V_{REF} ADC)
U7	*0.0605*	*0.1300*	*3.1741*	*0.2500*	*6.1044*	*0.1900*	*4.6392*
U6	0.0547	0.1066	2.6028	0.2257	5.5111	0.1662	4.0569
U5	0.0508	0.0910	2.2225	0.2096	5.1163	0.1503	3.6694
U4	0.0449	0.0676	1.6512	0.1853	4.5231	0.1264	3.0871
U3	0.0391	0.0442	1.0799	0.1610	3.9298	0.1026	2.5049
U2	0.0352	0.0287	0.6997	0.1448	3.5350	0.0867	2.1173
U1	0.0293	0.0053	0.1283	0.1205	2.9418	0.0629	1.5351
U0	0.0254	−0.0103	−0.2519	0.1043	2.5470	0.0470	1.1475
O6	0.5528	2.2164	54.1101	2.1320	52.0505	2.1742	53.0803
O5	0.7324	2.9336	71.6203	2.8767	70.2324	2.9051	70.9263
O4	0.9102	3.6436	88.9549	3.6140	88.2321	3.6288	88.5935
O3	0.9160	3.6668	89.5204	3.6380	88.8192	3.6524	89.1698
O2	0.9394	3.7602	91.8018	3.7351	91.1881	3.7476	91.4949
O2	0.9610	3.8465	93.9077	3.8246	93.3748	3.8355	93.6412
O0	*0.9708*	*3.8856*	*94.8631*	*3.8653*	*94.3669*	*3.8754*	*94.6150*

Table 13. Over-Scale and Under-Scale Min and Max Trip Point Calculations

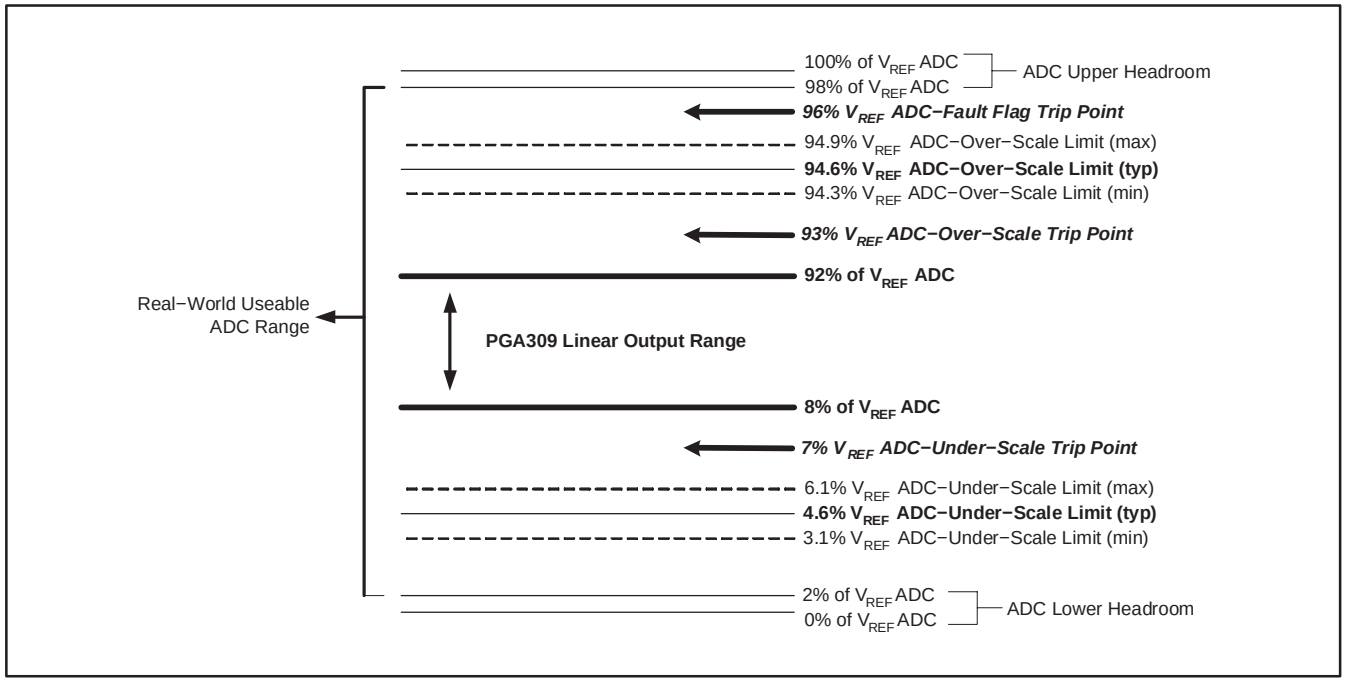


Figure 23. System ADC Range Budget for Over-Scale, Under-Scale, and Linear Output

LIMITING CONDITION	PGA309 V_{OUT} (V)	PGA309 V_{OUT} LIMIT (V)
96% VREF ADC—Fault Flag Trip Point	3.93216	4.9
3.1% VREF ADC—Under-Scale Limit (min)	0.126976	0.1
NOTE: V_{REF} ADC = 4.096V, V_{SA} = 5V		

Table 14. PGA309 V_{OUT} Limits for System ADC Range Budget

LINEARIZATION FUNCTION

Many bridge sensors have an inherent nonlinearity of their output with applied pressure. Figure 24 illustrates a typical nonlinearity correction using the PGA309 linearization circuitry.

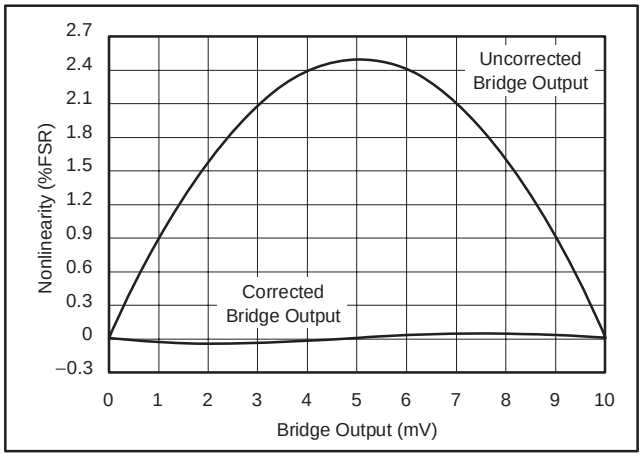


Figure 24. Bridge Pressure Nonlinearity Correction

The PGA309 contains a dedicated circuit for sensor voltage excitation and linearization, as shown in Figure 25. The linearization loop scales the selected V_{REF} and sums it together with a portion of the output voltage (V_{OUT}) to compensate for the bow-shaped nonlinearity of the bridge sensor output versus pressure. Using this technique, it is possible to compensate for parabolic nonlinearity resulting in up to to a 20:1 improvement over an uncompensated bridge output. If no linearity correction is desired, the sensor should be connected directly to the reference voltage (absolute system) or supply (ratiometric system). In applications not using linearization, both the V_{EXC} buffer and linearization DAC may be disabled by setting the appropriate Register 3 bits (10, 7:0) to '0'. This results in 50µA to 100µA of lower total quiescent current.

In systems where fault monitoring is critical, it is better to use V_{EXC} and K_{LIN} = 0. This optimizes fault monitoring comparator operation.

The output signal-dependence (V_{OUT} dependence) of the bridge excitation (V_{EXC}) adds a second-order term to the overall system transfer function (PGA309 + bridge sensor). The LinDAC (see Figure 26) scales a portion of V_{OUT} that is then summed with a scaled version of the reference voltage, V_{REF}. The LinDAC code can be set to compensate for each individual bridge sensor nonlinearity. As illustrated in Figure 26, there are two ranges available in the PGA309 linearization loop to accommodate a variety of sensor nonlinearities and V_{REF} combinations.

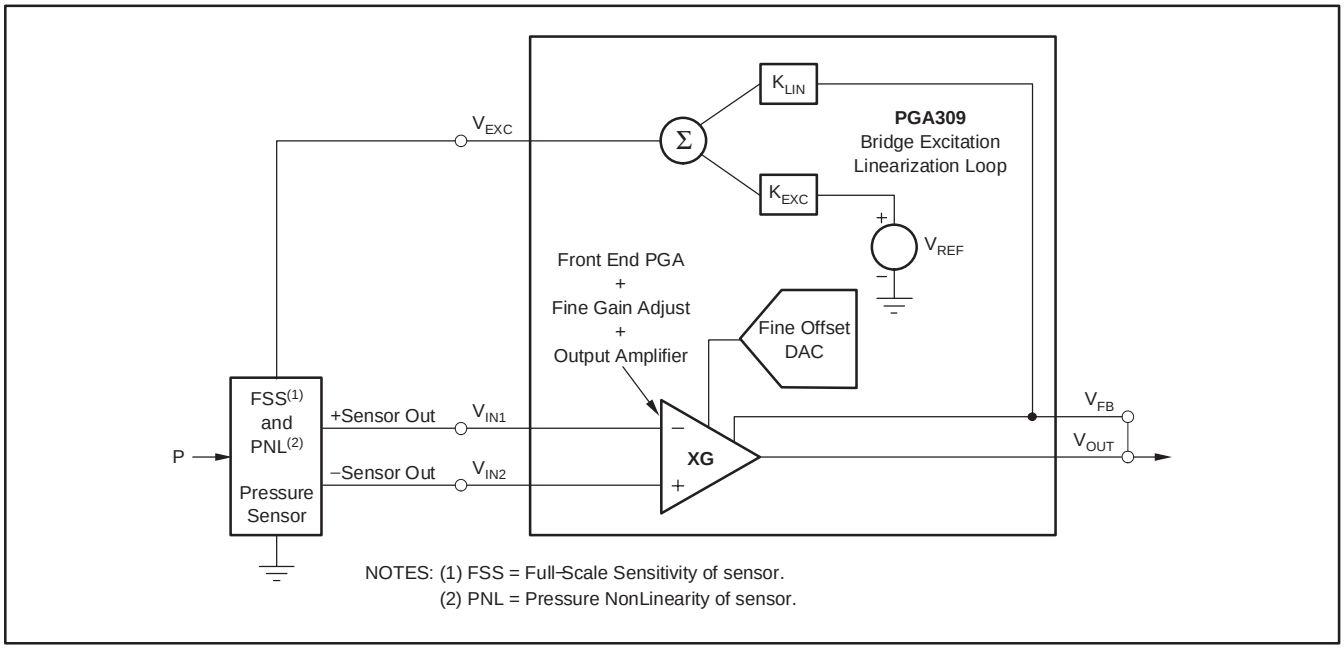


Figure 25. Bridge Excitation Linearization Loop

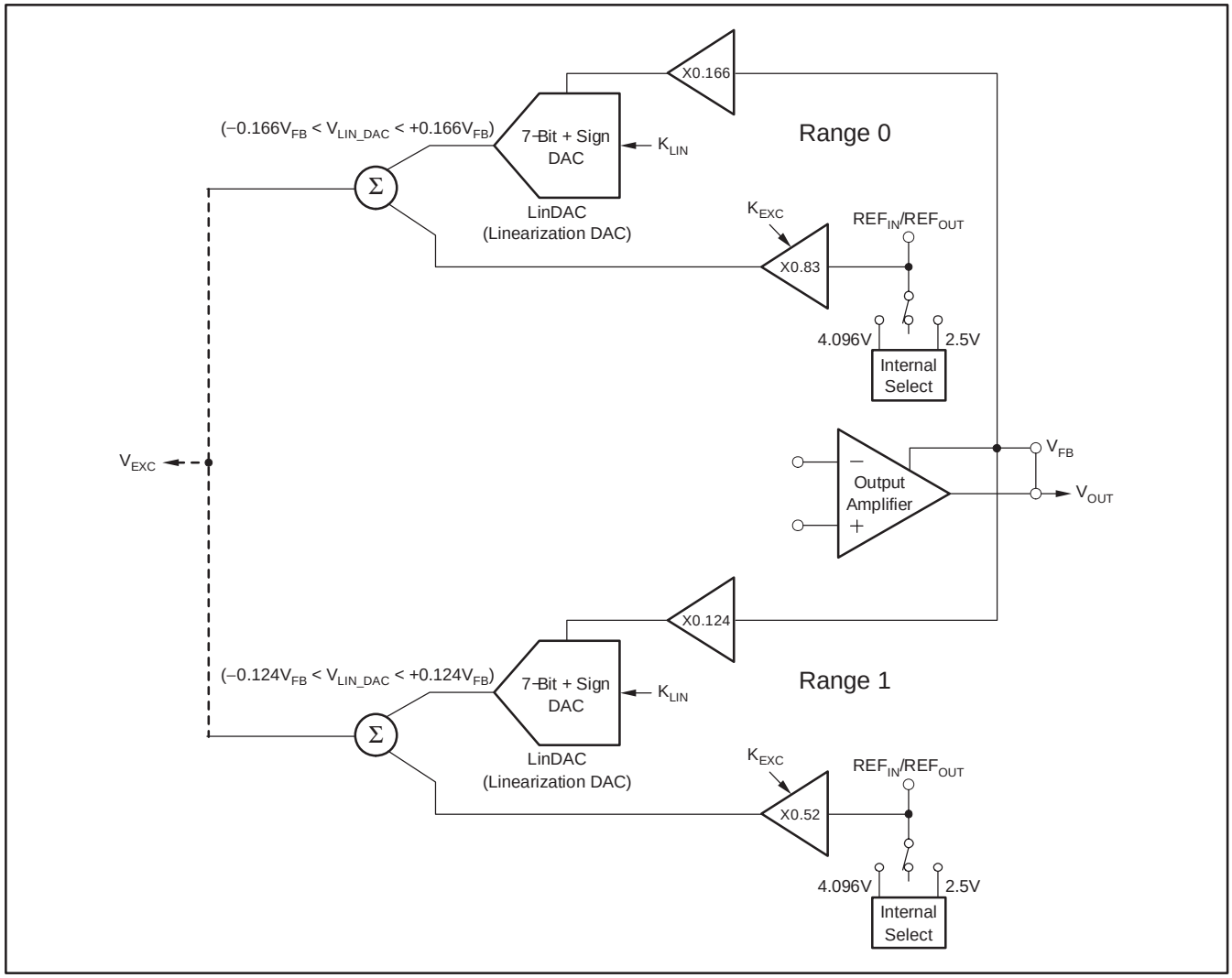


Figure 26. Linearization Circuitry

To determine the value for the LinDAC, also called the linearization coefficient K_{LIN}, the nonlinearity of the bridge sensor with constant excitation voltage must be known. The PGA309 linearization circuitry can only compensate for the parabolic-shaped portions of a sensor's nonlinearity with applied pressure. This nonlinearity is assumed to be constant over temperature or the temperature variations are assumed to be an insignificant contribution to the system error budget. For the typical PGA309 application, the K_{LIN} factor is not adjusted with temperature changes. Optimum correction occurs when maximum deviation from a linear output occurs at mid-scale (see Figure 27 and Figure 28). Sensors with nonlinearity curves similar to that of Figure 27, but not peaking at exactly mid-scale, can still be substantially improved. A sensor with an S-shaped nonlinearity curve (equal positive and negative nonlinearity) cannot be improved by using the PGA309 Linearization Circuitry.

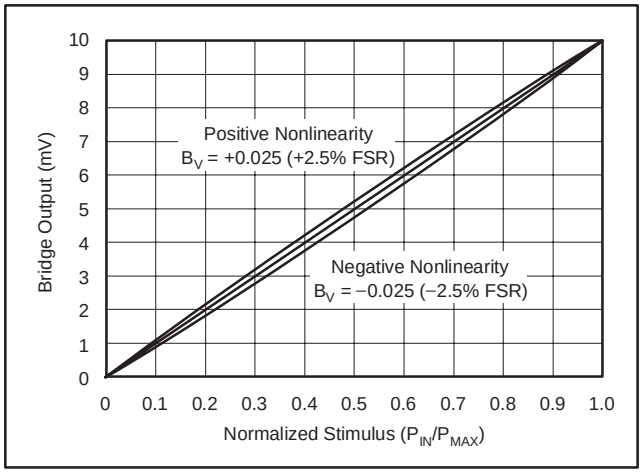


Figure 27. Parabolic Bridge Output vs Pressure

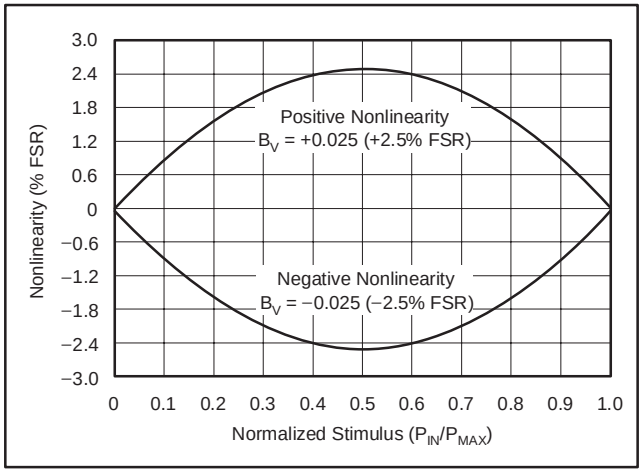


Figure 28. Parabolic Bridge Nonlinearity vs Pressure

Either positive or negative bridge nonlinearities can be compensated by the proper setting of the LinDAC polarity. To correct for positive bridge nonlinearity (upward bowing—see Figure 28), the LinDAC value should be set positive. For negative bridge nonlinearity (downward bowing—see Figure 28), set the LinDAC value negative.

The excitation voltage (V_{EXC}) directly scales the bridge sensor output and therefore affects the gain and offset when the linearization loop is used.

Key definitions and design equations for the linearization circuit are given in the next section.

System Definitions

P_{MIN}—Minimum System Input Pressure

P_{MAX}—Maximum System Input Pressure

FSS—Full Scale Sensitivity at P_{MAX} (that is, 5mV/V)

B_V—Bridge Nonlinearity with Applied Pressure. Maximum error at mid-scale input range (mid-pressure scale maximum error %FS: +2.5%FS = 0.025, −2.5% = −0.025)

P—Pressure Input

PNL—Nonlinear Pressure Output of Bridge with Linear Pressure Input P

$VOUT_{MIN}$—Minimum PGA309 V_{OUT} Voltage for P_{MIN} Bridge Input

$VOUT_{MAX}$—Maximum PGA309 V_{OUT} Voltage for P_{MAX} Bridge Input

V_{REF}—PGA309 Reference Voltage

K_{LIN}—PGA309 Linearization Coefficient

K_{EXC}—PGA Excitation Coefficient. Scale factor on V_{REF}.

K_P—Pressure Constant. Converts linear input pressure to nonlinear pressure detected by sensor. Referenced to full-scale input pressure.

G—Total PGA309 Gain of V_{OUT}/V_{IN}. G = Front-End PGA Gain + Fine Gain Adjust + Output Amplifier Gain.

V_{EXC}—Bridge Voltage Excitation (generated by PGA309 based on V_{REF}, K_{LIN}, K_{EXC}, V_{OUT})

Key Linearization Design Equations

Equation 1—Nonlinear pressure conversion for parabolic bridge sensor nonlinearity (B_V = positive for a positive parabolic nonlinearity, Bv = negative for a negative parabolic nonlinearity; see Figure 28):

$$PNL := P + 4(B_V) \cdot P_{MAX} \cdot \left[\left(\frac{P}{P_{MAX}} \right) - \left(\frac{P}{P_{MAX}} \right)^2 \right] \quad (1)$$

Equation 2—Pressure constant. PNL referenced to full scale input pressure:

$$K_P := \frac{\left(P + 4(B_V) \cdot P_{MAX} \cdot \left[\left(\frac{P}{P_{MAX}} \right) - \left(\frac{P}{P_{MAX}} \right)^2 \right] \right)}{P_{MAX}} \quad (2)$$

Equation 3—Linearization Constant:

$$K_{LIN} := \frac{4 \cdot B_V \cdot V_{REF} \cdot K_{EXC}}{\left(VOUT_{MAX} - VOUT_{MIN}\right) - 2 \cdot B_V \cdot \left(VOUT_{MAX} + VOUT_{MIN}\right)} \quad (3)$$

Equation 4—Total PGA309 Gain:

$$G := \frac{\left(VOUT_{MAX} - VOUT_{MIN}\right)}{\left(V_{REF} \cdot K_{EXC} \cdot FSS\right) + \left(K_{LIN} \cdot VOUT_{MAX} \cdot FSS\right)} \quad (4)$$

Equation 5 —PGA309 V_{OUT}:

$$V_{OUT} := \frac{\left(FSS \cdot G \cdot K_P \cdot V_{REF} \cdot K_{EXC}\right) + VOUT_{MIN}}{1 - \left(FSS \cdot G \cdot K_P \cdot K_{LIN}\right)} \quad (5)$$

Equation 6 —PGA309 V_{EXC}:

$$V_{EXC} := V_{REF} \cdot K_{EXC} + K_{LIN} \cdot V_{OUT} \quad (6)$$

Equation 7—LinDAC Counts Conversion:

$$\text{Decimal\#Counts} = \frac{|\text{Desired } K_{LIN}|}{(\text{Full−Scale Ratio}/128)} \quad (7)$$

Example: Linearization DAC Counts Conversion

Given: (Range 1: $-0.166V_{FB} < \text{LinDAC} < +0.166V_{FB}$)

Find: Lin DAC value for $K_{LIN} = -0.082$

Solution:

1. Decimal # Counts = 0.082 / (0.166 / 128) = 63.228
2. Use 63 counts → 0x3F → 0011 1111
3. However, −0.082 is needed. Add 1 in the sign bit (MSB, Bit 7) for negative ratio:
4. Final LinDAC setting: 1011 1111 → 0xBF

Key Ideal Design Equations

Equation 8—Ideal Gain, G

$$G_{IDEAL} := \frac{VOUT_{MAX} - VOUT_{MIN}}{V_{REF} \cdot FSS} \quad (8)$$

Equation 9—VOUT Ideal.

$$VOUT_{IDEAL}(P) := FSS \cdot G_{IDEAL} \cdot \left(\frac{P}{P_{MAX}}\right) \cdot V_{REF} + V_{OS} \quad (9)$$

Equation 10—Full-Scale Range of Output

$$FSR := VOUT_{MAX} - VOUT_{MIN} \quad (10)$$

Equation 11—VOUT Error (%FSR).

$$VOUT_{ERR\_FSR} := \left(\frac{VOUT - VOUT_{IDEAL}}{FSR}\right) \cdot 100 \quad (11)$$

Example: Linearization Design		
SYSTEM INPUTS	**VALUE**	**UNITS**
P_{MIN}	0	psi
P_{MAX}	100	psi
FSS	0.005	V/V
Bv	+0.025 (+0.025 = +2.5%)	%
$VOUT_{MAX}$	4.5	V
$VOUT_{MIN}$	0.5	V
V_{REF}	5	V
K_{EXC}	0.83	
PGA309 CALCS		
K_{LIN}	+0.110667	V/V
G	172.117	V/V
$VOUT_{IDEAL}$		
G_{IDEAL}	160	V/V
FSR	4	V

P (psi)	K_P	VOUT (V)	V_{EXC} (V)	$VOUT_{IDEAL}$ (V)	VOUT ERROR (%FSR)
0	0.0000	0.5000	4.2053	0.5000	0
10	0.1090	0.8986	4.2494	0.9000	−0.03464537
20	0.2160	1.2981	4.2937	1.3000	−0.04667445
30	0.3210	1.6983	4.3380	1.7000	−0.04126142
40	0.4240	2.0990	4.3823	2.1000	−0.02381898
50	0.5250	2.5000	4.4267	2.5000	1.1102E−14
60	0.6240	2.9010	4.4710	2.9000	0.02430134
70	0.7210	3.3017	4.5154	3.3000	0.04294918
80	0.8160	3.7020	4.5597	3.7000	0.04956629
90	0.9090	4.1015	4.6039	4.1000	0.03753519
100	1.0000	4.5000	4.6480	4.5000	2.2204E−14

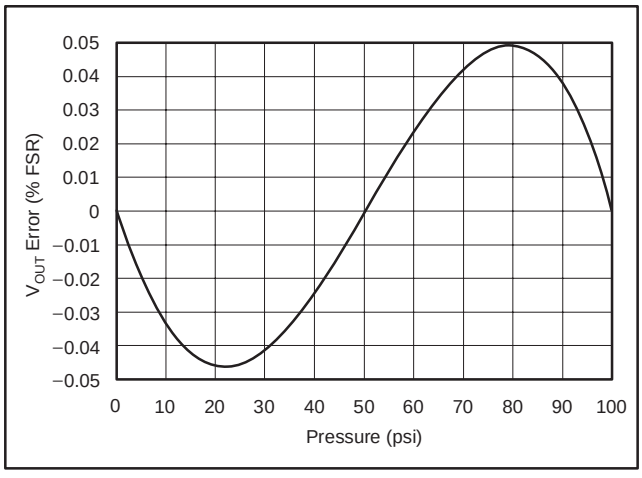


Figure 29. Parabolic Bridge Corrected Nonlinearity vs Pressure

In each end application, the linearization circuit limits should be checked for operation within the allowed range.

Table 15 and Table 16 illustrate the linearization range for several typical system applications. These tables account for the internal limits of the PGA309 linearization circuit and assume that V_{OUT} scaling is to account for over-scale and under-scale limits and fault detection. For specific end applications not listed, the following equations may be used to calculate critical design values, once the system design choices for V_{REF}, $V_{OUT\,MAX}$, $V_{OUT\,MIN}$ and linearization range, are made:

1. $V_{EXC\,MAX}$: Use *Equation (6)* at $VOUT_{MAX}$
2. $V_{EXC\,MIN}$: Use *Equation (6)* at $VOUT_{MIN}$
3. $B_{V\,MAX}$: (maximum compensatable nonlinearity)

Use $K_{LIN\,+MAX}$ to calculate $+B_{V\,MAX}$ and $K_{LIN\,-MAX}$ to calculate $-B_V$ Max by *Equation (3)* solved for Bv as:

$$B_V := \frac{VOUT_{MAX} - VOUT_{MIN}}{\left(\frac{4 \cdot V_{REF} \cdot K_{EXC}}{K_{LIN}}\right) + 2 \cdot \left(VOUT_{MAX} + VOUT_{MIN}\right)} \quad (12)$$

4. V_{LinDAC} Max = $((V_{REF}/4) - VOUT_{MAX}/10) \geq 300mV$
5. V_{EXC} Max ≤ V_{SA} − 0.1V
6. $K_{LIN} \leq K_{LIN\,MAX}$ (LinDAC range)

When using the Linearization Loop, care should be taken to ensure that the bridge sensor output common-mode voltage remains within the PGA309 input specifications. *Equation (6)* can be used to calculate the V_{EXC} at full-scale signal ($VOUT_{MAX}$). The common-mode voltage of the bridge sensor output is one-half of V_{EXC} if no common-mode or temperature sensing additional resistor is used in series with the bridge sensor.

During the sensor calibration process using the PGA309, a two-step process can be employed. First, the nonlinearity of the sensor bridge is measured with an initial gain and offset and with K_{LIN} = 0 (LinDAC set to Zero). Using the resulting sensor nonlinearity (B_V), values for K_{LIN}, Gain, and Offset are calculated. A second calibration measurement can be taken to adjust K_{LIN}, to account for any offsets and mismatches in the linearization circuitry. This calibration procedure is most easily performed using the PGA309 Designer's Kit and associated software and calibration spreadsheets.

$V_{SA\ MIN}$ (V)	$V_{SA\ MAX}$ (V)	V_{REF} (V)	ADC REF (V)	$V_{OUT\ MIN}$ (V)	$V_{OUT\ MAX}$ (V)	RANGE 0 $+B_{V\ MAX}$ $+B_V$ (0.025= 2.5%)	$V_{EXC\ MAX}$ (V)	$V_{EXC\ MIN}$ (V)	G	RANGE 0 $-B_{V\ MAX}$ $-B_V$ (−0.025= −2.5%)	$V_{EXC\ MAX}$ (V)	$V_{EXC\ MIN}$ (V)	G	RANGE 0 LinDAC MAX > 0.3V? (V)
2.7	5.5	2.5	2.5	0.175	2.225	0.0374	2.444	2.104	167.73	−0.0454	2.046	1.706	240.38	0.4025
2.7	5.5	2.5	2.048	0.123	1.761	0.0305	2.367	2.095	138.38	−0.0354	2.055	1.783	183.77	0.4489
4.5	5.5	4.096	2.5	0.175	2.175	0.0231	3.761	3.429	106.36	−0.0259	3.371	3.039	131.64	0.8065
4.5	5.5	4.096	4.096	0.246	3.564	0.0371	3.991	3.441	166.26	−0.0447	3.359	2.808	236.32	0.6676
4.5	5.5	4.096	2.048	0.143	1.782	0.0191	3.695	3.423	88.70	−0.0210	3.376	3.104	105.61	0.8458
4.7	5.5	4.5	4.5	0.27	4.185	0.0396	4.430	3.780	176.76	−0.0483	3.690	3.040	257.54	0.7065
5	5.5	5	5	0.3	4.65	0.0396	4.922	4.200	176.76	−0.0483	4.100	3.378	257.54	0.785

PGA309 V_{SA} Operating Range | PGA309 V_{REF} | System ADC REF (ADC full-scale) | PGA309 V_{OUT} Linear Range | PGA309 ($+B_{V\ MAX}$) | PGA309 V_{EXC} Range ($+B_{V\ MAX}$) | PGA309 Gain $V_{OUT}/V_{DIFF\ IN}$ ($+B_{V\ MAX}$) | PGA309 ($-B_{V\ MAX}$) | PGA309 V_{EXC} Range for ($-B_{V\ MAX}$) | PGA309 Gain $V_{OUT}/V_{DIFF\ IN}$ ($-B_{V\ MAX}$) | PGA309 LinDAC Max Check

Assumes: 1) Over-scale and under-scale limits and fault detection desired.
2) FSS used to calculate a representative gain value (G) for completeness.

NOTE: Range 0, K_{EXC} = 0.83, $K_{LIN\ -MAX}$ = −0.166, $K_{LIN\ +MAX}$ = 0.166, FSS = 0.005V/V

Table 15. Range 0—Typical System Applications and Maximum Nonlinearity Correction

$V_{SA\ MIN}$ (V)	$V_{SA\ MAX}$ (V)	V_{REF} (V)	ADC REF (V)	$V_{OUT\ MIN}$ (V)	$V_{OUT\ MAX}$ (V)	RANGE 1 $+B_{V\ MAX}$ $+B_V$ (0.025= 2.5%)	$V_{EXC\ MAX}$ (V)	$V_{EXC\ MIN}$ (V)	G	RANGE 1 $-B_{V\ MAX}$ $-B_V$ (−0.025= −2.5%)	$V_{EXC\ MAX}$ (V)	$V_{EXC\ MIN}$ (V)	G	RANGE 0 LinDAC MAX > 0.3V? (V)
2.7	5.5	2.5	2.5	0.175	2.225	0.0439	1.576	1.322	260.17	−0.0552	1.278	1.024	400.35	0.4025
2.7	5.5	2.5	2.048	0.123	1.761	0.0358	1.518	1.315	215.76	−0.0429	1.285	1.082	302.87	0.4489
4.5	5.5	4.096	2.5	0.175	2.175	0.0272	2.400	2.152	166.69	−0.0312	2.108	1.860	215.03	0.8065
4.5	5.5	4.096	4.096	0.246	3.564	0.0435	2.572	2.160	258.02	−0.0543	2.099	1.688	393.13	0.6676
4.5	5.5	4.096	2.048	0.143	1.782	0.0226	2.351	2.148	139.44	−0.0253	2.112	1.909	171.72	0.8458
4.7	5.5	4.5	4.5	0.27	4.185	0.0464	2.859	2.373	273.88	−0.0588	2.307	1.821	429.97	0.7065
5	5.5	5	5	0.3	4.65	0.0464	3.177	2.637	273.88	−0.0588	2.563	2.023	429.97	0.785

PGA309 V_{SA} Operating Range | PGA309 V_{REF} | System ADC REF (ADC full-scale) | PGA309 V_{OUT} Linear Range | PGA309 ($+B_{V\ MAX}$) | PGA309 V_{EXC} Range ($+B_{V\ MAX}$) | PGA309 Gain $V_{OUT}/V_{DIFF\ IN}$ ($+B_{V\ MAX}$) | PGA309 ($-B_{V\ MAX}$) | PGA309 V_{EXC} Range ($-B_{V\ MAX}$) | PGA309 Gain $V_{OUT}/V_{DIFF\ IN}$ ($-B_{V\ MAX}$) | PGA309 LinDAC Max Check

Assumes: 1) Over-scale and under-scale limits and fault detection desired.
2) FSS used to calculate a representative gain value (G) for completeness.

NOTE: Range 1, K_{EXC} = 0.52, $K_{LIN\ -MAX}$ = −0.124, $K_{LIN\ +MAX}$ = 0.124, FSS = 0.005V/V

Table 16. Range 1—Typical System Applications and Maximum Nonlinearity Correction

TEMPERATURE MEASUREMENT

The center of the PGA309 temperature measurement circuitry is the Temp ADC. The Temp ADC and its associated PGA, input mux, and REF mux provide a flexible and configurable temperature sensing block for reading either on-chip or external temperatures. Figure 30 illustrates the PGA309 temperature sense block.

The internal temperature sensing is accomplished by using on-chip diode junctions. The Internal Temperature Sensor mode is configured through setting the bits in Register 6 to the values shown in Table 17 and Table 18. The Temp ADC output can be read from Register 0 and is 12-bit + sign extended, right-justified, Two's Complement data format for R_1 and R_0 = '11', and TEN = '1' (see Table 19). For this Temp ADC resolution, the typical measured temperature resolution is 0.0625°C and the accuracy is ±2°C. The temperature accuracy is a relative error that is calibrated out with the PGA309 + sensor calibration to the accuracy of the calibration temperature measurement equipment.

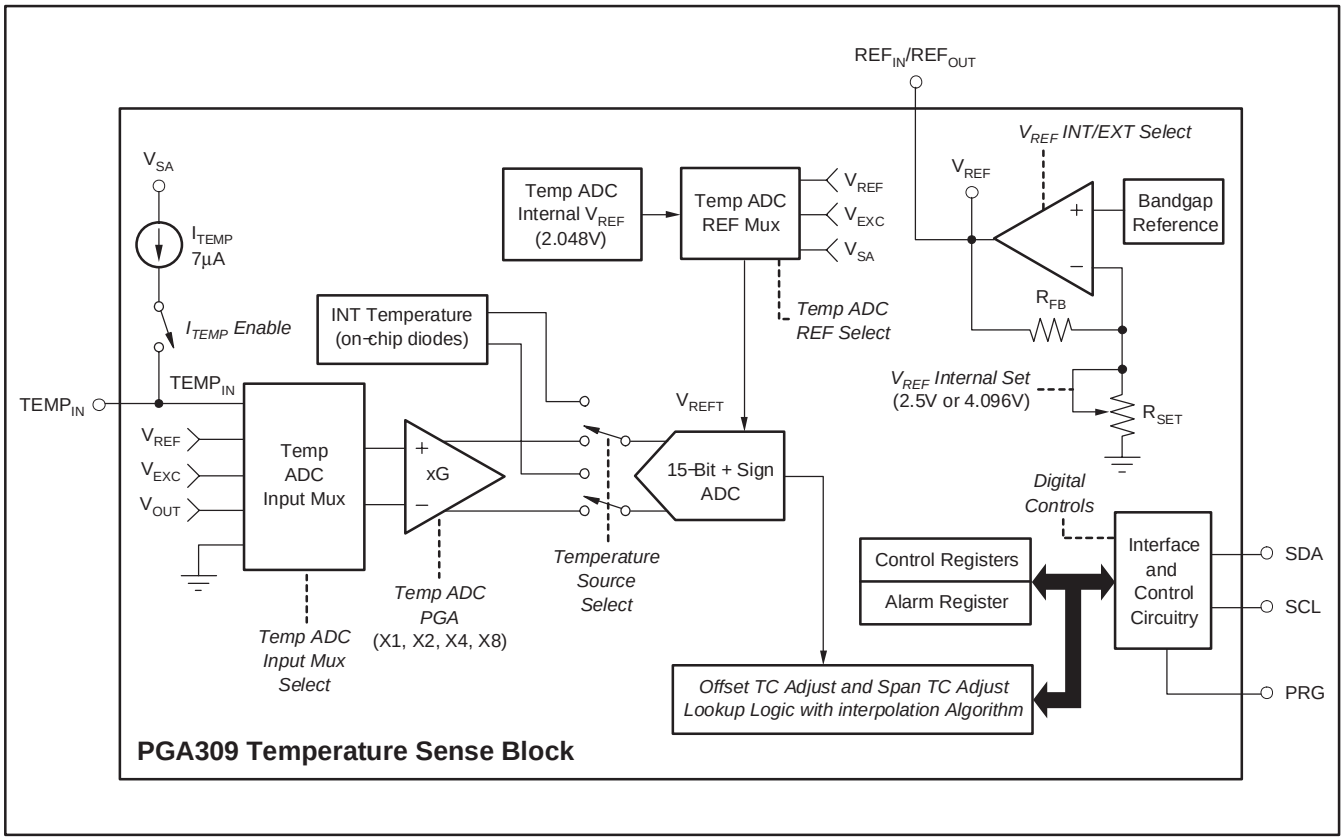


Figure 30. Temperature Sense Block

BIT	BIT NAME	BIT STATE	CONFIGURATION
15	RFB	0	Reserved Factory Bit—set to zero for proper operation
14	RFB	0	Reserved Factory Bit—set to zero for proper operation
13	ADC2X	0	Unused for Internal Temperature Mode; set to zero.
12	ADCS	0	
11	ISEN	0	
10	CEN	1	Enable the Temp ADC
9	TEN	1	Internal Temperature mode selected
8	AREN	0	Unused for Internal Temperature Mode; set to zero.
7	RV1	0	
6	RV0	0	
5	M1	0	
4	M0	0	
3	G1	0	
2	G0	0	
1	R1	1	See Temp ADC Resolution (Conversion time); select below
0	R0	1	See Temp ADC Resolution (Conversion time); select below

Table 17. Internal Temperature Mode Configuration—Register 6

R1	R0	TEMP ADC RESOLUTION (CONVERSION TIME) SELECT TEN = '1'
0	0	9-Bit + Sign, Right-Justified, Sign-Extended, 0.5°C (3ms)
0	1	10-Bit + Sign, Right-Justified, Sign-Extended, 0.25°C (6ms)
1	0	11-Bit + Sign, Right-Justified, Sign-Extended, 0.125°C (12ms)
1	1	12-Bit + Sign, Right-Justified, Sign-Extended, 0.0625°C (24ms)

Table 18. Temperature Mode Resolution—Register 6

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY) AD15.....AD0	DIGITAL OUTPUT (HEX)
128	0000 1000 0000 0000	0800
127.9375	0000 0111 1111 1111	07FF
100	0000 0110 0100 0000	0640
80	0000 0101 0000 0000	0500
75	0000 0100 1011 0000	04B0
50	0000 0011 0010 0000	0320
25	0000 0001 1001 0000	0190
0.25	0000 0000 0000 0100	0004
0.0	0000 0000 0000 0000	0000
−0.25	1111 1111 1111 1100	FFFC
−25	1111 1110 0111 0000	FE70
−55	1111 1100 1001 0000	FC90
−128	1111 1000 0000 0000	F800

Table 19. Internal Temperature Mode—Data Format (12-Bit Resolution)—Register 0

There are several optional configurations possible for the Temp ADC when External Temperature Sensor mode is selected. In this mode, the $TEMP_{IN}$ pin is being read as an indication of temperature. $TEMP_{IN}$ may be referenced to GND, V_{EXC}, or V_{REF}. In addition, V_{OUT} may also be selected to be read relative to GND through the Temp ADC. Figure 31 shows the allowed Temp ADC input mux configurations. Note that the choice to read V_{OUT} will result in reading the V_{OUT} pin of the PGA309 and not the V_{FB} pin. This will be a different voltage than the final conditioned sensor output at V_{FB} in applications that use an R_{ISO} resistor for overvoltage output protection and capacitive load isolation (see Output Amplifier section for details).

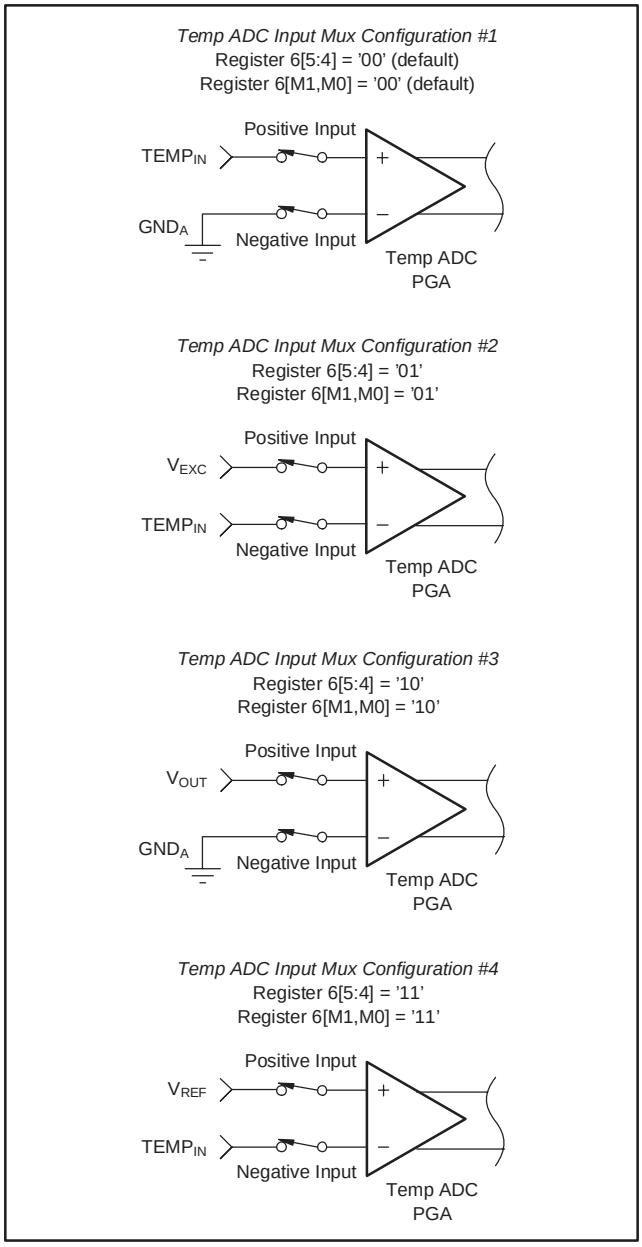


Figure 31. Temp ADC Input Mux Options

The Temp ADC PGA has four available gain settings that are detailed in Table 20.

G1 [3]	G0 [2]	TEMP ADC PGA GAIN
0	0	X1
0	1	X2
1	0	X4
1	1	X8

Table 20. Temp ADC PGA Gain Select—Register 6

The temperature sense block also contains an 7µA (typ) current source that is enabled by a logic '1' written to Register 6, bit 11, ISEN. A logic '0' disables I_{TEMP} from the $TEMP_{IN}$ pin. This current source can be used to excite an external resistive temperature device or diode for bridge sensor temperature measurement, as shown in Figure 32.

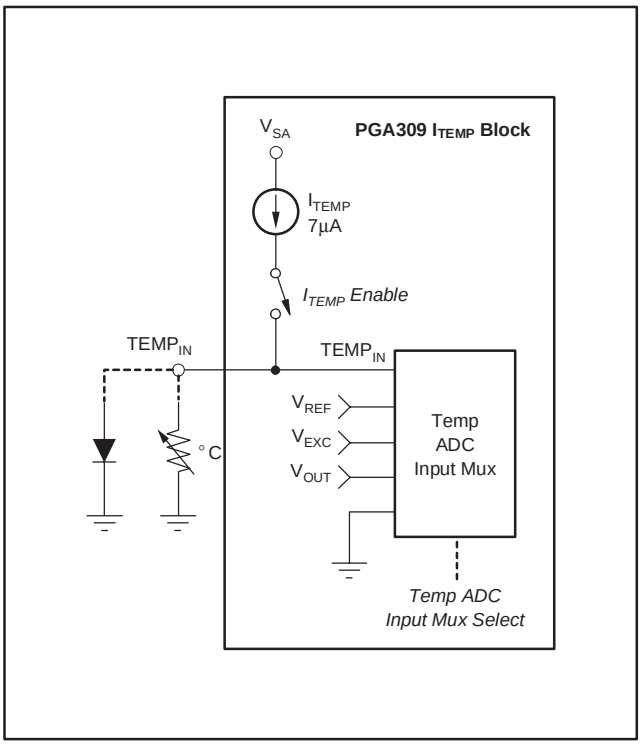


Figure 32. I_{TEMP} for External Temperature Measurement

The Temp ADC has several choices for its reference voltage for analog-to-digital conversions when used in External Temperature mode; these are illustrated in Table 21. In addition, the resolution of the Temp ADC when used in External Temperature mode is also register-selectable (see Table 22).

AREN [8]	RV1 [7]	RV0 [6]	TEMP ADC REFERENCE (V_{REFT})
0	0	0	V_{REF}
0	0	1	V_{EXC}
0	1	0	V_{SA}
0	1	1	Factory Reserved
1	X	X	Temp ADC Internal REF (2.048V)
NOTE: X = don't care.			

Table 21. Temp ADC Reference Select—Register 6

R1 [1]	R0 [0]	EXTERNAL SIGNAL MODE [TEN=0], EXTERNAL REFERENCE [AREN=0]	EXTERNAL SIGNAL MODE [TEN=0], INTERNAL REFERENCE [2.048V, AREN=1]
0	0	11-Bit + Sign, Right-Justified, Sign-Extended (6ms)	11-Bit + Sign, Right-Justified, Sign-Extended (8ms)
0	1	13-Bit + Sign, Right-Justified, Sign-Extended (24ms)	13-Bit + Sign, Right-Justified, Sign-Extended (32ms)
1	0	14-Bit + Sign, Right-Justified, Sign-Extended (50ms)	14-Bit + Sign, Right-Justified, Sign-Extended (64ms)
1	1	15-Bit + Sign, Right-Justified, Sign-Extended (100ms)	15-Bit + Sign, Right-Justified, Sign-Extended (128ms)

Table 22. Temp ADC Resolution (Conversion time)—Register 6

Temp ADC Start-Convert Control

The Temp ADC has two conversion modes: Single and Continuous. In Continuous Conversion mode (CEN = '1'), the Temp ADC initiates the next conversion cycle immediately after a conversion is complete. In Single Conversion mode (CEN = '0') the Temp ADC start-convert bit (ADCS) acts as a start-convert/busy bit and must be written or set to '1' before a conversion is initiated. After a '1' is written to ADCS, it will be a '1' if read immediately and can be polled until it returns to a '0', indicating the conversion is complete. The Start-Convert modes allowed are shown in Table 23.

In Figure 33 continuous start-convert control is selected. After an initial power-on reset timeout of typically 25ms, the register configuration (part one) of the EEPROM is read. Immediately after this, a Temp ADC conversion is started. At the end of this first conversion, the temperature coefficients (part two) of the EEPROM are read, and Zero and Gain DAC settings are adjusted. When CEN = '1', then at the end of each conversion another conversion is started. When the temperature coefficients are through being read, the EEPROM is read again at the beginning where the register configuration values are stored. Note that the only ADC results that are used to trigger the reading of the second half of the EEPROM (temperature coefficients) are the ones after a valid register configuration read part of the EEPROM. This operation yields the most temperature updates over a given time period.

CEN [10]	ADCS [12]	CONVERSION MODE	COMMENTS
0	0	Single	Temp ADC in standby mode – no conversions.
0	1	Single	Temp ADC starts conversion and ADCS acts as busy bit with it changing to a '0' at end of conversion.
1	X	Continuous	ADCS bit exercises no control – typically ADCS = '1' since conversions are continuous.

Table 23. Temp ADC Start-Convert Control—Register 6

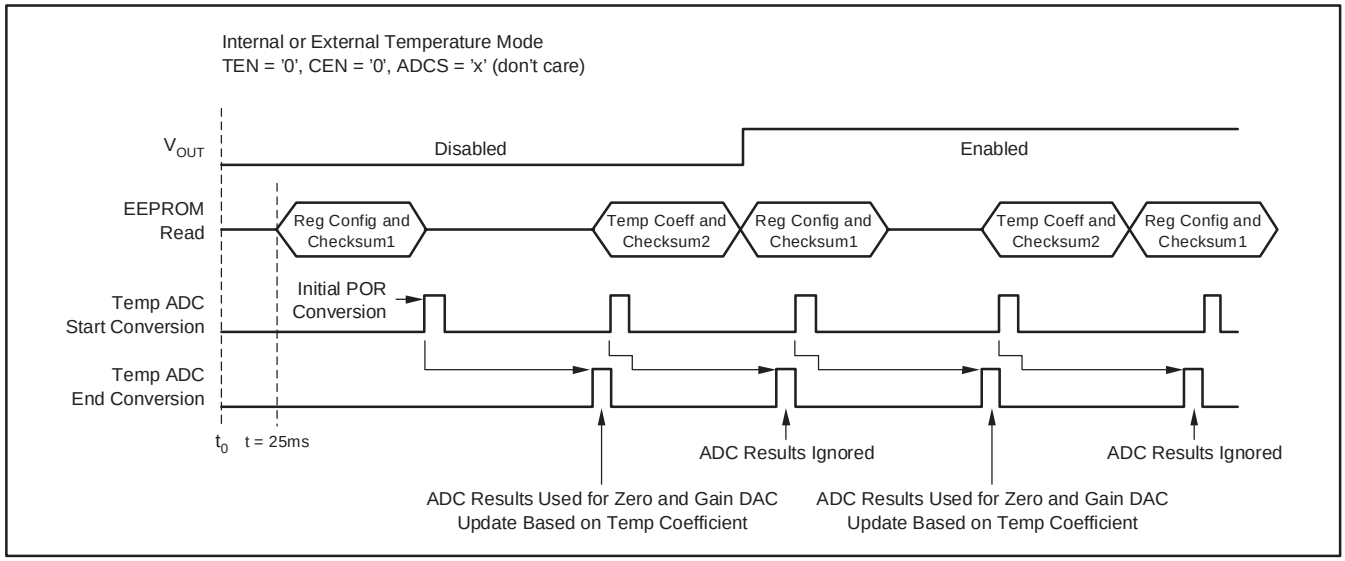


Figure 33. Temp ADC Continuous Start-Convert Control

In Figure 34, single start-convert control is selected. After an initial power-on reset timeout of typically 25ms, the register configuration (part one) of the EEPROM is read. Immediately after this, a Temp ADC conversion is started if CEN = '0' and ADCS = '1'. At the end of this first conversion, the temperature coefficients (part two) of the EEPROM are read, and Zero and Gain DAC settings are adjusted. When CEN = '0' and ADCS = '1', a new start conversion only occurs after reading the register configuration part of the EEPROM. At the end of this conversion, the second part of the EEPROM (temperature coefficients) is read, the Gain and Zero DAC temperature calculations are done, and each respective DAC updated. Note that in the Single Start-Convert mode, if CEN = '0' and ADCS = '0' (no Temp ADC conversions), the PGA309 will wait 25ms after power-on, read the register configuration part of the EEPROM, and without an ADC conversion, read the Lookup Table and calculate Gain and Zero DAC values. These values are based on the current ADC output register (all zero). The PGA309 output will then be enabled and will wait about 25ms, and read the register configuration part of the EEPROM. The output remains enabled with a continuous loop of reading the register configuration part of the EEPROM, waiting 25ms, and back to reading again.

One final control option for External Temperature mode is the ADC2X bit, Register 6 bit [13]. This bit allows the conversion speed of the Temp ADC to be increased for external temperature readings only.

Table 24 shows the typical settings and the effect of the ADC2X bit.

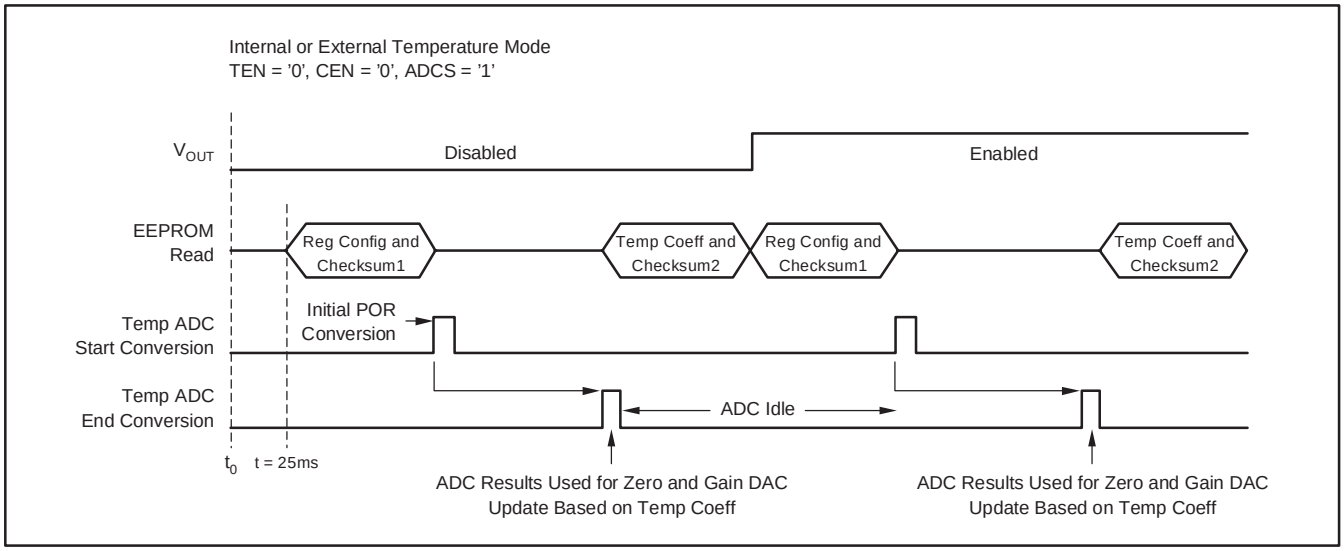


Figure 34. Temp ADC Single Start-Convert Control

R1 [1]	R0 [0]	[TEN=0], [AREN=0], [ADC2X=0]	[TEN=0], [AREN=0], [ADC2X=1]	[TEN=0] [2.048V, AREN=1], [ADC2X=0]	[TEN=0] [2.048V, AREN=1], [ADC2X=1]
0	0	11-Bit + Sign (6ms)	11-Bit + Sign (3ms)	11-Bit + Sign (8ms)	11 Bit + Sign (4ms)
0	1	13-Bit + Sign (24ms)	13-Bit + Sign (12ms)	13-Bit + Sign (32ms)	13 Bit + Sign (16ms)
1	0	14-Bit + Sign (50ms)	14-Bit + Sign (25ms)	14-Bit + Sign (64ms)	14 Bit + Sign (32ms)
1	1	15-Bit + Sign (100ms)	15-Bit + Sign (50ms)	15-Bit + Sign (128ms)	15 Bit + Sign (64ms)

Table 24. Temp ADC Conversion Speed Options for External Temperature Mode

External Temperature Sensing with an Excitation Series Resistor

For some bridge sensor applications, it is desired to measure the temperature of the bridge sensor by the change in the bridge resistance. This is accomplished by adding a series resistor in either the top or the bottom of the bridge excitation connections. When this is done, the common-mode voltage range of the PGA309 inputs must be observed over the operating temperature range of the application.

Figure 35 shows a top-side series resistor used to monitor the change in bridge resistance with temperature. For simplification of analysis, the effective bridge resistance is converted to one resistor (R_{BT}), as shown. For a given temperature, R_{BT} will be a fixed value; 1.8kΩ for this example at 70°C. Since R_T has a negligible change in temperature (50ppm/°C) compared with R_{BT} (3500ppm/°C), R_T is used to detect a change in R_{BT}. For this application, the Temp PGA is configured for V_{EXC} on the +input, and $TEMP_{IN}$ on the –input. The Temp ADC uses V_{EXC} as its reference, V_{REFT}. The PGA gain is set to X8. Notice that two different values for V_{EXC} will be analyzed to emulate the changing voltage on V_{EXC} due to the linearization block adjusting V_{EXC} to minimize error on the bridge sensor output with applied pressure. The square-boxed values show numerical results for V_{EXC} = 2.9V and the oval-ringed values for V_{EXC} = 2.4V. The final Temp ADC reading will be the same value as shown relative to full-scale range. This is equivalent to the same digital output of the Temp ADC regardless of what value V_{EXC} is adjusted to by the linearization block.

Figure 36 shows a bottom-side series resistor used to monitor the change in bridge resistance with temperature. Again, for simplification of analysis, the effective bridge resistance is converted to one resistor, R_{BT}, as shown. For 70°C, R_{BT} will be 1.8kΩ for this example. R_T will be used to measure the change in R_{BT}. The Temp PGA is configured for $TEMP_{IN}$ on the +input and GND on the –input. V_{EXC} is selected as the Temp ADC reference, V_{REFT}. The PGA gain is X8. The square-boxed values are results for V_{EXC} = 2.9V and the oval-ringed values for V_{EXC} = 2.4V. It is seen that the final Temp ADC reading will be the same regardless of the V_{EXC} value.

If the linearization block is not used in the application, the bridge sensor top excitation connection is either connected to V_{SA} or V_{REF} instead of V_{EXC}. In either of these cases, top-side (Figure 35) or bottom-side (Figure 36), external temperature sensing can be done by adding a series resistor, R_T. The Temp ADC reference (V_{REFT}) should be changed to the bridge excitation voltage (V_{SA} or V_{REF}) for the specific application. This yields a constant Temp ADC output at a given temperature independent of changes in the bridge excitation voltage.

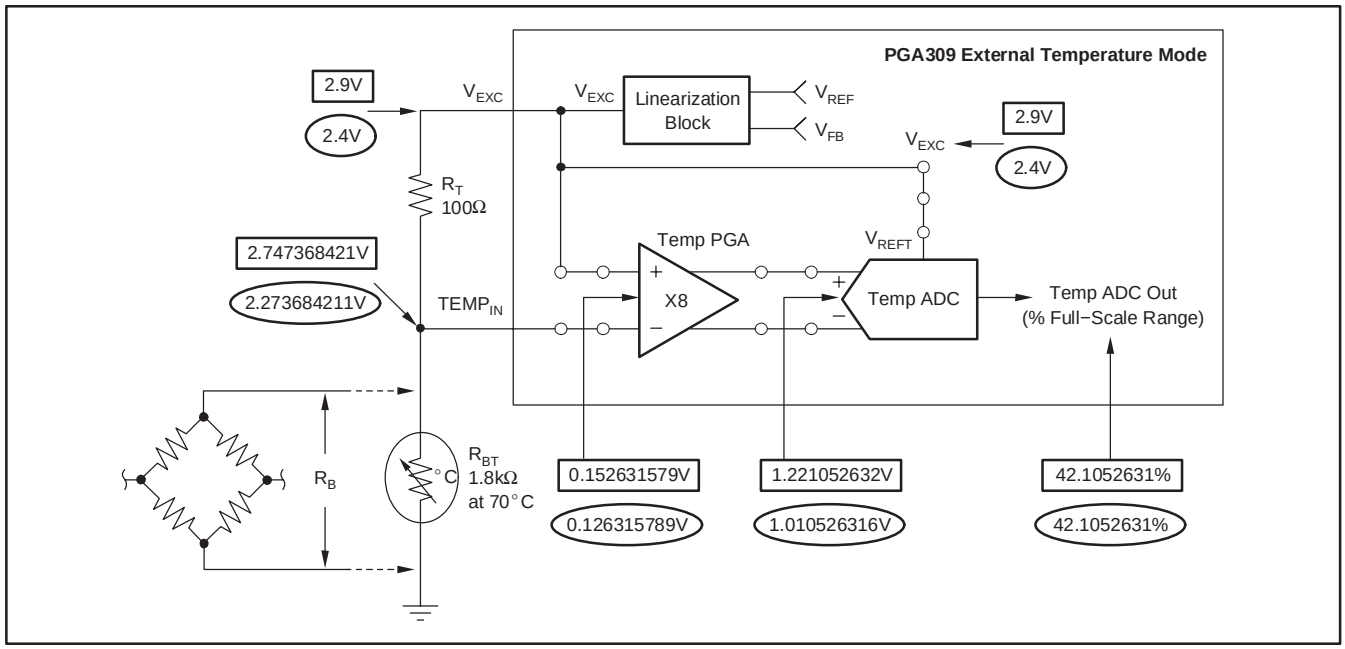


Figure 35. External Temperature Sensing of Bridge Sensor with Top-Side Series Resistor

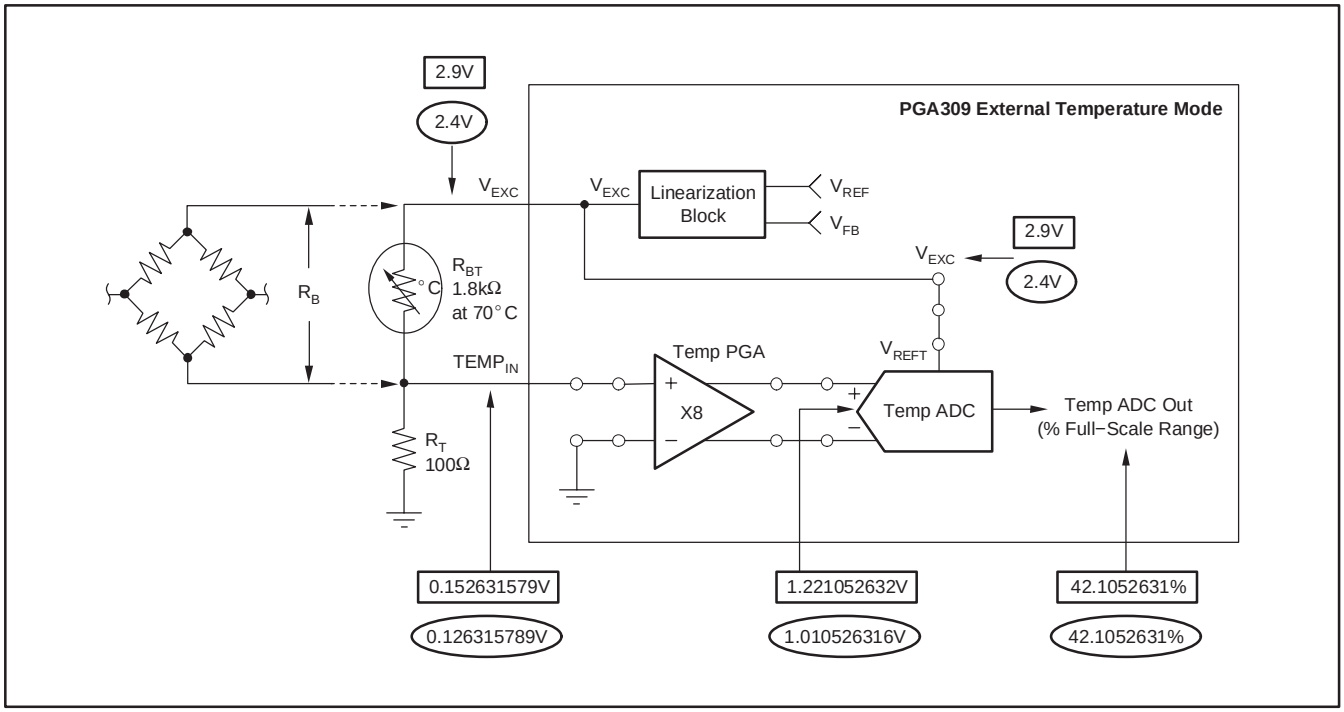


Figure 36. External Temperature Sensing of Bridge Sensor with Bottom-Side Series Resistor

OUTPUT AMPLIFIER

The Output Amplifier section of the PGA309 is configured to allow maximum flexibility and accuracy in the end application. Figure 37 depicts the output amplifier in a common three-terminal sensor application. In this application, it is desired to provide overvoltage protection due to mis-wires on the output of the PGA309, as well as a 10nF capacitor on the sensor module output for EMI/RFI filtering. In this configuration, R_{ISO} and R_{FB} provide overvoltage protection on $V_{OUT\ FILT}$ to 16V by limiting the current into V_{OUT} and V_{FB} to about 150mA [(16V − 0.7V)/100Ω]. The 0.7V drop being the internal ESD structure to GND or V_{SA}. In addition, R_{ISO} serves to isolate the 10nF RFI/EMI capacitive load from V_{OUT}. R_{FB} adds a slight gain error that is calibrated out with the PGA309 + sensor calibration. Note that the point of feedback around the output amplifier is taken from $V_{OUT\ FILT}$ and as such, after PGA309 + sensor calibration, the output amplifier will accurately scale $V_{OUT\ FILT}$ to match the desired conditioned sensor voltage. C_F provides a second feedback path around the output amplifier for guaranteed stability. With the configuration shown, the output amplifier is stable for internal output amplifier gains from X2 (125kHz bandwidth, 63° loop gain phase margin, typical values) to X9 (64kHz bandwidth, 86° loop gain phase margin, typical values). Table 25 details the typical output amplifier resistor values for RFO and RGO, as well as open-loop output resistance. These values, combined with the typical output amplifier open-loop gain curve and standard op amp stability techniques, allow the output amplifier to be tailored and configured for the specific sensor application.

GAIN	R_{FO} TYPICAL (kΩ)	R_{GO} TYPICAL (kΩ)
X2	18	18
X2.4	21	15
X3	24	12
X3.6	26	10
X4.5	28	8
X6	30	6
X9	32	4
NOTE: R_O = open-loop output resistance = 675Ω, typical at 1MHz.		

Table 25. Output Amplifier Typical Gain Resistor Values

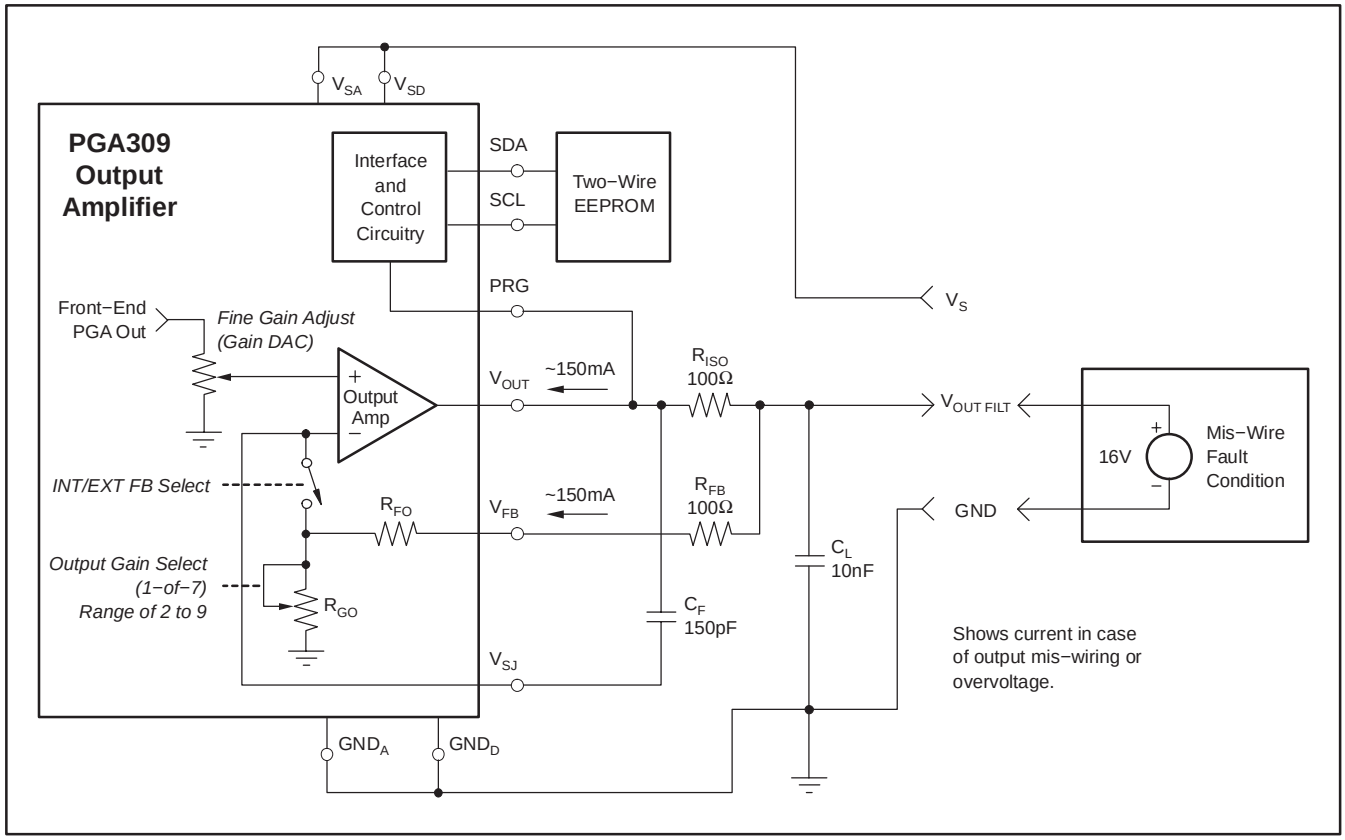


Figure 37. Output Amplifier in a Common 3−Terminal Sensor Application

In addition to using its own internal gain setting resistors, R_{FO} and R_{GO}, the output amplifier may use external feedback resistors RFO_{EXT} and RGO_{EXT}, as shown in Figure 38**.** Table 26 details the bits used in Register 4 for the desired output amplifier gain configurations. To use the external feedback resistors, set GO2, GO1, and GO0 to all 1s. In addition to allowing external feedback resistors to be used, this configuration provides a handy mechanism for testing the output amplifier stability, even if internal gain settings are to be used. As shown in Figure 38, external feedback resistors RFO_{EXT} and RGO_{EXT} are both set to 18kΩ, equivalent to the typical resistor values used for an internal gain setting of X2. If V_{OUT} is biased up to mid-scale (+2.5V for V_{SA} = +5V), a signal generator may be used to inject a 200mV_{PP} square wave (1kHz) into the end of RGO_{EXT} and a response measured at V_{OUT}. This provides a transient response for the output amplifier in a given configuration. Standard stability transient response criteria for a dominant two-pole system may be used to determine suitable phase margin based upon the measured overshoot and ringing on V_{OUT}.

GO2 [14]	GO1 [13]	GO0 [12]	OUTPUT AMPLIFIER GAIN
0	0	0	2
0	0	1	2.4
0	1	0	3
0	1	1	3.6
1	0	0	4.5
1	0	1	6
1	1	0	9
1	1	1	Disable Internal Feedback

Table 26. Output Amplifier Gain Selections—Register 4

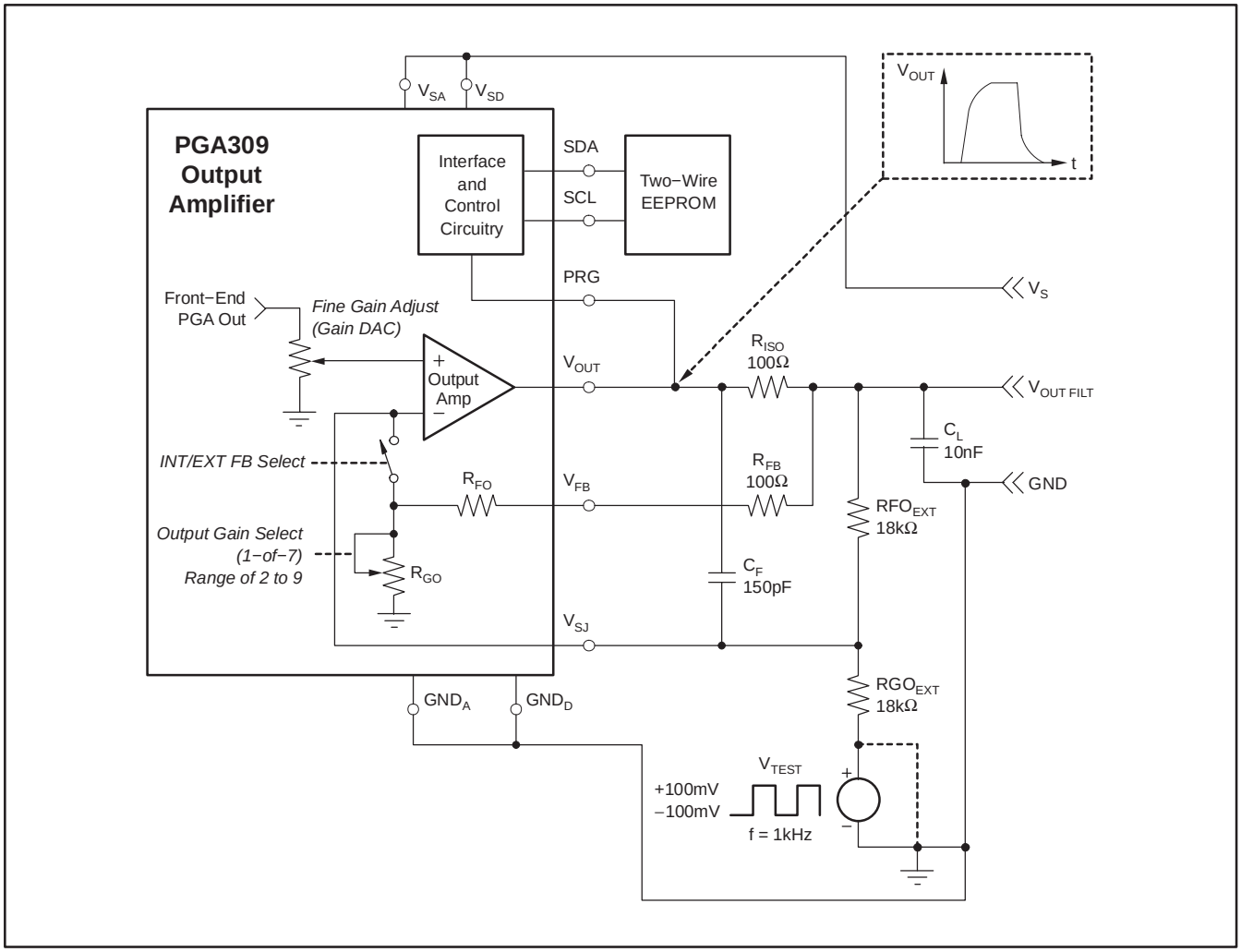


Figure 38. Output Amplifier Using External Feedback Resistors RFO_{EXT} and RGO_{EXT}

For low-supply applications, the minimum gain for the output amplifier is related to its input voltage range and output voltage swing. In Figure 39, the supply is lowered to +2.7V. The tested input voltage range of the output amplifier is 0V to V_{SA}−1.5V, as reflected in Figure 39. The output voltage swing is tested to be 0.1V to +2.6V for a 10kΩ load, as shown. This calculates to a minimum gain of X2.08. For best performance, the output amplifier should be scaled for a minimum gain of X2.4 for this application. Usually, this is only a factor at lower voltages but is easily checked for each individual application.

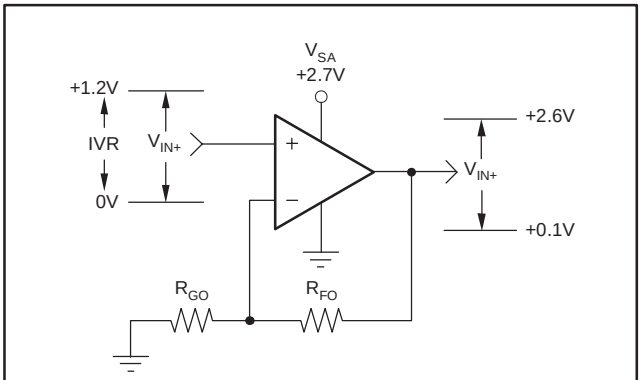
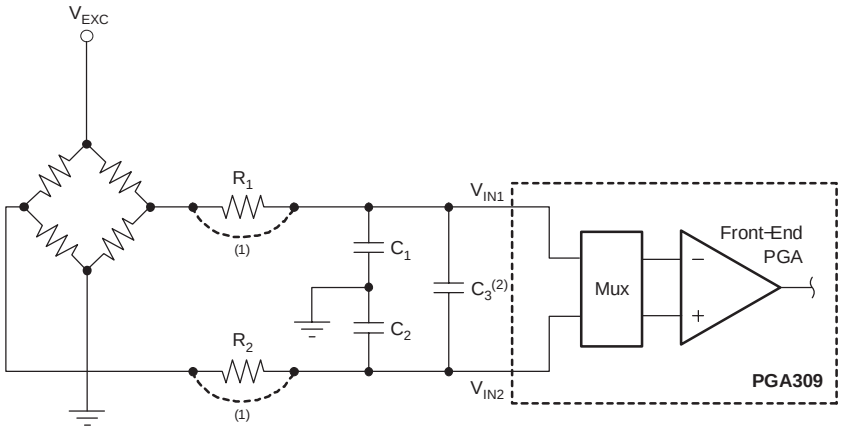


Figure 39. Output Amplifier Minimum Gain at Low Supply

GENERAL AC CONSIDERATIONS

In addition to normal good analog layout and design practices, there are a few key items to check when designing with the PGA309.

1. REF_{IN}/REF_{OUT}, pin 16: Keep capacitive loading to 200pF or less.
2. V_{EXC}, pin 1: Keep capacitive loading to 200pF or less.
3. V_{SA}, pin 3 and V_{SD}, pin 10: Keep these within 200mV of each other. Internally, the PGA309 separates its digital and analog power supplies to minimize cross-talk between the two. Externally, tie the two together and bypass, directly at the pins, with a 0.1µF capacitor. If an RC filter is used between the two supplies, ensure that maximum drop is never more than 200mV.
4. GND_A, pin 2 and GND_D, pin11: Ensure that these are both tied directly together and connected to the same ground point.
5. V_{SJ}, pin 8: This is the negative input to the output amplifier and as such, it is high-impedance. Route low-impedance traces, such as V_{OUT}, and noisy traces away from V_{SJ}. Minimize trace lengths to avoid unwanted additional capacitance on V_{SJ}.
6. V_{IN1}, pin 4 and V_{IN2}, pin 5: For source resistances greater than or equal to 10kΩ, add a capacitor of 1nF to 2nF between V_{IN1} and V_{IN2} to minimize noise coupling.
7. V_{IN1}, pin 4 and V_{IN2}, pin 5: RFI filtering is always a concern for instrumentation amplifier applications. RFI signals injected into instrumentation amplifiers become rectified and appear on the output as a DC drift or offset; high-gain circuits amplify this effect. Figure 40 depicts input filtering for the PGA309. Depending upon the distance of the bridge sensor from the PGA309 and the sensor module shielding, R_1 and R_2 may be required. C_1 should be equal to C_2, and C_3 should be ten times larger than C_1 to attenuate any common-mode signals that become differential due to the mismatch in C_1 and C_2. All input filter components should be located directly at the PGA309 inputs to avoid and trace lengths from becoming receiving RFI antennas.



NOTES: (1) Depends on bridge sensor resistance and distance from bridge sensor to PGA309.
(2) $C_1 = C_2$, $C_3 = 10 \times C_1$.

Figure 40. Input Filtering

OPERATING MODES

Power-On Sequence and Normal Stand-Alone Operation

The PGA309 internal state machine controls the operations of the part in stand-alone mode, without any external digital controller. In this mode, the PGA309 performs the functions of a Two-Wire interface master to read the data from the EEPROM.

The PGA309 has power-on reset (POR) circuitry to reset the internal registers and subcircuits to their initial states. This power-on reset also occurs when the supply is detected to be too low so that the PGA309 is in a known state when the supply becomes valid again. The threshold for the POR circuit is approximately +1.5V to +2.5V.

After the power supply becomes valid, the PGA309 waits for approximately 25ms and then attempts to read the configuration register data (Register 3—Register 6 bit settings) from the first 16 bytes of the external EEPROM device. If the EEPROM has the proper programmed flag word (0x5449, “TI” ASCII) in address locations 0 and 1, the PGA309 will continue reading the EEPROM. Otherwise, the PGA309 will wait for one second before trying again. If the PGA309 detects that there was no response from the EEPROM and the Two-Wire bus was in a valid idle state (SCL = ‘1’, SDA = ‘1’), then the PGA309 will wait for 1s and try again. If the Two-Wire bus is stuck with SDA = ‘0’, the PGA309 will try to free the bus by sending extra clocks down SCL (see the Digital Interface section for details), and wait for 25ms before trying to read the EEPROM again. If the EEPROM configuration read is successful (including valid Checksum1 data) and either bits ADCS or CEN in Register 6 are set to ‘1’, the PGA309 will trigger the Temp ADC to measure the temperature information as configured in the configuration registers. For 16-bit resolution results, the converter takes approximately 125ms to complete a conversion. Once the conversion is complete, the PGA309 begins reading the Lookup Table from EEPROM address locations 16 and higher, to calculate the settings for the Gain and Zero DACs using the piecewise linear interpolation algorithm. The PGA309 reads the entire Lookup Table and determines if the checksum for the Lookup Table (Checksum2) is correct. Each entry in the Lookup Table requires approximately 500µs to read from the EEPROM. Once Checksum2 is determined to be valid, the calculated value for the Gain and Zero DACs is updated into their respective registers, and the output amplifier (V_{OUT}) is enabled. The PGA309 then begins looping through this entire procedure, starting again with reading the configuration data from the first part of the EEPROM. This loop continues indefinitely.

> **NOTE:** During the entire initial power-on sequence, the PGA309 V_{OUT} is disabled (high-impedance) until valid EEPROM contents are verified and an ADC conversion is complete, as described above and illustrated in Figure 41. If the the PGA309 is used in a true three-wire connection (V_S, GND and V_{OUT} with PRG pin shorted to V_{OUT}) the time interval after power-up is the only opportunity that an external communications controller can initiate digital communication with the PGA309 and trigger a one second delay in the internal state machine. After V_{OUT} is enabled no further digital communication is possible.

If the PGA309 detects that there is no EEPROM device present (that is, it does not receive an acknowledge to a slave address byte sent to the EEPROM), the PGA309 will wait for approximately one second and try again. It will continue in this loop indefinitely with V_{OUT} disabled.

At any time, if the PGA309 is addressed through the Two-Wire or One-Wire interface, the internal state machine aborts its cycle and initiates a 1s delay. After the 1s delay has timed out, a EEPROM read is started. The 1s delay is reset every time the PGA309 is addressed. This allows an external microcontroller to control the function of the PGA309, as long as some communication activity is addressed to the PGA309 at least once per second. V_{OUT} will stay in the state (enabled or disabled) that it was in before the PGA309 was addressed. If full microcontroller control of the PGA309 is desired from initial power-on, then the Test pin should be brought high to enable the output after the internal PGA309 registers have been configured to their desired state.

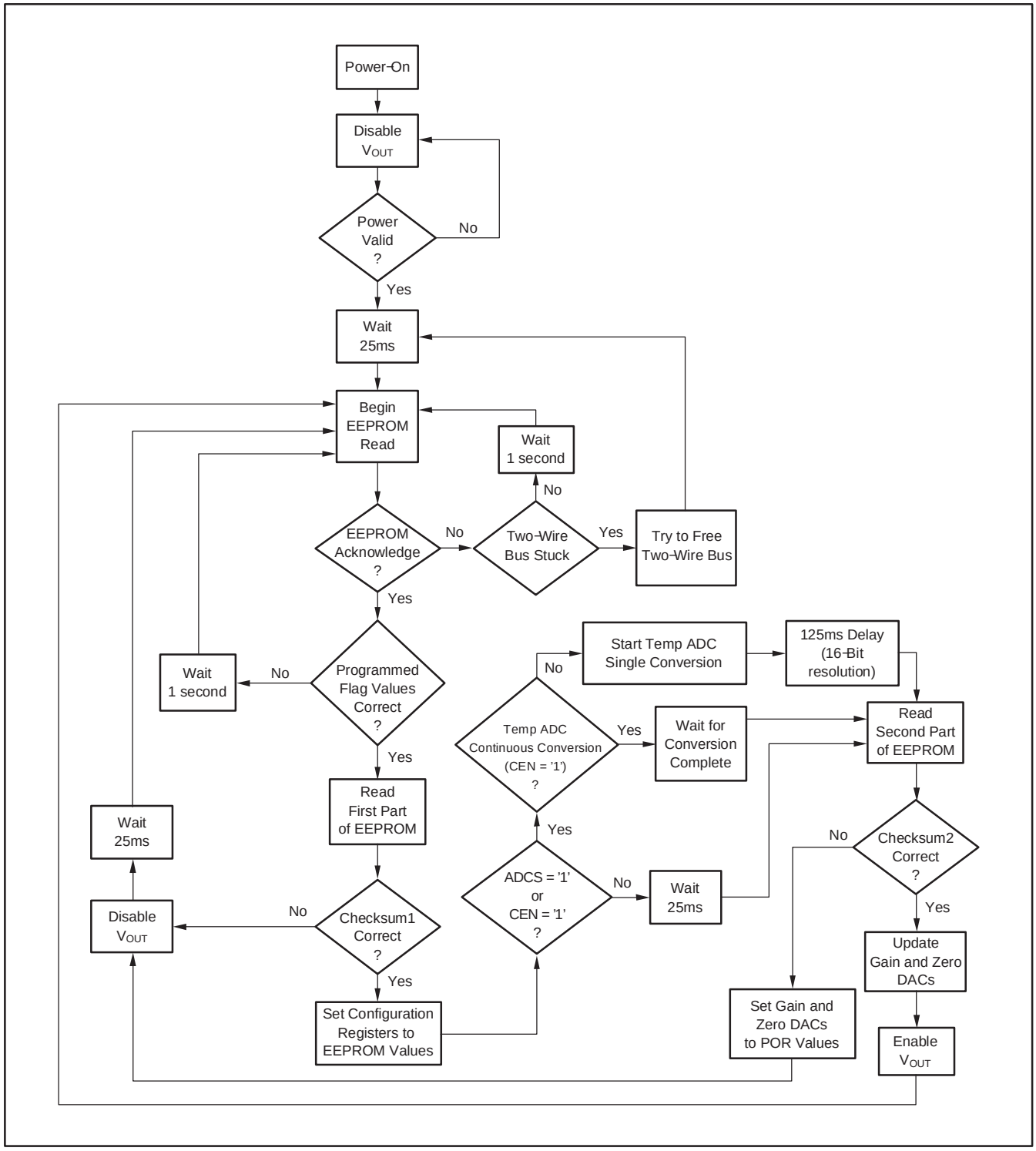


Figure 41. State Machine—Power-On Sequence and Operation in Stand-Alone Mode

Checksum Error Event

If at any time the PGA309 detects an invalid Checksum1 from the first part of the EEPROM, the PGA309 will disable V_{OUT}, wait for approximately 25ms, and try to read the EEPROM again from the beginning. It will continue to re-read the EEPROM indefinitely. If at any time the PGA309 detects an invalid Checksum2 from the second part of the EEPROM (the Lookup Table data), it will disable V_{OUT}, set the Gain and Zero DACs to their POR values, return to the read configuration register portion (first part of the EEPROM) of the loop, and then try to read the EEPROM Lookup Table again when the next temperature conversion completes.

Test Pin

The PGA309 has a user-accessible test pin (Test, pin 9), which stops the internal state machine cycle and enables the output drive (V_{OUT}) when it is brought high (logic '1'). This mode can be used for ease of troubleshooting or initial configuration diagnostics during the system design. During normal (stand-alone) operation, the Test pin must be pulled or shorted to GND (logic '0').

If the Test pin is pulled high at any time, the following happens:

- The state machine described previously is interrupted and reset to its initial state. Any EEPROM transactions are interrupted and the Two-Wire bus is released.
- The PGA309 output (V_{OUT}) is enabled.
- All internal registers are kept to their current values. If the Test pin is high when the supply becomes valid, the registers stay in the initial (POR) state and output is enabled immediately.
- An external controller can modify any of the writable PGA309 registers using either a One-Wire or Two-Wire digital interface.

In this mode, a test signal can be applied to the front-end of the PGA309, which quickly verifies if the signal path through the PGA309 is functioning correctly.

Power−On Initial Register States

In a power-up or a brownout event, the POR circuit resets all the PGA309 registers to their initial state. All registers are set to zeros except for the Gain and Zero DACs, which both are set to 0x4000.

Table 27 summarizes the key settings for the POR states.

PARAMETER	POR STATE
Coarse Offset	0V
Front-End PGA Gain	X4 ($V_{IN1} = V_{INP}$, $V_{IN2} = V_{INN}$)
Gain DAC	X0.5
Output Amplifier Gain	X2
Zero DAC	$0.25V_{REF}$
V_{REF} Select	External Reference
Lin DAC	X0
Fault Monitor	Disabled
Over/Under-Scale	Disabled
V_{EXC}	Disabled
I_{TEMP}	Disabled
Temp ADC	External Signal Mode

Table 27. POR States for Key Parameters

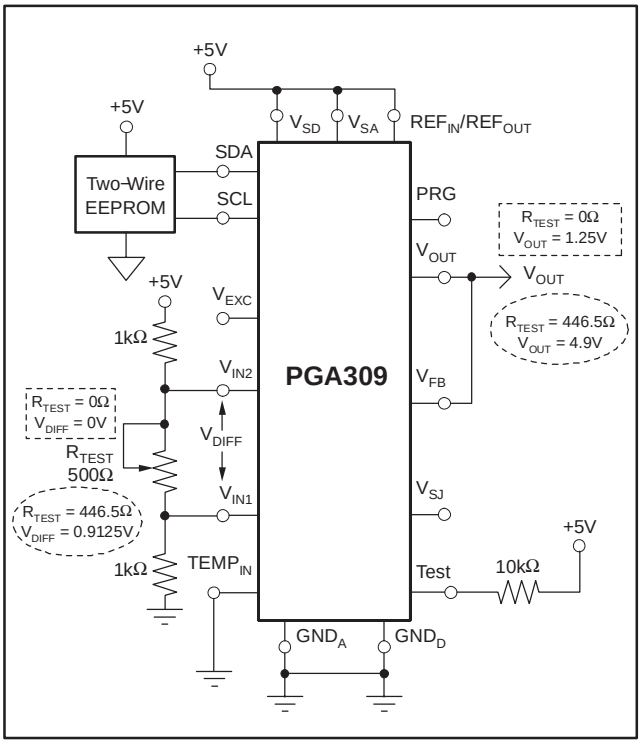


Figure 42. Signal Path Functional Check with Test = '1' on Power-Up

Example: PGA309 Power-Up State

For a +5V supply and configuration as shown in Figure 42 with Test pin HIGH, the gain and offset scaling through the PGA309 on power-up becomes:

$V_{OUT} = V_{DIFF}$ (Front-End PGA Gain)(Output Amplifier Gain)(Fine Gain) + $0.25V_{REF}$(Fine Gain)(Output Amplifier Gain)

$V_{OUT} = V_{DIFF}$ (4)(2)(0.5) + (0.25(5)(0.5)) × 2

$V_{OUT} = 4\ V_{DIFF} + 1.25V$

DIGITAL INTERFACE

There are two digital interfaces on the PGA309. The PRG pin uses a One-Wire, UART compatible interface, with bit rates from 4.8kbits/s (4800 baud) to 38.4kbits/s (38400 baud). The SDA and SCL pins together form an industry standard Two-Wire interface at clock rates from 1kHz to 400kHz. The external EEPROM uses the Two-Wire interface for programming and reading. Communication to the PGA309 internal registers can be conducted through either digital interface, One-Wire or Two-Wire. Additionally, the external EEPROM can be programmed through the PGA309 One-Wire interface pin, PRG.

Two-Wire Interface

The industry standard Two-Wire timing diagram is shown in Figure 43, with the timing diagram definitions in Table 28. The key operating states are:

- Bus Idle: Both SDA and SCL lines remain high.
- Start Data Transfer: A change in the state of the SDA line, from high to low, while the SCL line is high, defines a START condition. Each data transfer is initiated with a START condition.
- Stop Data Transfer: A change in the state of the SDA line from low to high while the SCL line is high defines a STOP condition. Each data transfer is terminated with a repeated START or STOP condition.
- Data Transfer: The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device. The receiver acknowledges the transfer of data.
- Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge bit. A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge clock pulse. Setup and hold times must be taken into account. On a master receive, the termination of the data transfer can be signaled by the master generating a not-acknowledge on the last byte that has been transmitted by the slave (see Figure 44).

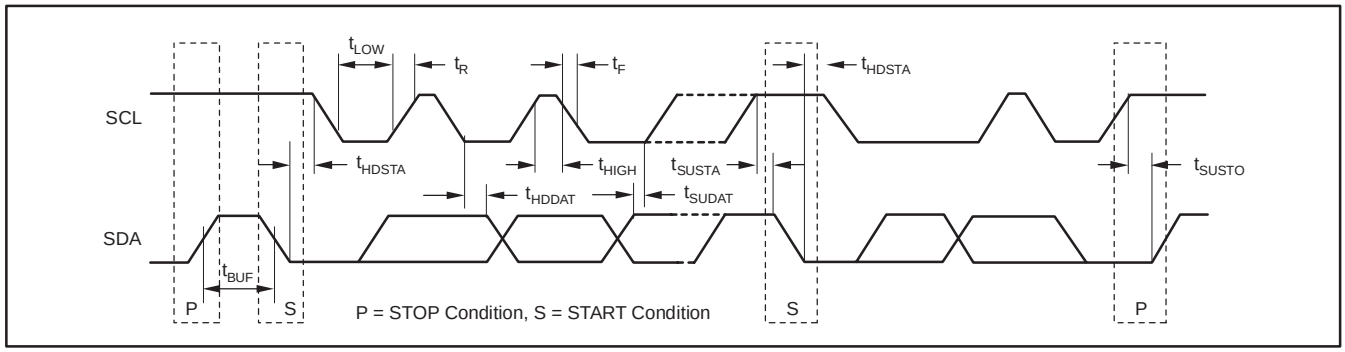


Figure 43. Two-Wire Timing Diagram

PARAMETER		MIN	MAX	UNITS
SCL Operating Frequency	f_{SCL}	1	400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}	600		ns
Hold Time After Repeated START Condition. After this period, the first clock is generated.	t_{HDSTA}	600		ns
Repeated START Condition Setup Time	t_{SUSTA}	600		ns
STOP Condition Setup Time	t_{SUSTO}	600		ns
Data Hold Time	t_{HDDAT}	0		ns
Data Setup Time	t_{SUDAT}	100		ns
SCL Clock LOW Period	t_{LOW}	1300		ns
SCL Clock HIGH Period	t_{HIGH}	600		ns
Clock/Data Fall Time	t_F		300	ns
Clock/Data Rise Time	t_R		300	ns

Table 28. Two-Wire Timing Diagram Definitions

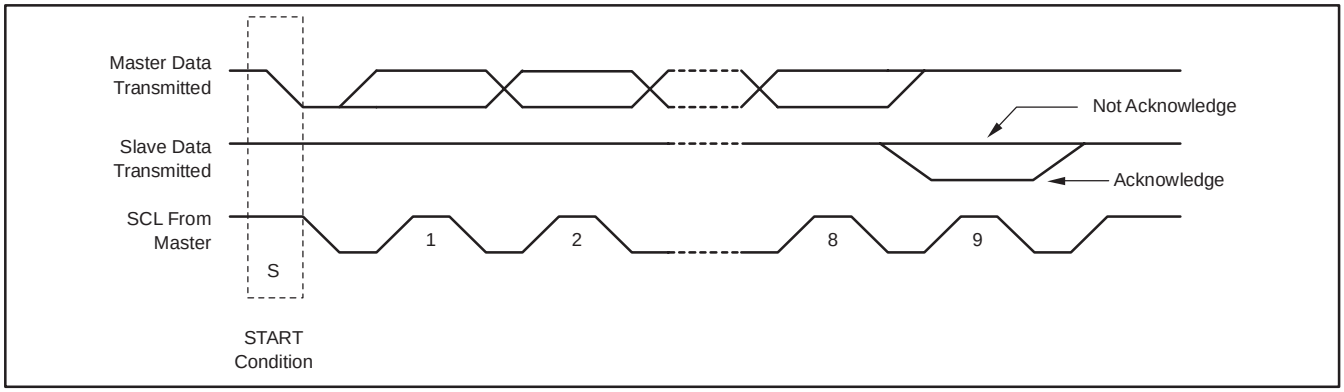


Figure 44. Two-Wire Acknowledge

Device Addressing:
Following a START condition issued by the master, a control byte is the first byte received. The seven most significant bits (MSBs) of the control byte are the slave address for the part being addressed. The last bit of the control byte is a read/write control bit (read = '1', write = '0'). The slave addresses for the PGA309 and supported external EEPROM are shown in Figure 45.

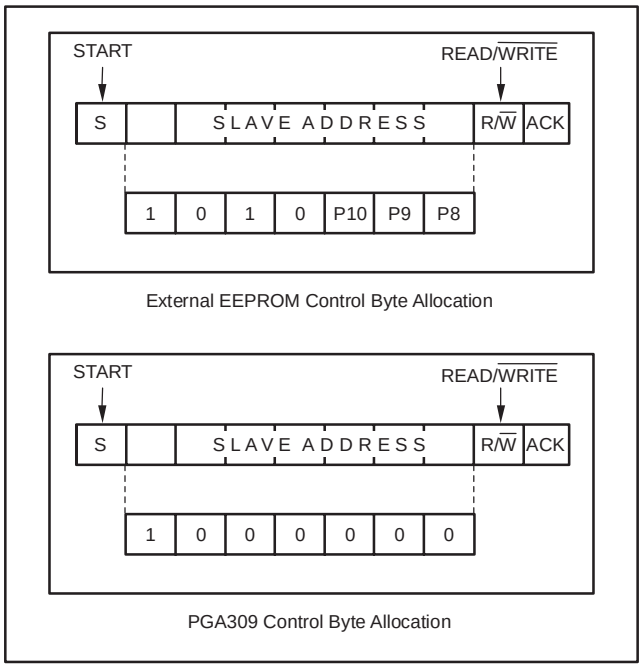


Figure 45. External EEPROM and Control Byte Allocation

Two−Wire Access to PGA309
The read and write timing supported for interfacing directly with the PGA309 internal registers is shown in Figure 46.

One-Wire Interface
The PGA309 may be configured through a single-wire UART-compatible interface (PRG pin). The interface also allows programming of the external industry-standard Two-Wire EEPROM device. There are six communication transactions that are available. These transactions allow the internal register pointer to be updated, the external EEPROM pointer to be updated, internal registers to be read, internal registers to be written, EEPROM data to be read, and EEPROM data to be written. It is possible to connect the PRG pin, which uses the One-Wire interface, to the V_{OUT} pin in true three-wire sensor module and still allow for digital programming.

Each transaction consists of several bytes of data transfer. Each byte consists of 10 bit periods. The first bit is the start bit and is always zero. The PRG pin should always be high when no communication is in progress. The one-to-zero (high-to-low) transition signals the start of a byte transfer and all timing information for the current byte is referenced to this transition. The second through ninth bits are the eight data bits for the byte and are transferred least significant bit (LSB) first. The tenth bit is the stop bit and is always one. The recommended circuit implementation is to use a pull-up resistor and/or current source with an open drain (or open collector) driver connected to the PRG pin, which is also an open drain output. The PRG pin may be driven high by the digital programmer (controller) during transmit from the controller, but some form of pull-up will be required to allow the signal to go high during receive, since the PGA309 can only pull the output low. Figure 47 shows a typical connection between the PGA309 PRG pin and the controller.

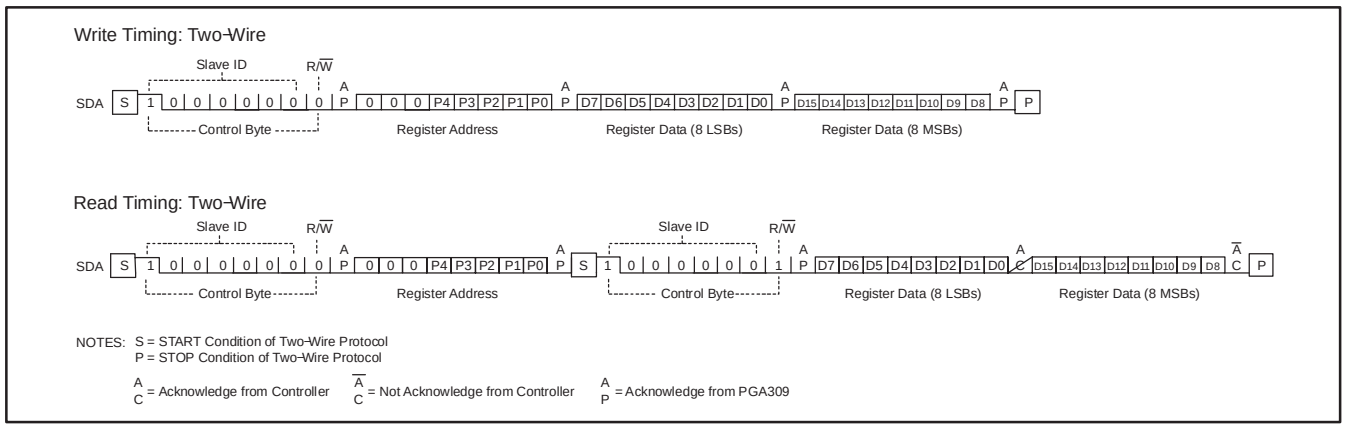


Figure 46. Two-Wire Access to PGA309 Timing

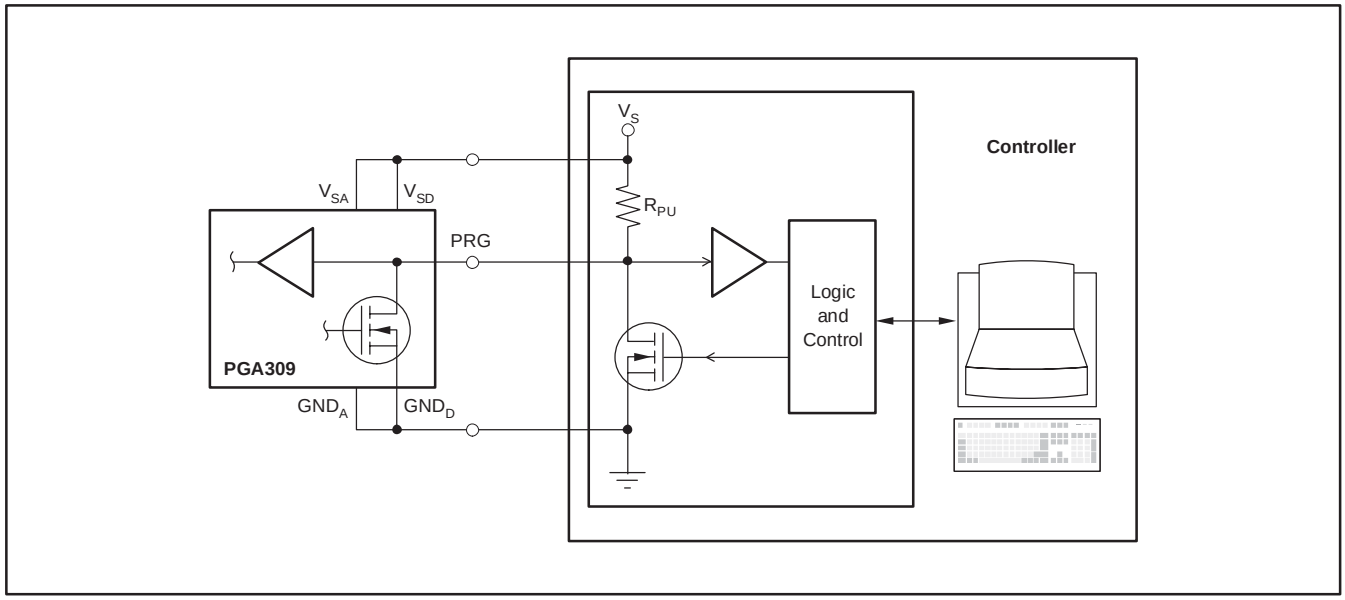


Figure 47. Typical PGA309 PRG To Controller Connection

All communication transactions start with an initialization byte transmitted by the controller. This byte (55h) is used to sense the baud rate used for the communication transaction. The baud rate is sensed during the initialization byte of every transaction. This baud rate is used for the entire transaction. Each transaction may use a different baud rate if desired. Baud rates of 4800 to 38400 are supported. The second byte is a command byte transmitted by the controller.

There are six possible commands:

- Set Register Address Pointer (01h)
- Set EEPROM Address Pointer (02h)
- Write Register (04h)
- Write EEPROM Word (08h)
- Read Register (10h)
- Read EEPROM Word (20h)

See Figure 48 for timing details of these transactions.

Figure 48. One-Wire (PRG) Access to PGA309 and External EEPROM Timing

Additional data transfer occurs after the command byte. The number of bytes and direction of data transfer depends on the command byte.

For the Set Register Address Pointer command, one additional byte is required to be transmitted by the controller. This is used to select the PGA309 internal register for the next Write Register or Read Register command. For the Write Register command, two additional bytes are required to be transmitted by the controller. These two bytes, transmitted least significant byte first, are stored in the PGA309 internal register pointed to by the register address pointer. The addressed register will be updated with all 16 bits simultaneously at the completion of the transfer of the second byte. For the Read Register command, two additional bytes are transmitted by the PGA309. The PGA309 waits for eight bit periods after the completion of the command byte before beginning to transmit. This allows time for the controller to ensure that the PGA309 will be able to control the One-Wire interface. The first byte transmitted is the least significant byte of the register and the second byte is the most significant byte of the register.

For a One-Wire PGA309 register write, the transactions may be repeated immediately one after the other, as shown in Figure 49. For a One-Wire PGA309 register read, the transactions may be repeated after the data has been received from the PGA309, also shown in Figure 49.

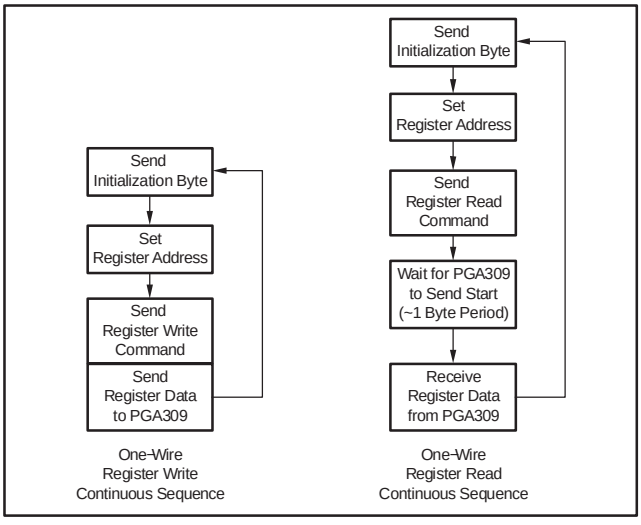


Figure 49. One-Wire Access to PGA309 Registers

For the Set EEPROM Address Pointer command, two additional bytes are required to be transmitted by the controller. These are used for the EEPROM address for the next Write EEPROM or Read EEPROM command. For the Write EEPROM command, two additional bytes are required to be transmitted by the controller. These two bytes are written to the EEPROM and stored at the address contained in the EEPROM address pointer. The first byte (least significant byte) is written to the address in the EEPROM address pointer. The second byte (most significant byte) is written to the address in the EEPROM address pointer plus one. To avoid any confusion, it is required that the EEPROM address pointer always be set to a value that is even. The first byte is written to the even address and the second byte is written to the next consecutive odd address. The controller is responsible for ensuring that the EEPROM device has enough time to successfully complete the write operation before additional EEPROM communication occurs. For a typical EEPROM, this will be about 5.6ms (0.6ms for the PGA309 to write a 16-bit byte into the EEPROM and 5ms for the EEPROM nonvolatile internal write cycle). For the Read EEPROM command, two additional bytes are transmitted by the PGA309. The PGA309 waits for eight bit periods after the completion of the command byte to allow time for data direction change. The PGA309 also waits for a read communication from the EEPROM device to occur. This will typically be approximately 600µs of additional delay. The first byte transmitted is the least significant byte (from address) and the second byte transmitted is the most significant byte (from address + 1).

For continuous One-Wire PGA309 EEPROM writes, the controller must insert a typical 5.6ms delay between transactions, as shown in Figure 50. For continuous One-Wire PGA309 EEPROM reads, the transactions may be repeated after the data has been received from the PGA309, as shown in Figure 50.

If there is an invalid communication transaction or disconnect with the EEPROM, a One-Wire EEPROM read will be all 1s.

One-Wire Interface Timeout

To allow for resynchronization of the One-Wire interface, and if synchronization between the controller and the PGA309 be lost for any reason, a timeout mechanism is implemented. The timeout period is set to approximately 25ms to 35ms. If the timeout period expires between the initialization byte and the command byte, between the command byte and any data byte, or between any data bytes, the PGA309 will reset the One-Wire interface circuitry such that it will be expecting an initialization byte. Every time that a byte is transmitted on the One-Wire interface, this timeout period is restarted.

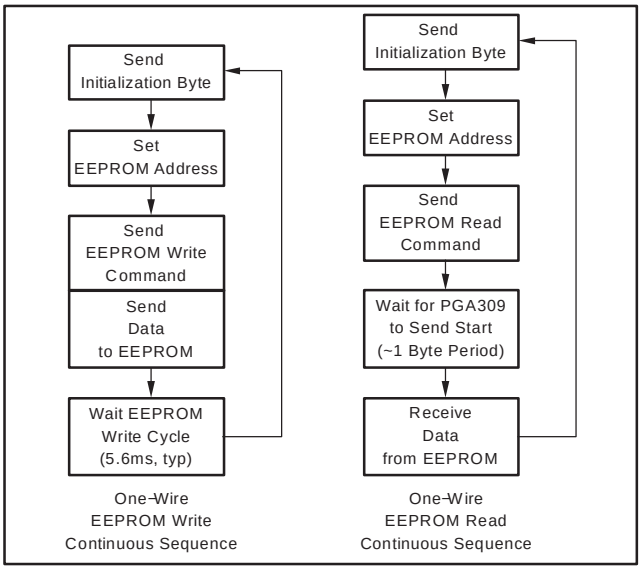


Figure 50. One-Wire Access to External EEPROM

One-Wire Interface Timing Considerations

Figure 51 illustrates the key timing and jitter considerations for the One-Wire interface and Table 29 contains the specifications for ensured, reliable operation. Although the One-Wire baud rate can change from transaction to transaction, within a transaction it must remain within ±1% of its initialization byte value.

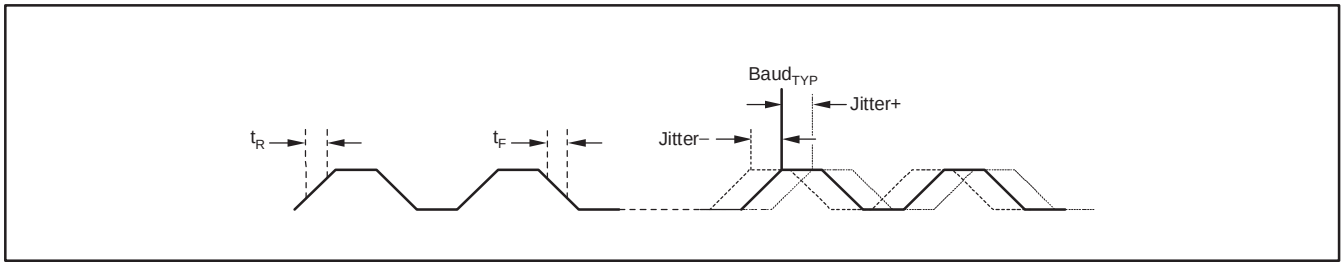


Figure 51. One-Wire Timing Diagram

PARAMETER	MIN	TYP	MAX	UNITS
Baud	4.8K		38.4K	Bits/s
Rise Time, t_R			0.5	%Baud
Fall Time, t_F			0.5	%Baud
Jitter(1)			±1	%Baud

(1) Transmit jitter from controller to PGA309. Standard UART interfaces will accept data sent from the PGA309 during One-Wire transactions.

Table 29. One-Wire Timing Diagram Definitions

Two-Wire Access to External EEPROM

The read and write timing for the PGA309 interface to the external EEPROM when the PGA309 receives commands through the One-Wire interface (PRG pin) is shown in Figure 52. If direct Two-Wire access is made to the external EEPROM, all manufacturer reading and writing modes are allowed. Note that the PGA309 One-Wire access to the external EEPROM through the PGA309 Two-Wire interface supports full 10-bit EEPROM addressing mode. This allows the user to store other configuration information in a larger than needed external EEPROM, since a 1K EEPROM is the largest needed for PGA309 configuration register and Lookup Table coefficients. In addition, please note that the PGA309 SCL and SDA pins have light internal pull-up current sources to V_{SD} (85µA typical on each pin). This is more than adequate for most applications that involve placing only the external EEPROM close to the PGA309 on the same printed circuit board (PCB). Other applications that add load and capacitance to the SDA and SCL lines may need additional external pull-up resistors to V_{SD} to ensure the rise timing requirements are met at all times. At the end of a EEPROM write cycle, there is a typical 5ms EEPROM write cycle during which the data is stored in a nonvolatile fashion internally to the EEPROM. During this time, if Two-Wire direct access is attempted, there will be no acknowledge from the EEPROM. If communicating to the external EEPROM through the PGA309 One-Wire interface, this EEPROM write cycle time is a “No Communication Allowed” time period.

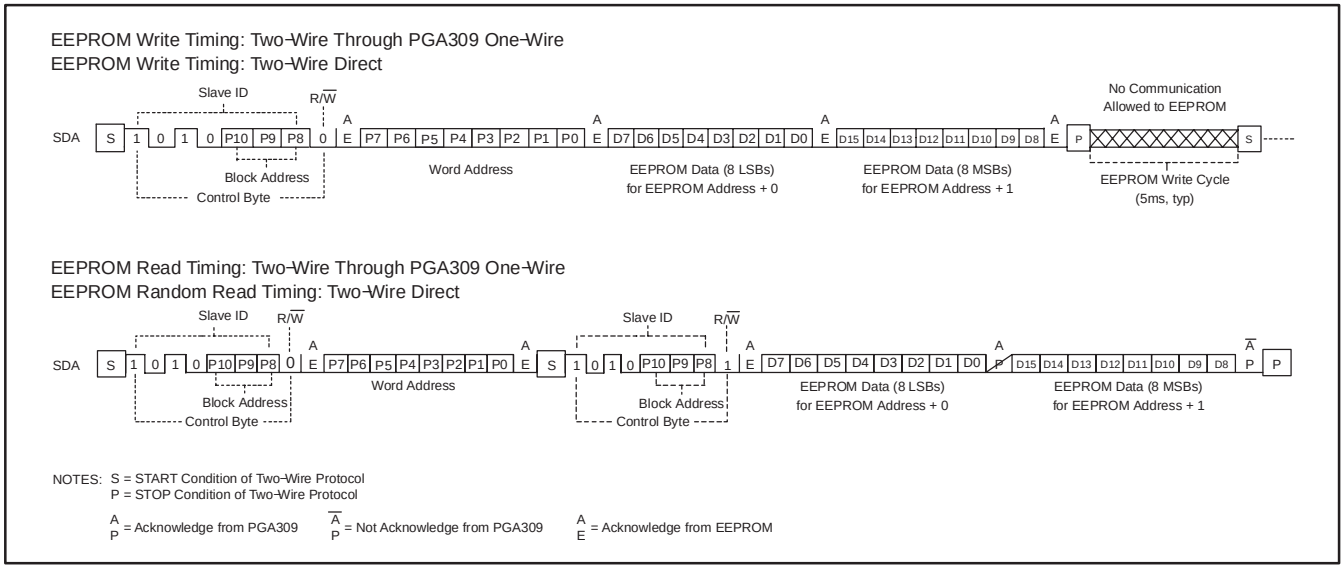


Figure 52. Two-Wire Access to External EEPROM Timing

One-Wire Interface Initiated Two-Wire EEPROM Transactions

The Write EEPROM and Read EEPROM commands initiate a communication transaction on the Two-Wire bus between the PGA309 and the EEPROM device (see Figure 52). The Write EEPROM command causes the PGA309 to generate a Two-Wire start condition and send a Two-Wire slave address byte to the EEPROM device with the four MSBs set to '1010' and the three LSBs set to bits 10−8 of the EEPROM address pointer. The R/$\overline{W}$ bit is set to '0' to indicate a write instruction. If the PGA309 receives an acknowledge from the EEPROM device, it then sends a byte with eight LSBs of the EEPROM address pointer. If the PGA309 receives an acknowledge from this byte, the PGA309 sends the least significant byte of the data to the EEPROM. Upon successful receipt of an acknowledge to this byte, the PGA309 transmits the most significant byte. After the acknowledge bit of this byte, the PGA309 generates a Two-Wire stop condition to terminate data transfer to the EEPROM. The Read EEPROM command causes the PGA309 to generate a Two-Wire start condition and send a Two-Wire slave address byte to the EEPROM with the four MSBs set to '1010', the three LSBs set to bits 10−8 of the EEPROM Address Pointer, and the R/$\overline{W}$ bit set to '0' to indicate a write instruction. If the PGA309 receives an acknowledge from the EEPROM device, it will then send a byte with the eight LSBs of the EEPROM address pointer. If the PGA309 receives an acknowledge from this byte, the PGA309 generates another Two-Wire START condition, send another slave address byte but this time with the R/$\overline{W}$ bit set to '1' to indicate a read instruction. If the PGA309 receives an acknowledge, it continues to clock the SCL line to receive the first byte from the EEPROM, acknowledge this byte, receive the second byte, not acknowledge the second byte to terminate data transfer, and then generate a Two-Wire STOP condition.

PGA309 Stand-Alone Mode and Two-Wire Transactions

In Stand-Alone mode (see Operating Modes section), the PGA309 accesses the external EEPROM in a different fashion than that presented for the *One-Wire Interface Initiated Two-Wire Transactions*. If all other POR conditions have been met to allow a PGA309 to allow access to a properly programmed external EEPROM, the PGA309 will first access the first part of the external EEPROM (configuration register data) as shown in Figure 53.

If the Checksum1 is correct and the PGA309 is triggered to read the second part of the EEPROM, it will proceed as shown in Figure 54. If the One-Wire disable bit, OWD, bit 15, in Register 4 is set to '1' then after initial POR and following a valid Checksum2, the One−Wire interface is disabled and the PRG pin becomes high impedance and One-Wire communication cannot take place unless power is cycled. This is part of the provisions to allow for direct connection of the PRG pin to V_{OUT}.

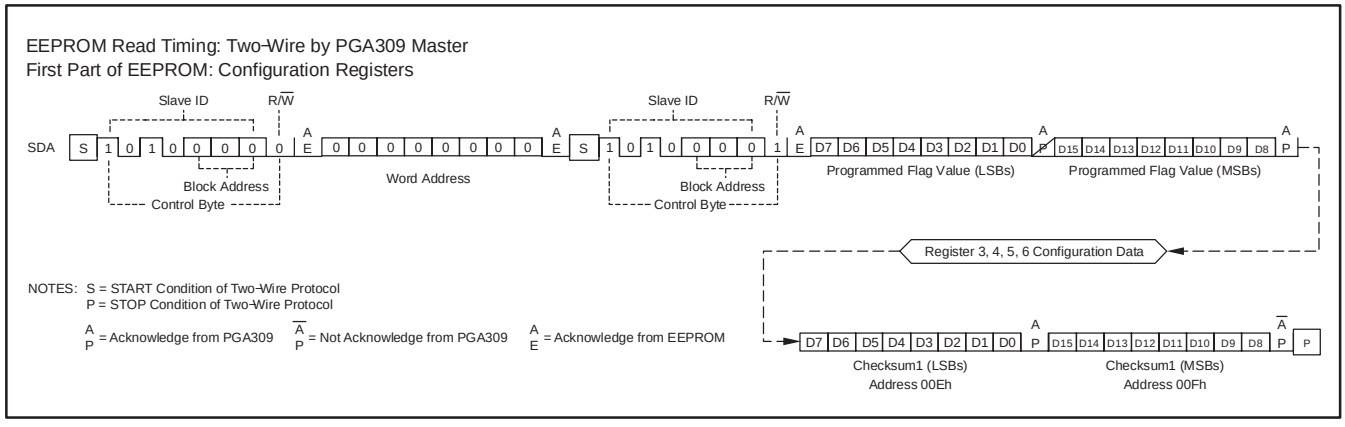


Figure 53. First Part of External EEPROM Timing for Stand-Alone Mode

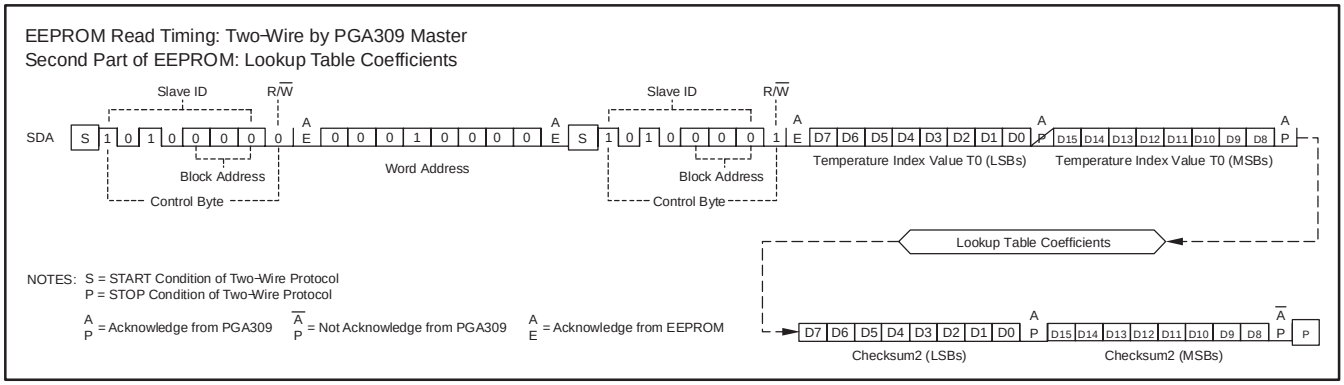


Figure 54. Second Part of External EEPROM Timing for Stand-Alone Mode

PGA309 Two-Wire Bus Master Operation and Bus Sharing Considerations

Whenever the PGA309 is called upon to communicate to the external EEPROM, the PGA309 needs to become the master on the Two-Wire interface bus. In order to do this in a reliable and orderly fashion, the PGA309 contains several monitors and algorithms to check for bus availability, prevent bus contention in case other devices are connected in parallel with the External EEPROM, and fault diagnostics to attempt to free a stuck bus.

If the PGA309 is ever addressed on its Two-Wire or One-Wire interface, with it providing a successful acknowledge, it will cease all transactions as a master on the Two-Wire bus and give up control for one second. Each time the PGA309 is addressed on the Two-Wire bus, the one second timeout is reset (see Figure 55).

Figure 56 details the algorithms used by the PGA309 when it wants to become master on the Two-Wire bus. A 25ms timer is started. Now SCL is monitored for being low. If SCL is not low, the PGA309 checks to see if communication on the Two-Wire bus is between a START and a STOP. If the bus communication is between a START and a STOP, the PGA309 waits for the 25ms timer to time out, and then checks if SDA is low. If SDA is not low, the PGA309 has an opportunity to become bus master (SCL = SDA = '1') and takes it. During the 25ms interval, if there is any SCL activity, the 25ms timer will restart.

If SCL remains low for the entire 25ms timer countdown, the PGA309 waits 25ms before starting the 25ms timer again to begin the check of the bus for an idle state (SDA = SCL = '1').

If SDA is low after the 25ms timer counts down, the PGA309 interprets this as a *stuck-bus* condition. The PGA309 attempts to free the stuck bus by sending up to ten clocks down SCL to free up SDA. If it is successful in causing SDA to go high, the PGA309 sends a START and then STOP sequence to ensure whichever device was causing the stuck bus is completely reset. Now the bus should be in an idle state (SDA = SCL = '1') and the PGA309 can become the master on the bus.

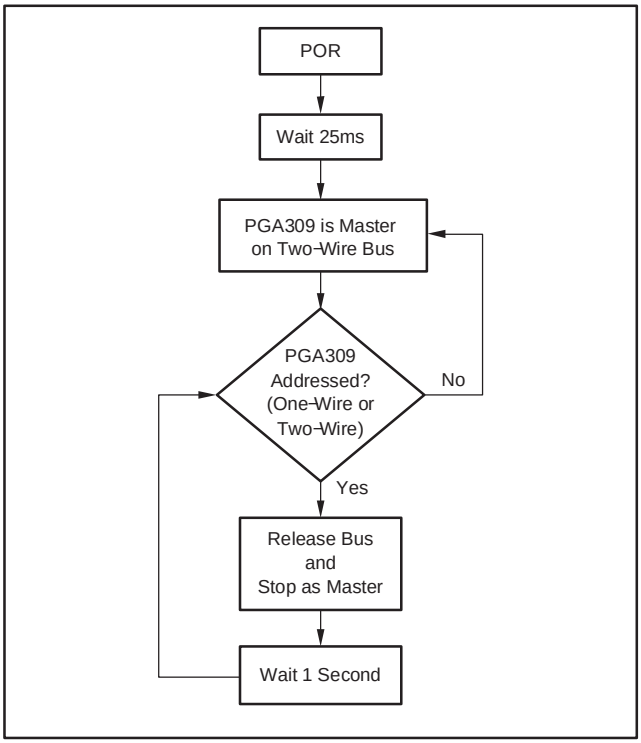


Figure 55. Two-Wire Bus Relinquish by PGA309 in Master Mode

If the PGA309 is communicating on the bus as a master and it sees contention, the PGA309 will release the bus and retry in 25ms. Contention is defined as the PGA309 wanting SCL high and SCL is low, or wanting SDA high and SDA is low.

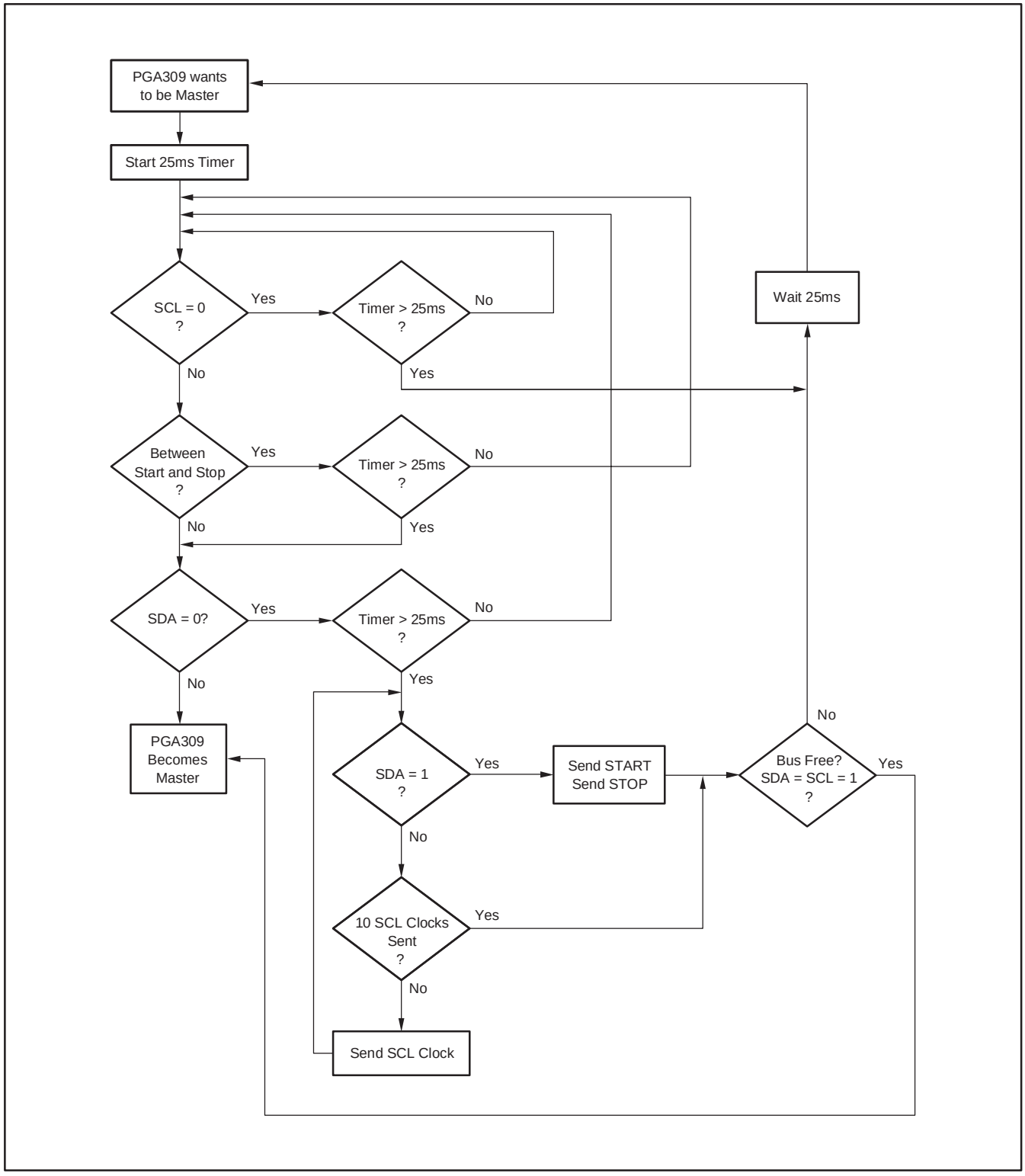


Figure 56. Two-Wire Bus Master Algorithm

One-Wire Operation with PRG Connected to V_{OUT}

In some sensor applications, it is desired to provide the end-user of the sensor module with three pins, V_S, GND, and Sensor Out. It is also desired in these applications to digitally calibrate the sensor module after its final assembly of sensor and electronics. The PGA309 has a mode that allows the One-Wire interface pin (PRG) to be tied directly to the PGA309 output pin (V_{OUT}), as shown in Figure 57.

For the PGA309 + sensor calibration, it is necessary to configure and reconfigure internal registers on the PGA309 and then measure the analog voltage on V_{OUT} as a result of these register value settings. To do this while V_{OUT} is tied to PRG requires the ability to enable and disable V_{OUT}. This allows a multiplexing operation between PRG using the connection as a bidirectional digital interface and V_{OUT} driving the connection as a conditioned sensor output voltage. In addition, it is convenient to configure the Temp ADC for Single Start Convert mode and delay the start of the Temp ADC until after V_{OUT} is enabled and internal circuitry has had a chance to settle to accurate final values. This is especially important in applications that use the linearization circuitry, tie the sensor to V_{EXC}, and measure temperature external to the PGA309 (i.e., temperature sense series resistor in the upper or lower excitation leg of the bridge sensor).

Register 7 (Output Enable Counter Control Register) contains the control bits for setting both the amount of time V_{OUT} is active on the common connection and also the delay from V_{OUT} enabled to the start of a Temp ADC conversion. These individual bits are defined in Table 30 and Table 31.

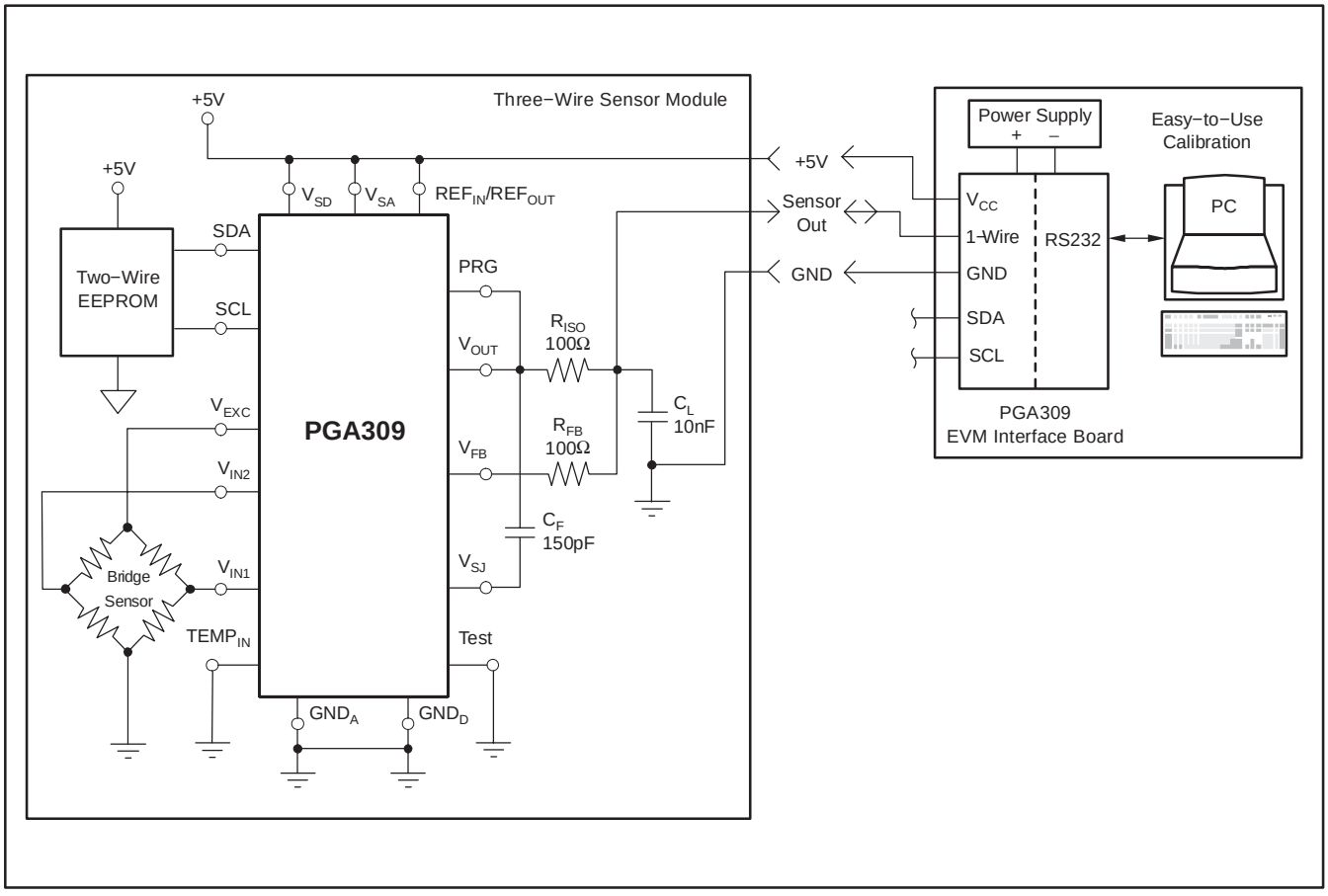


Figure 57. One-Wire Operation with PRG Tied to V_{OUT}

DLY 3 [11]	DLY 2 [10]	DLY 1 [9]	DLY 0 [8]	DECIMAL EQUIVALENT (INITIAL COUNTER VALUE)	TEMP ADC DELAY (ms)
0	0	0	0	0	0
0	0	0	1	1	10
0	0	1	0	2	20
0	0	1	1	3	30
0	1	0	0	4	40
0	1	0	1	5	50
0	1	1	0	6	60
0	1	1	1	7	70
1	0	0	0	8	80
1	0	0	1	9	90
1	0	1	0	10	100
1	0	1	1	11	110
1	1	0	0	12	120
1	1	0	1	13	130
1	1	1	0	14	140
1	1	1	1	15	150
NOTE: Temp ADC delay = intial counter value x 10ms.					

Table 30. Temp ADC—Delay After V_{OUT} Enable (Register 7)

DIGITAL INPUT (BINARY) OEN7……OEN0 [7……0]	DECIMAL EQUIVALENT (INITIAL COUNTER VALUE)	V_{OUT} ENABLE TIMEOUT (ms)
0000 0000	0	0 (V_{OUT} Disabled)
0010 0000	32	320
0100 0000	64	640
0110 0000	96	960
1000 0000	128	1280
1010 0000	160	1600
1100 0000	192	1920
1110 0000	224	2240
1111 1111	255	2550
NOTE: V_{OUT} enable timeout = inital counter value x 10ms.		

Table 31. Output Enable Counter for One-Wire Interface/V_{OUT} Multiplexed Mode (Register 7)

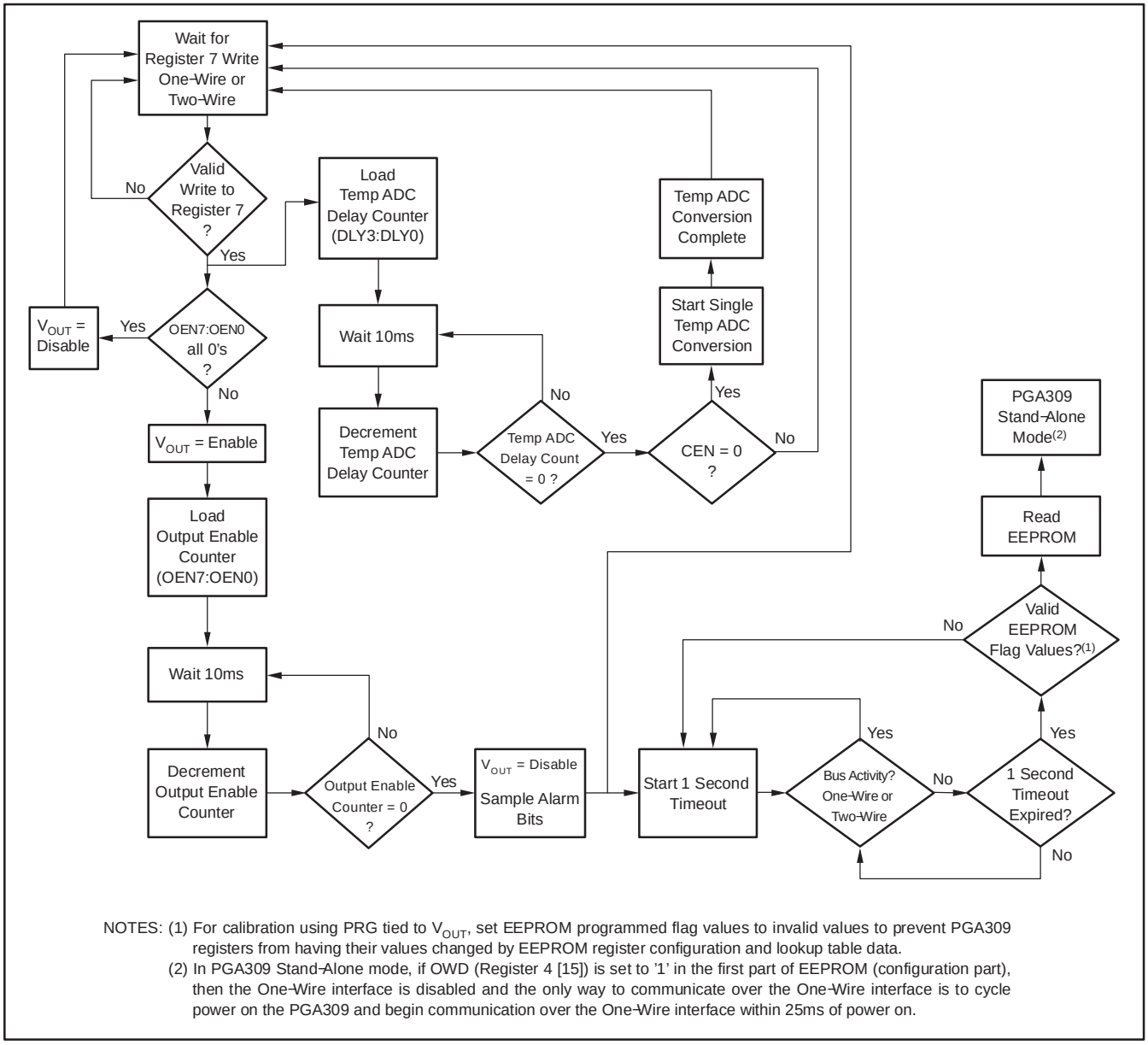
Figure 58 details the output enable/disable state machine. Upon initial POR, there is 25ms for communication through either digital interface to prevent the PGA309 from going through its POR sequence and reaching Stand-Alone mode. At any time the PGA309 is powered and either digital interface (One-Wire or Two-Wire) can write to Register 7, the output enable/disable state machine can be forced to run. Writing a non-zero value to OEN7:OEN0 will cause V_{OUT} to be immediately enabled and the Output Enable Counter to be loaded with the OEN7:OEN0 value (decimal equivalent x 10ms = initial Output Enable Counter value). V_{OUT} remains enabled until this initial Output Enable Counter value is decremented to 0 by 10ms increments. V_{OUT} is then disabled and a one second timeout begun waiting for bus activity on either digital interface (PRG pin for three-wire sensor application). As long as there is activity on the PRG pin, the one second timeout will be continually reset. After one second of no bus activity, the PGA309 stops and the state machine will try to read the EEPROM. It is important to store *invalid* data in the programmed flag values of the EEPROM for this calibration process, to prevent it from being read, which could change the register settings in the PGA309. This will also force the one second timeout to be reset and allow as long as needed for communication to start and stop on PRG. Once all registers in the PGA309 have been set to their desired values, another write to Register 7 will start the process all over again so a new analog value of V_{OUT} can be measured.

The second part of the output enable/disable state machine is the Temp ADC delay. During calibration, it will be desired to read the Temp ADC conversion result at different absolute calibration temperatures. These readings combined with measured V_{OUT} at these respective temperatures are used to calculate the final temperature coefficients to be stored in the Lookup Table part of the external EEPROM. To use this function, the Temp ADC must be set to Single Start Convert mode (CEN = 0, Register 6 [10]). After a write to Register 7, the Temp ADC delay counter is loaded with the DLY3:DLY0 value (decimal equivalent x 10ms = initial Temp ADC delay counter value). This initial Temp ADC delay counter value is decremented to 0 by 10ms increments. When it reaches 0, a single Temp ADC conversion is triggered. No additional write to Register 6 [12] (the ADCS bit) is needed to initiate the conversion. Upon completion of the conversion, this branch of the state machine returns to waiting for the next valid Register 7 write.

The output enable/disable state machine allows three-wire sensor applications to measure temperature through the PGA309, against the calibration standard, for the PGA309 + sensor combination. It also allows PGA309 + sensor characteristics over pressure and temperature to be measured through the PGA309. These real-world results allow for accurate calculation of temperature coefficients for the Lookup Table and therefore, accurate PGA309 + sensor digital calibration on a module-by-module basis.

The values of the Fault Monitor Alarm bits are latched immediately before the output is disabled to allow their values to be read through the One-Wire interface during factory calibration.

Once the final values are to be programmed into the EEPROM, it is desirable to have the One-Wire Interface disabled in three-wire sensor applications. This prevents V_{OUT} changes in the final end-use from being read back into the PGA309 through the One-Wire interface (PRG pin) and potentially misinterpreted as bus activity, which could then cause V_{OUT} to become disabled. To disable the One-Wire Interface, set the OWD bit to '1' during the final EEPROM program write. The OWD (One-Wire Disable) bit is located in Register 4 [15]. After this final programming, all is not lost as any power-up sequence will allow the One-Wire Interface (PRG pin) control if communication is initiated within 25ms of the application of power to the PGA309.



NOTES: (1) For calibration using PRG tied to V_{OUT}, set EEPROM programmed flag values to invalid values to prevent PGA309 registers from having their values changed by EEPROM register configuration and lookup table data.
(2) In PGA309 Stand-Alone mode, if OWD (Register 4 [15]) is set to '1' in the first part of EEPROM (configuration part), then the One-Wire interface is disabled and the only way to communicate over the One-Wire interface is to cycle power on the PGA309 and begin communication over the One-Wire interface within 25ms of power on.

Figure 58. Output Enable/Disable State Machine

APPLICATION BACKGROUND

A typical bridge pressure sensor is shown in Figure 59. For a given bridge excitation voltage (V_{EXC}), the output voltage of the bridge ($V_{INP} - V_{INN}$) is a voltage proportional to the pressure applied to the sensor.

Span is the scale factor for $V_{INP} - V_{INN}$ at full-scale pressure input relative to the bridge excitation ($V_{BR+} - V_{BR-}$). Span is also called FSO (Full-Scale Output), FSS (Full-Scale Sensitivity), Sensitivity, or Gain. For example, with a bridge excitation voltage of 5V, a 2mV/V FSS implies that the bridge output will be 10mV at full-scale pressure.

Offset, also known as Zero, is the output of the bridge ($V_{INP} - V_{INN}$) with zero pressure applied. Often a bridge sensor's Zero may be equal to or greater than its FSS for a given excitation voltage. Figure 60 graphically illustrates the definition of Span and Offset.

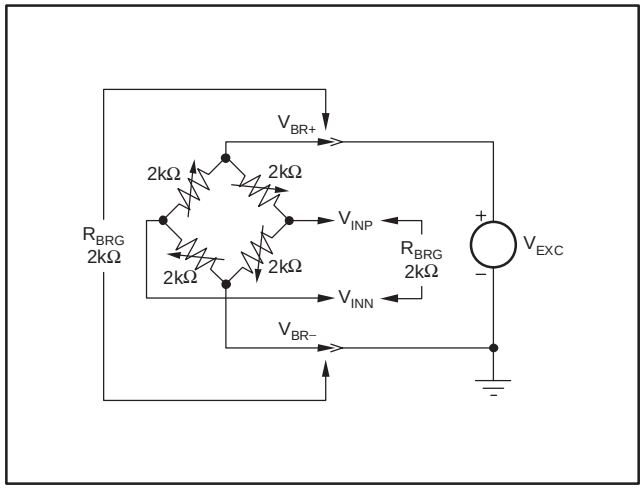


Figure 59. Typical Bridge Sensor

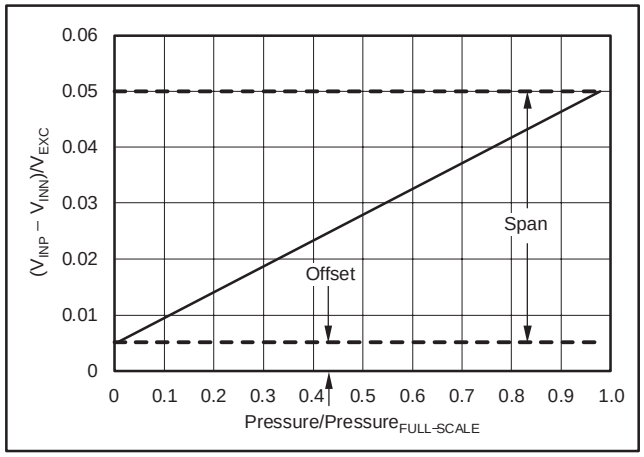


Figure 60. Example of Span and Offset

An ideal sensor would have span and offset curves over temperature, as shown in Figure 3. Real-world sensors have span and offset changes that change over temperature. Both span and offset have variations at +25°C, linear changes with temperature, and nonlinear changes with temperature. Figure 4 and Figure 5 illustrate span and offset changes over temperature for a bridge sensor with second-order nonlinearities. TC1 coefficients represent a linear change with temperature, and TC2 a second-order change with temperature.

Many bridge sensors have a nonlinear output with applied pressure. Figure 64 shows the non-ideal curves for both a positive and negative nonlinear bridge sensor output with applied pressure. The PGA309 provides calibration over temperature for both span and offset and has dedicated linearization circuitry to linearize many types of bridge sensors whose outputs are not linear with applied pressure.

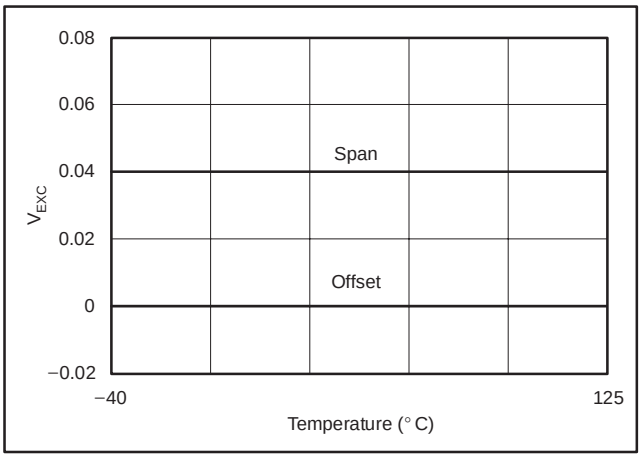


Figure 61. Ideal Span and Offset vs Temperature

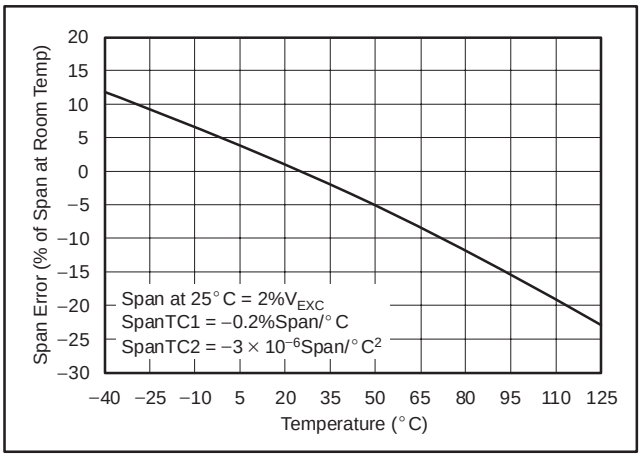


Figure 62. Effect of Nonlinearity on Bridge Sensor Span Over Temperature

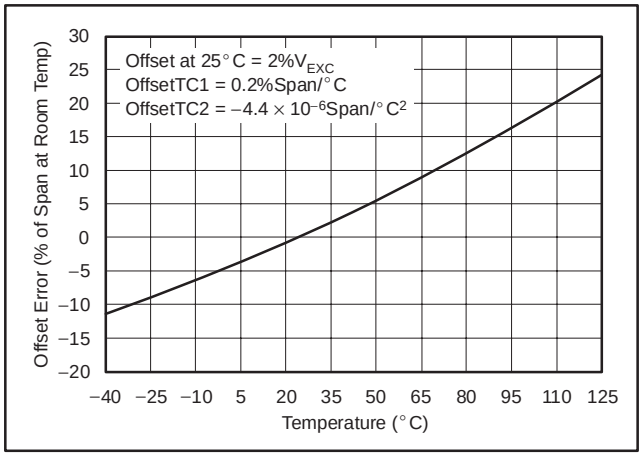


Figure 63. Effect of Nonlinearity on Bridge Sensor Offset Over Temperature

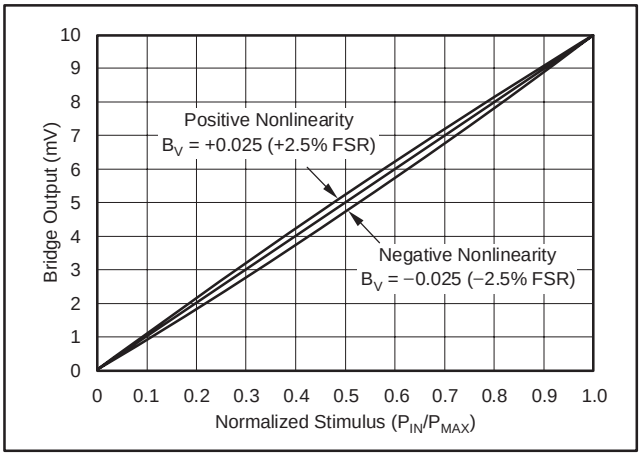


Figure 64. Non-Ideal Curves for Both a Positive and Negative Nonlinear Bridge Sensor Output with Applied Pressure

SYSTEM SCALING OPTIONS FOR BRIDGE SENSORS

There are two system scaling options for bridge sensor outputs: Absolute Scale and Ratiometric Scale.

Absolute Scale

Absolute Scale conditions the output range to be scaled as a percentage of a reference voltage, V_{REF}. For example, the absolute-scaled output of a bridge sensor can be set to the range of 10% to 90% of V_{REF}. Figure 65 illustrates such a case.

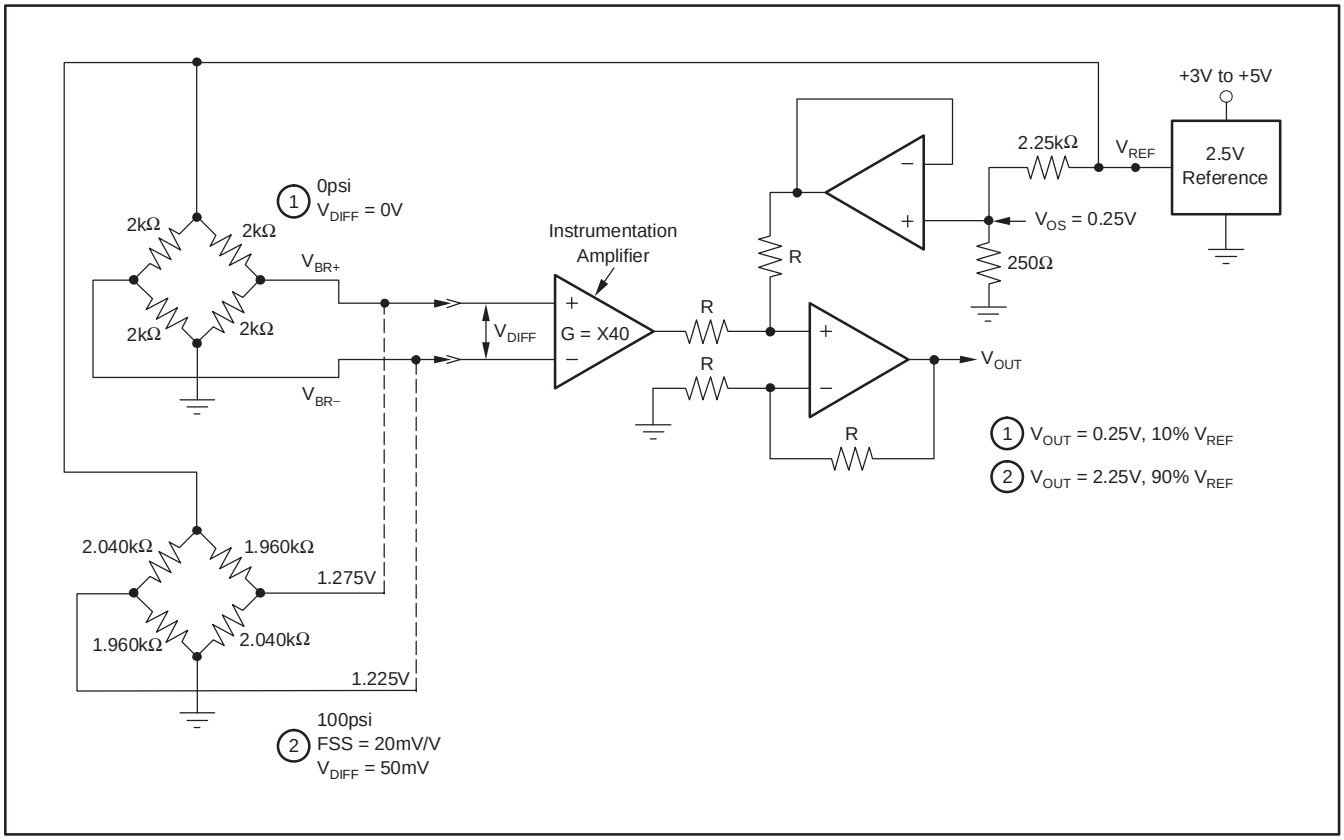


Figure 65. Absolute Scaling Conditions

Ratiometric Scale

Ratiometric Scale conditions the output range to be scaled as a percentage of the supply voltage. For example, the ratiometric-scaled output of a bridge sensor can be set to the range of 10% to 90% of V_S. Figure 66 illustrates such a case. Figure 67 shows that as the supply voltage, V_S, is lowered from +5V to +3V the range for V_{OUT} of 10% to 90% of V_S remains the same. The PGA309 accommodates both Absolute and Ratiometric scaling of bridge sensors.

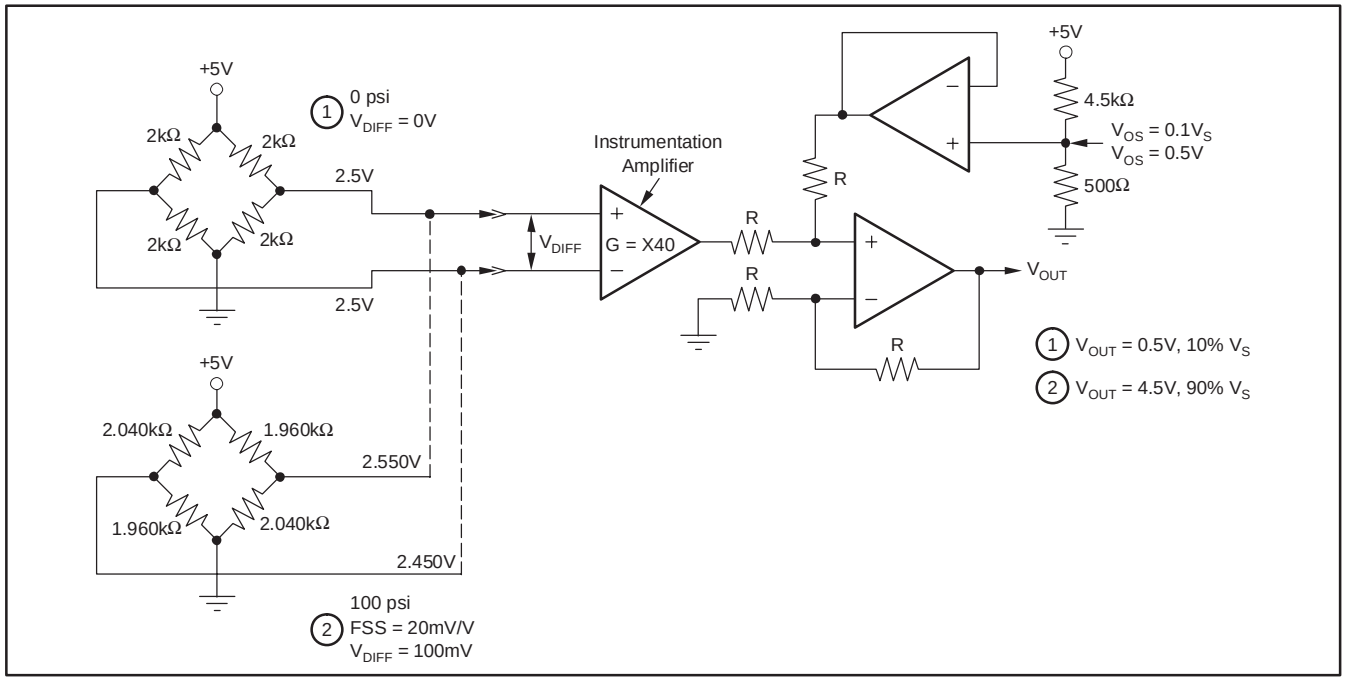


Figure 66. Ratiometric Configuration, 5V

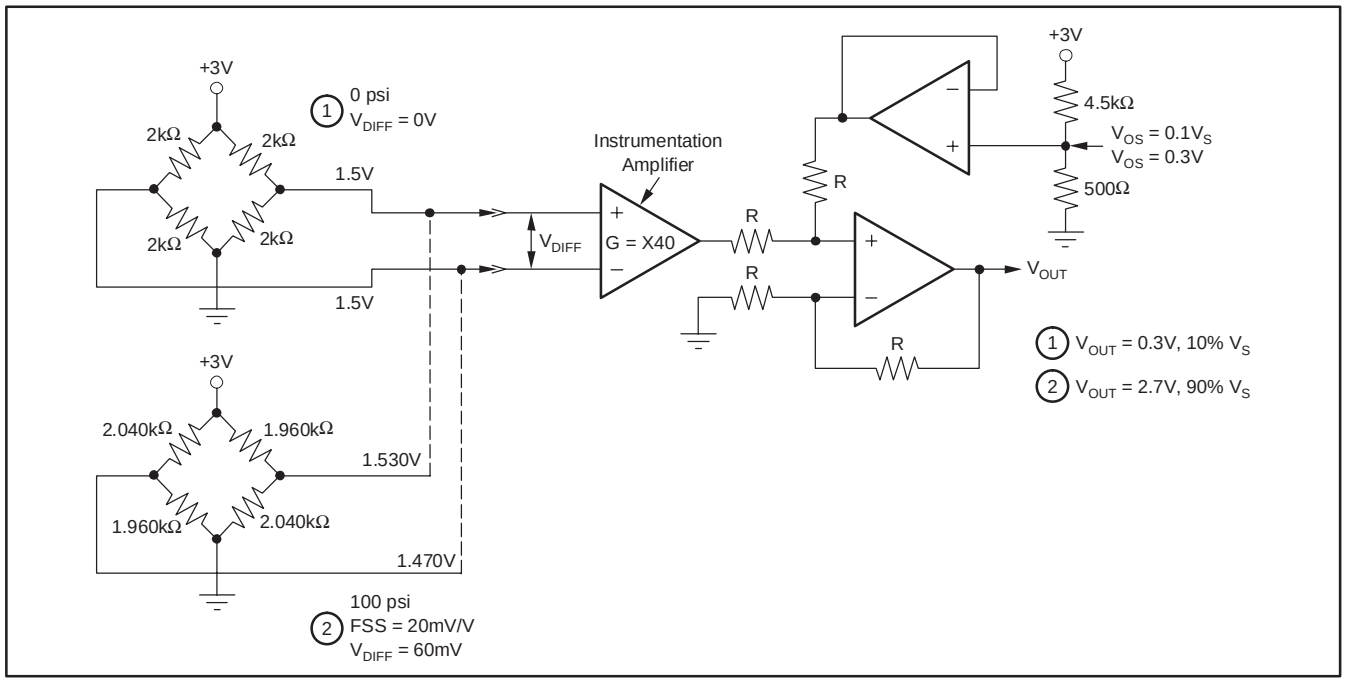


Figure 67. Ratiometric Configuration, 3V

TRIMMING REAL WORLD BRIDGE SENSORS FOR LINEARITY

Traditional methods for trimming nonlinear, real-world bridge sensors to a linear, useful function require additional resistors to be added around the base bridge sensor, as shown in Figure 68. This approach often requires special prepackaged fixtures and special laser trim or manual trim resistors. The trims are interactive with each other, which requires multiple test/trim/test/trim passes and this only allows for a finite number of trims and range for a particular bridge sensor.

The PGA309 provides a modern digital trim approach for bridge sensors, as shown in Figure 69. This technique allows for post-package trim of both the bridge sensor and its signal conditioning electronics. The digital trimming is simplified through the use of a computer interface and spreadsheet analysis computation tools. A near infinite number of trim cycles can be performed with finer resolution, wider range, and less interaction between trimmed parameters than the traditional trim. Packaging shifts are eliminated.

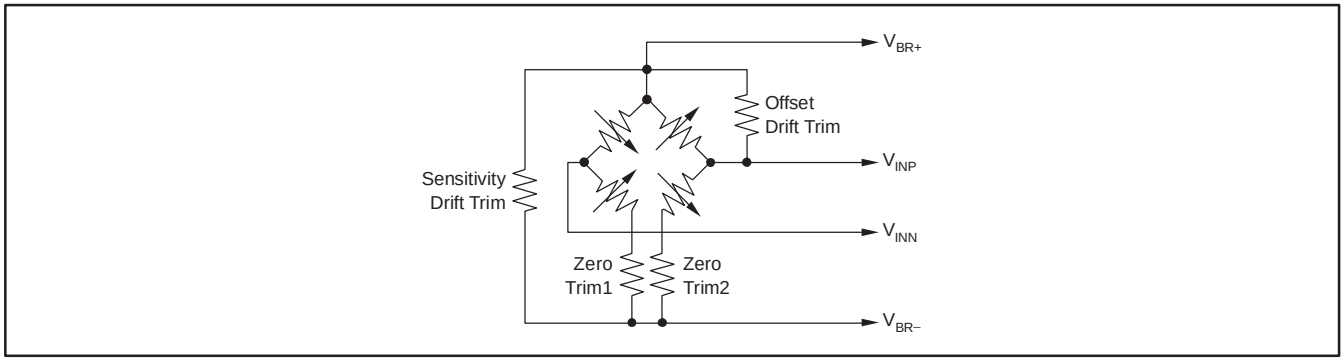


Figure 68. Typical Trim Configuration

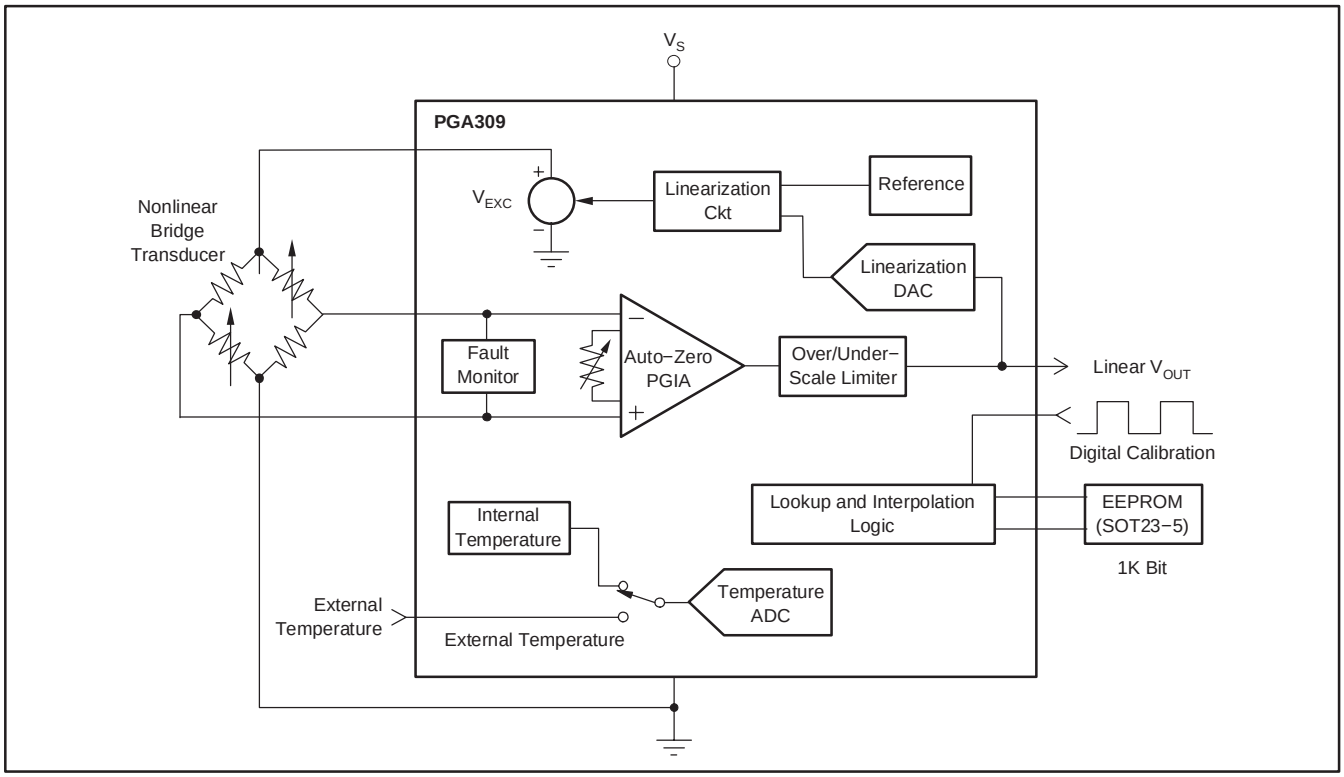


Figure 69. PGA309 Trim Configuration

REGISTER DESCRIPTIONS

PGA309 INTERNAL REGISTER OVERVIEW

ADDRESS POINTER					REGISTER DESCRIPTION	TYPE(1)	REGISTER CONTROLS
P4	P3	P2	P1	P0			
0	0	0	0	0	Register 0—Temp ADC Output	R	Temp ADC Output Data
0	0	0	0	1	Register 1—Fine Offset Adjust (Zero DAC)	R/W	Fine Offset Adjust (Zero DAC) Setting
0	0	0	1	0	Register 2—Fine Gain Adjust (Gain DAC)	R/W	Fine Gain Adjust (Gain DAC) Setting
0	0	0	1	1	Register 3—Reference Control and Linearization Register	R/W	Reference Configuration Settings; V_{EXC} Enable; Linearization Setting
0	0	1	0	0	Register 4—Front End PGA Coarse Offset Adjust and Gain Select; Output Amplifier Gain Select	R/W	Front End PGA Coarse Offset Setting; PGA Gain Select; Output Amplifier Gain Select; One-Wire Disable
0	0	1	0	1	Register 5—PGA Configuration and Over/Under Scale Limit	R/W	Over/Under Scale Limits, Polarities, Enable; Fault Comparator Select
0	0	1	1	0	Register 6—Temp ADC Control Register	R/W	Temp ADC Conversion Speed, Ref Select; Int/Ext Temp Mode Select; Ext Temp PGA Configuration; $TEMP_{IN}$ Current Source Enable
0	0	1	1	1	Register 7—Output Enable Counter Control	R/W	Temp ADC Delay Setting; One-Wire Interface Output Enable Setting
0	1	0	0	0	Register 8—Alarm Status	R	Fault Monitor Comparator Outputs

(1) Type: R = Read-only, R/W = Read/Write

Table 32. PGA309 Internal Register Overview

INTERNAL REGISTER MAP

Register 0: Temp ADC Output Register (Read Only, Address Pointer = 00000)

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Descriptions:

AD[15:0] Temp ADC Output

Internal Temperature Mode: 12-bit + sign extended, right justified, Two's Complement data format
External Temperature Mode: 15-bit + sign extended, right-justified, Two's Complement data format

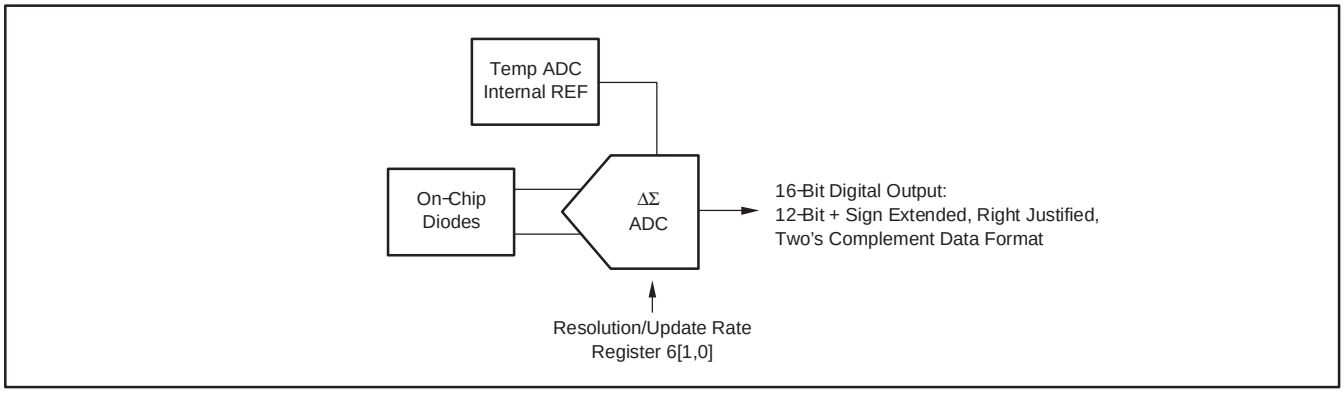


Figure 70.

TEMPERATURE (°C)	DIGITAL OUTPUT AD15.....AD0 (BINARY)	DIGITAL OUTPUT (HEX)
150	0000 1001 0110 0000	0960
128	0000 1000 0000 0000	0800
127.9375	0000 0111 1111 1111	07FF
100	0000 0110 0100 0000	0640
80	0000 0101 0000 0000	0500
75	0000 0100 1011 0000	04B0
50	0000 0010 0010 0000	0320
25	0000 0001 1001 0000	0190
0.25	0000 0000 0000 0100	0004
0.0	0000 0000 0000 0000	0000
−0.25	1111 1111 1111 1100	FFFC
−25	1111 1110 0111 0000	FE70
−55	1111 1100 1001 0000	FC90

Table 33. Internal Temperature Mode—Data Format (12-Bit Resolution). TEN = 1; R_1, R_0 = '11'

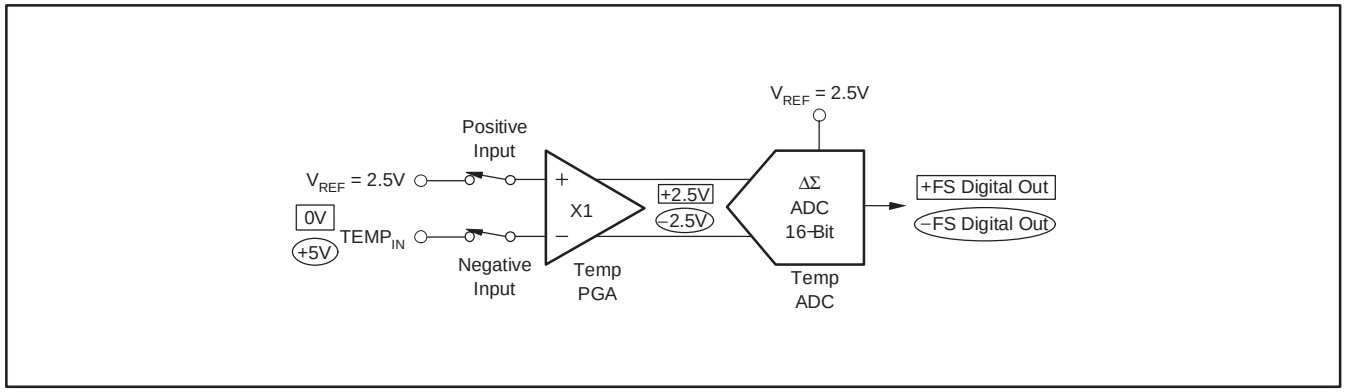


Figure 71.

$TEMP_{IN}$ (V)	TEMP ADC INPUT (V)	TEMP ADC INPUT (RATIO TO FULL SCALE)(1)	DIGITAL OUTPUT AD15.....AD0 (BINARY)	DIGITAL OUTPUT (HEX)
+0.0001	+2.49992371	+0.999969 V_{REFT}	0111 1111 1111 1111	7FFF
+0.625	+1.875	+0.75 V_{REFT}	0110 0000 0000 0000	6000
+1.25	+1.25	+0.5 V_{REFT}	0100 0000 0000 0000	4000
+1.925	+0.575	+0.23 V_{REFT}	0001 1101 0111 0001	1D71
+2.4999	+76.29µ	+(1/32768) V_{REFT}	0000 0000 0000 0001	0001
+2.5	0	+0 V_{REFT}	0000 0000 0000 0000	0000
+2.50007629	−76.29µ	−(1/32768) V_{REFT}	1111 1111 1111 1111	FFFF
+3.075	−0.575	−0.23 V_{REFT}	1110 0010 1000 1111	E28F
+3.75	−1.25	−0.5 V_{REFT}	1100 0000 0000 0000	C000
+4.375	−1.875	−0.75 V_{REFT}	1010 0000 0000 0000	A000
+5	−2.5	−1 V_{REFT}	1000 0000 0000 0000	8000

(1) V_{REFT} can be V_{SA}, V_{EXC}, or V_{REF}.

Table 34. External Signal Mode—Data Format Example (Register 6 = ‘0000 0100 0011 0011’), 15-Bit + Sign Resolution. REN = 1, RS = 1.

Register 1: Fine Offset Adjust (Zero DAC) Register (Read/Write, Address Pointer = 00001)

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	ZD15	ZD14	ZD13	ZD12	ZD11	ZD10	ZD9	ZD8	ZD7	ZD6	ZD5	ZD4	ZD3	ZD2	ZD1	ZD0
POR VALUE	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Descriptions:

ZD[15:0]: Zero DAC control, 16-bit unsigned data format

DIGITAL INPUT (HEX)	DIGITAL INPUT ZD15.....ZD0 (BINARY)	ZERO DAC OUTPUT (V)	ZERO DAC OUTPUT
0000	0000 0000 0000 0000	0	0 V_{REF}
0001	0000 0000 0000 0001	0.00007629	(1/65536) V_{REF}
051F	0000 0101 0001 1111	0.100021362	0.02 V_{REF}(1)
4000	0100 0000 0000 0000	1.25	0.25 V_{REF}
8000	1000 0000 0000 0000	2.5	0.50 V_{REF}
C000	1100 0000 0000 0000	3.75	0.75 V_{REF}
FAE1	1111 1010 1110 0001	4.899978638	0.98 V_{REF}(1)
FFFF	1111 1111 1111 1111	4.999923706	0.9999847 V_{REF}
(1) Ensured by design Zero DAC Range of Adjustment (0.02V_{REF} to 0.98V_{REF})			

Table 35. Zero DAC—Data Format Example (V_{REF} = +5V)

Zero DAC Equation:

Decimal # Counts = $V_{ZERO\ DAC}$ / (V_{REF}/65536)

Zero DAC Example:

Want: $V_{ZERO\ DAC}$ = 0.5V
Given: V_{REF} = 5V
Decimal # Counts = 0.5 / (5/65536) = 6553.6
Use 6554 counts → 0x199A → 0001 1001 1001 1100

Register 2: Fine Gain Adjust (Gain DAC) Register (Read/Write, Address Pointer = 00010)

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	GD15	GD14	GD13	GD12	GD11	GD10	GD9	GD8	GD7	GD6	GD5	GD4	GD3	GD2	GD1	GD0
POR VALUE	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Descriptions:

GD[15:0]: Gain DAC control, 16-bit unsigned data format

DIGITAL INPUT (HEX)	DIGITAL INPUT ZD15.....ZD0 (BINARY)	GAIN ADJUST
0000	0000 0000 0000 0000	0.333333333
0001	0000 0000 0000 0001	0.333343505
32F2	0011 0010 1111 0010	0.466003417
4000	0100 0000 0000 0000	0.500000000
6604	0101 0101 0000 0100	0.598999023
9979	1001 1001 0111 1001	0.733001708
CC86	1100 1100 1000 0110	0.865997314
FFFF	1111 1111 1111 1111	1.000000000

Table 36. Gain DAC—Data Format

Gain DAC Equation:

1 LSB = (1.000000000 – 0.333333333) / 65536 = 1.0172526×10^{-5}

Decimal # counts = (Desired Gain – 0.333333333) / (1.0172526×10^{-5})

Gain DAC Example:

Want: Fine Gain = 0.68

Decimal # counts = (0.68 – 0.333333333) / (1.0172526×10^{-5}) = 34,078.72

Use 34079 counts → 0x851F → 1000 0101 0001 1111

Register 3: Reference Control and Linearization Register (Read/Write, Address Pointer = 00011)

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	RFB	RFB	RFB	SD	EXS	EXEN	RS	REN	LD7	LD6	LD5	LD4	LD3	LD2	LD1	LD0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Descriptions:

RFB: **Reserved Factory Bit: Set to zero for proper operation**

SD: **Analog Shutdown Mode for Internal Controlled Power-Up (0 = enabled, 1 = disabled)**

EXS: **Linearization Adjust and Excitation Voltage (V_{EXC}) Gain Select (Range1 or Range2)**
0 = Range 1 ($-0.166V_{FB}$ < Linearization DAC Range < $+0.166V_{FB}$, V_{EXC} Gain = $0.83V_{REF}$)
1 = Range 2 ($-0.124V_{FB}$ < Linearization DAC Range < $+0.124V_{FB}$, V_{EXC} Gain = $0.52V_{REF}$)

EXEN: **V_{EXC} Enable**
1 = Enable V_{EXC}
0 = Disable V_{EXC}

RS: **Internal V_{REF} Select (2.5V or 4.096V)**
0 = 4.096V
1 = 2.5V

REN: **Enable/Disable Internal V_{REF} (disable for external V_{REF}—connect external V_{REF} to REF_{IN}/REF_{OUT} pin)**
0 = External Reference (disable internal reference)
1 = Internal Reference (enable internal reference)

LD[7:0]: Linearization DAC setting, 7-bit + sign

DIGITAL INPUT (HEX)	DIGITAL INPUT LD7……LD0 (BINARY)	LINEARIZATION ADJUST
FF	1111 1111	−0. 164703125 V_{FB}
E0	1110 0000	−0.1245 V_{FB}
C0	1100 0000	−0.083 V_{FB}
A0	1010 0000	−0.0415 V_{FB}
81	1000 0001	−0.001296875 V_{FB}
00	0000 0000	0 V_{FB}
01	0000 0001	+0.001296875 V_{FB}
20	0010 0000	+0.0415 V_{FB}
40	0100 0000	+0.083 V_{FB}
60	0110 0000	+0.1245 V_{FB}
7F	0111 1111	+0.164703125 V_{FB}

Table 37. Linearization DAC—Data Format Example (Range 1: $-0.166V_{FB}$ < Linearization DAC Range < $+0.166V_{FB}$)

Linearization DAC Equation:

Decimal # counts = |Desired K_{LIN}| / (Full-Scale Ratio/128)

Linearization DAC Example:

Given: (Range 1: $-0.166V_{FB}$ < Linearization DAC Range < $+0.166V_{FB}$)
Want: K_{LIN} Ratio = −0.082
Decimal # counts = 0.082 / (0.166/128) = 63.228
Use 63 counts → 0x3F → 0011 1111
However, we want −0.082, so we add a '1' in the sign bit (MSB, bit 7) for negative ratio:
Final Linearization DAC setting: 1011 1111 → 0xBF

Register 4: PGA Coarse Offset Adjust and Gain Select/Output Amplifier Gain Select Register (Read/Write, Address Pointer = 00100)

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	0WD	GO2	GO1	GO0	GI3	GI2	GI1	GI0	RFB	RFB	RFB	OS4	OS3	OS2	OS1	OS0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Descriptions:

OWD: One-Wire Disable (only valid while V_{OUT} is enabled, for use when PRG is connected to V_{OUT})
1 = Disable
0 = Enable

GO[2:0]: Output Amplifier Gain Select, 1-of-7 plus internal feedback disable

GI[3:0]: Front-End PGA Gain Select, 1-of-8, and Input Mux Control
GI3 = Input Mux Control
GI[2:0] = Gain Select

RFB: Reserved Factory Bit: Set to zero for proper operation

OS[4:0]: Coarse Offset Adjust on Front-End PGA, 4-bit + sign
1LSB = V_{REF}/1250

GO2 [14]	GO1 [13]	GO0 [12]	OUTPUT AMPLIFIER GAIN
0	0	0	2
0	0	1	2.4
0	1	0	3
0	1	1	3.6
1	0	0	4.5
1	0	1	6
1	1	0	9
1	1	1	Disable Internal Feedback

Table 38. Output Amplifier—Gain Select

GI3 MUX CNTL [11]	GI2 GAIN SEL2 [10]	GI1 GAIN SEL1 [9]	GI0 GAIN SEL0 [8]	INPUT MUX STATE(1)	FRONT-END PGA GAIN
0	0	0	0	$V_{IN1} = V_{INP}$, $V_{IN2} = V_{INN}$	4
0	0	0	1	$V_{IN1} = V_{INP}$, $V_{IN2} = V_{INN}$	8
0	0	1	0	$V_{IN1} = V_{INP}$, $V_{IN2} = V_{INN}$	16
0	0	1	1	$V_{IN1} = V_{INP}$, $V_{IN2} = V_{INN}$	23.27
0	1	0	0	$V_{IN1} = V_{INP}$, $V_{IN2} = V_{INN}$	32
0	1	0	1	$V_{IN1} = V_{INP}$, $V_{IN2} = V_{INN}$	42.67
0	1	1	0	$V_{IN1} = V_{INP}$, $V_{IN2} = V_{INN}$	64
0	1	1	1	$V_{IN1} = V_{INP}$, $V_{IN2} = V_{INN}$	128
1	0	0	0	$V_{IN1} = V_{INN}$, $V_{IN2} = V_{INP}$	−4
1	0	0	1	$V_{IN1} = V_{INN}$, $V_{IN2} = V_{INP}$	−8
1	0	1	0	$V_{IN1} = V_{INN}$, $V_{IN2} = V_{INP}$	−16
1	0	1	1	$V_{IN1} = V_{INN}$, $V_{IN2} = V_{INP}$	−23.27
1	1	0	0	$V_{IN1} = V_{INN}$, $V_{IN2} = V_{INP}$	−32
1	1	0	1	$V_{IN1} = V_{INN}$, $V_{IN2} = V_{INP}$	−42.67
1	1	1	0	$V_{IN1} = V_{INN}$, $V_{IN2} = V_{INP}$	−64
1	1	1	1	$V_{IN1} = V_{INN}$, $V_{IN2} = V_{INP}$	−128

(1) V_{IN1} = Pin 4, V_{IN2} = Pin 5, V_{INP} = positive input to front-end PGA, V_{INN} = negative input to front-end PGA; ee detailed block diagram (Figure 75).

Table 39. Front End PGA—Gain Select

OS4 [4]	OS3 [3]	OS2 [2]	OS1 [1]	OS0 [0]	COARSE OFFSET (mV)	COARSE OFFSET
1	1	1	1	1	−58.3333	$-14(V_{REF}/1200)$
1	1	1	1	0	−54.1666	$-13\ (V_{REF}/1200)$
1	1	1	0	1	−50	$-12\ (V_{REF}/1200)$
1	1	1	0	0	−45.8333	$-11\ (V_{REF}/1200)$
1	1	0	1	1	−41.6666	$-10\ (V_{REF}/1200)$
1	1	0	1	0	−37.5	$-9\ (V_{REF}/1200)$
1	1	0	0	1	−33.3333	$-8(V_{REF}/1200)$
1	1	0	0	0	−29.1666	$-7\ (V_{REF}/1200)$
1	0	1	1	1	−29.1666	$-7\ (V_{REF}/1200)$
1	0	1	1	0	−25.0	$-6\ (V_{REF}/1200)$
1	0	1	0	1	−20.8333	$-5\ (V_{REF}/1200)$
1	0	1	0	0	−16.6666	$-4\ (V_{REF}/1200)$
1	0	1	0	1	−12.5	$-3\ (V_{REF}/1200)$
1	0	0	1	0	−8.3333	$-2\ (V_{REF}/1200)$
1	0	0	0	1	−4.1666	$-1\ (V_{REF}/1200)$
0	0	0	0	0	0	$0V_{REF}$
0	0	0	0	1	+4.166	$+1\ (V_{REF}/1200)$
0	0	0	1	0	+8.3333	$+2\ (V_{REF}/1200)$
0	0	0	1	1	+12.5	$+3\ (V_{REF}/1200)$
0	0	1	0	0	+16.6666	$+4\ (V_{REF}/1200)$
0	0	1	0	1	+20.8333	$+5\ (V_{REF}/1200)$
0	0	1	1	0	+25.0	$+6\ (V_{REF}/1200)$
0	0	1	1	1	+29.1666	$+7\ (V_{REF}/1200)$
0	1	0	0	0	+29.1666	$+7\ (V_{REF}/1200)$
0	1	0	0	1	+33.3333	$+8\ (V_{REF}/1200)$
0	1	0	1	0	+37.5	$+9\ (V_{REF}/1200)$
0	1	0	1	1	+41.6666	$+10\ (V_{REF}/1200)$
0	1	1	0	0	+45.8333	$+11\ (V_{REF}/1200)$
0	1	1	0	1	+50	$+12\ (V_{REF}/1200)$
0	1	1	1	0	+54.1666	$+13\ (V_{REF}/1200)$
0	1	1	1	1	+58.3333	$+14\ (V_{REF}/1200)$

Table 40. Coarse Offset Adjust on Front-End PGA—Data Format Example (V_{REF} = +5V)

Register 5: PGA Configuration and Over/Under-Scale Limit Register (Read/Write, Address Pointer = 00101)

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	RFB	RFB	CLK_ CFG1	CLK_ CFG0	EXT EN	INT EN	EXT POL	INT POL	RFB	OU EN	HL2	HL1	HL0	LL2	LL1	LL0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Descriptions:

RFB: (Reserved Factory Bit): Set to zero for proper operation

CLK_CFG[1:0]: Clocking scheme for front-end PGA auto-zero and Coarse Offset DAC Chopping

EXTEN: Enable External Fault Comparator Group (INP_HI, INP_LO, INN_LO, INN_HI)
1 = Enable External Fault Comparator Group
0 = Disable External Fault Comparator Group

INTEN: Enable Internal Fault Comparator Group (A2SAT_LO, A2SAT_HI, A1SAT_LO, A1SAT_HI, A3_VCM)
1 = Enable Internal Fault Comparator Group
0 = Disable Internal Fault Comparator Group

EXTPOL: Selects V_{OUT} output polarity when External Fault Comparator Group detects a fault, if EXTEN=1
1 = Force V_{OUT} high when any comparator in the External Fault Comparator Group detects a fault
0 = Force V_{OUT} low when any comparator in the External Fault Comparator Group detects a fault

INTPOL: Selects V_{OUT} output polarity when Internal Fault Comparator Group detects a fault, if INTEN=1
1 = Force V_{OUT} high when any comparator in the Internal Fault Comparator Group detects a fault
0 = Force V_{OUT} low when any comparator in the Internal Fault Comparator Group detects a fault

OUEN: Over/Under−Scale Limit Enable.
1 = Enable Over/Under-Scale limits
0 = Disable Over/Under-Scale limits

HL[2:0]: Over-Scale Threshold Select

LL[2:0]: Under-Scale Threshold Select

CLK_CFG1 [13]	CLK_CFG0 [12]	PGA FRONT END AUTO-ZERO	COARSE ADJUST DAC CHOPPING
0	0	7kHz typical	3.5kHz typical
0	1	7kHz typical	Off (none)
1	0	7kHz typical, Random Clocking	3.5kHz typical, Random Clocking
1	1	7kHz typical	3.5kHz typical, Random Clocking

Table 41. Clock Configuration (Front End PGA Auto-Zero and Coarse Adjust DAC Chopping)

HL2 [5]	HL1 [4]	HL0 [3]	OVER-SCALE THRESHOLD (V)	OVER-SCALE THRESHOLD
0	0	0	4.854	0.9708 V_{REF}
0	0	1	4.805	0.9610 V_{REF}
0	1	0	4.698	0.9394 V_{REF}
0	1	1	4.580	0.9160 V_{REF}
1	0	0	4.551	0.9102 V_{REF}
1	0	1	3.662	0.7324 V_{REF}
1	1	0	2.764	0.5528 V_{REF}
1	1	1	Reserved	—

Table 42. Over-Scale Threshold Select (V_{REF} = +5V)

LL2 [2]	LL1 [1]	LL0 [0]	UNDER-SCALE THRESHOLD (V)	UNDER-SCALE THRESHOLD
0	0	0	0.127	0.02540 V_{REF}
0	0	1	0.147	0.02930 V_{REF}
0	1	0	0.176	0.03516 V_{REF}
0	1	1	0.196	0.03906 V_{REF}
1	0	0	0.225	0.04492 V_{REF}
1	0	1	0.254	0.05078 V_{REF}
1	1	0	0.274	0.05468 V_{REF}
1	1	1	0.303	0.06054 V_{REF}

Table 43. Under-Scale Threshold Select (V_{REF} = +5V)

Register 6: Temp ADC Control Register (Read/Write, Address Pointer = 00110)

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	RFB	RFB	ADC 2x	ADCS	ISEN	CEN	TEN	AREN	RV1	RV0	M1	M0	G1	G0	R1	R0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Descriptions:

RFB: **Reserved Factory Bit: Set to zero for proper operation**

ADC2X: **Temp ADC runs 2X faster (not for internal Temp Sense Mode)**
0 = 1X conversion speed (6ms typical, R1, R0 = ‘00’, TEN = ‘0’, AREN = ‘0’)
1 = 2X conversion speed (3ms typical, R1, R0 = ‘00’, TEN = ‘0’, AREN = ‘0’)

ADCS: **Start (restart) the Temp ADC (single conversion control if CEN = 0)**
0 = No Start/Restart Temp ADC
1 = Start/Restart Temp ADC (each write of a ‘1’ causes single conversion; when conversion is completed ADCS = ‘0’)

ISEN: **$TEMP_{IN}$ Current source (I_{TEMP}) Enable**
1 = Enable 7µA current source, I_{TEMP}
0 = Disable 7µA current source, I_{TEMP}

CEN: **Enable Temp ADC Continuous Conversion Mode**
1 = Continuous Conversion mode
0 = Noncontinuous Conversion mode

TEN: **Internal Temperature Mode Enable**
1 = Internal Temperature Sensor Mode Enabled
0 = External Signal Mode

For TEN = 1, set the following bits as shown:
ADC2X = 0
ADCS = set as desired
CEN = set as desired
AREN = 0
RV[1:0] = 00
M[1:0] = 00
G[1:0] = 00
R[1:0] = Set for desired Temp ADC resolution.

AREN: **Temp ADC internal reference enable**
1 = Enable Temp ADC internal reference (internal reference is 2.048V typical)
0 = Disable Temp ADC internal reference (use external ADC reference; see RV[1:0])

RV[1:0]: **Temp ADC External Reference Select (V_{SA}, V_{EXC}, V_{REF})**

M[1:0]: **Temp ADC Input Mux Select**

G[1:0]: Temp ADC PGA Gain Select (X1, X2, X4, X8)

R[1:0]: Temp ADC Resolution (Conversion time) Select

AREN [8]	RV1 [7]	RV [6]	TEMP ADC REFERENCE (V_{REFT})
0	0	0	V_{REF}
0	0	1	V_{EXC}
0	1	0	V_{SA}
0	1	1	Factory Reserved
1	X	X	Temp ADC Internal REF (2.048V)
NOTE: X = don't care			

Table 44. Temp ADC Reference Select

M1 [5]	M0 [4]	TEMP ADC PGA +INPUT	TEMP ADC PGA −INPUT
0	0	$TEMP_{IN}$	GND_A
0	1	V_{EXC}	$TEMP_{IN}$
1	0	V_{OUT}	GND_A
1	1	V_{REF}	$TEMP_{IN}$

Table 45. Temp ADC Input Mux Select

G1 [3]	G0 [2]	TEMP ADC PGA GAIN
0	0	X1
0	1	X2
1	0	X4
1	1	X8

Table 46. Temp ADC PGA Gain Select

Internal Temperature Mode (Register 6 [9] = '1')

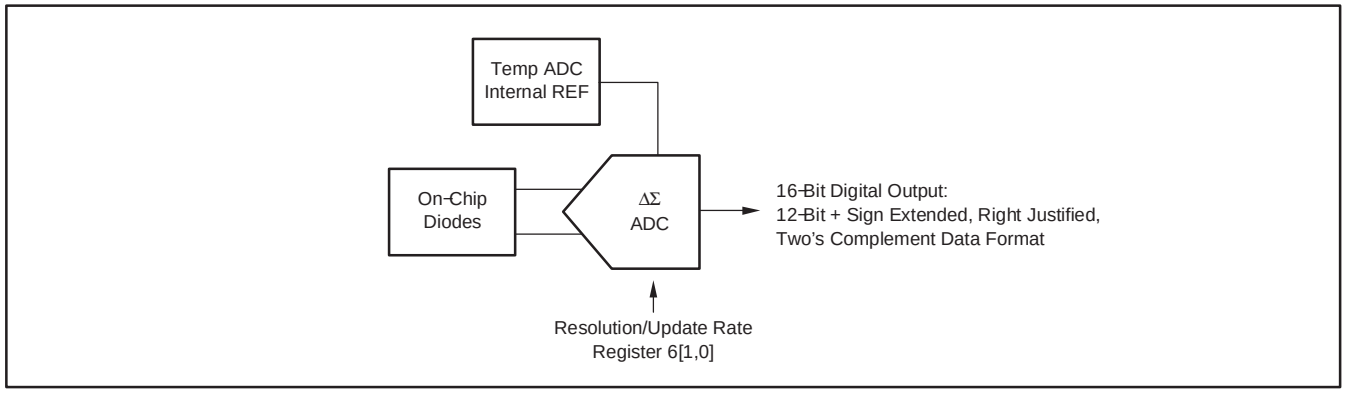


Figure 72.

External Signal Mode (Register 6 [9], TEN = '0')

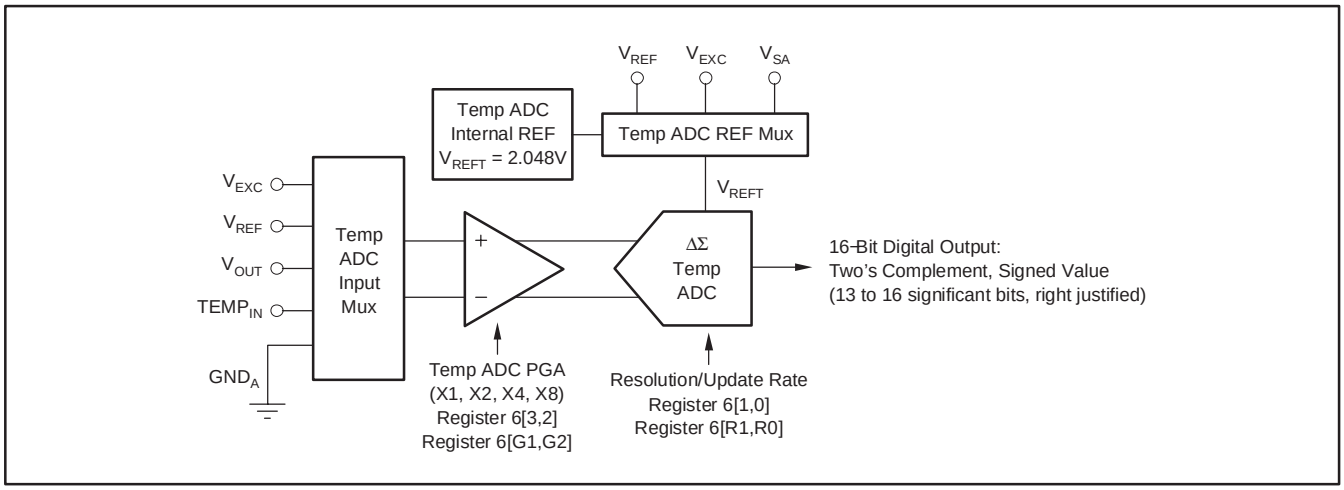


Figure 73.

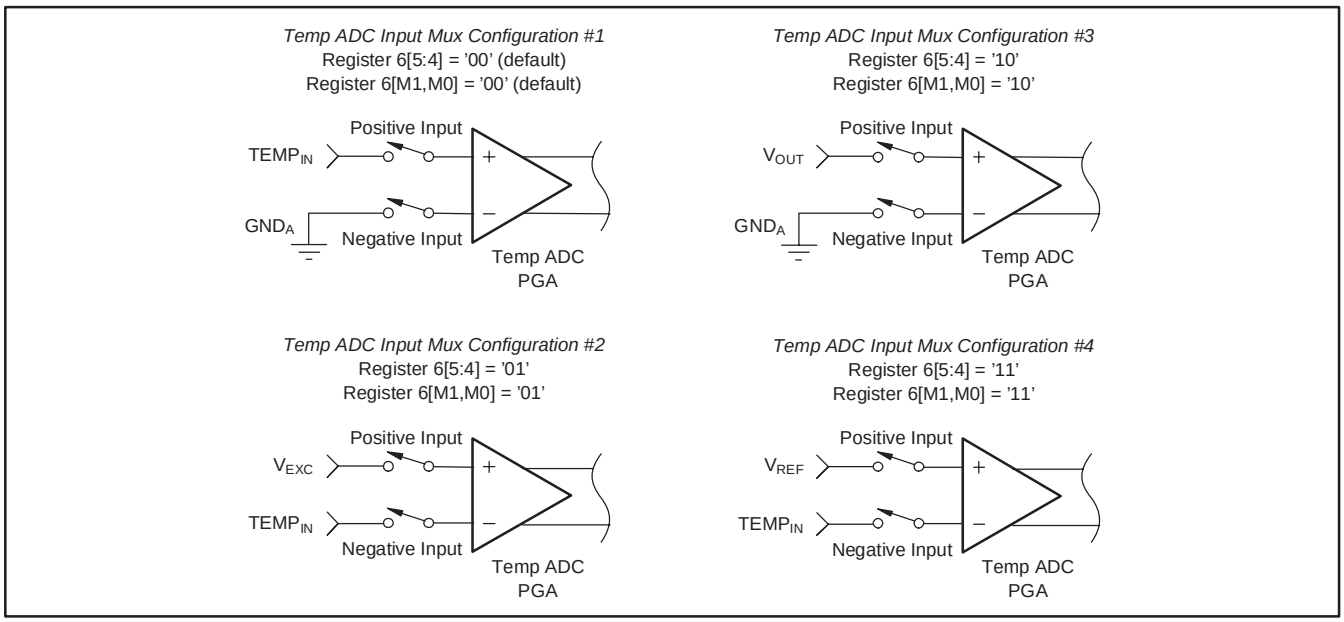


Figure 74.

R1 [1]	R0 [0]	INTERNAL TEMPERATURE MODE [TEN = 1]	EXTERNAL SIGNAL MODE [TEN = 0|, EXTERNAL REFERENCE [AREN = 0]	EXTERNAL SIGNAL MODE [TEN = 0|, INTERNAL REFERENCE [2.048V, AREN = 1]
0	0	9-Bit + Sign, 0.5°C, (3ms)	11-Bit + Sign (6ms)	11-Bit + Sign (8 ms)
0	1	10-Bit + Sign, 0.25°C, (6ms)	13-Bit + Sign (24ms)	13-Bit + Sign (32ms)
1	0	11-Bit + Sign, 0.125°C, (12ms)	14-Bit + Sign (50 ms)	14-Bit + Sign (64 ms)
1	1	12-Bit + Sign, 0.0625°C, (24ms)	15-Bit + Sign (100 ms)	15-Bit + Sign (128 ms)

Table 47. Temp ADC—Resolution (Conversion Tme) Select

Register 7: Output Enable Counter Control Register (Read/Write, Address Pointer = 00111)

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	RFB	RFB	RFB	RFB	DLY3	DLY2	DLY1	DLY0	OEN7	OEN6	OEN5	OEN4	OEN3	OEN2	OEN1	OEN0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Descriptions:

RFB: Reserved Factory Bit: Set to zero for proper operation

DLY[3:0]: Temp ADC Delay

Temp ADC begins conversion after DLY[3:0] x 10ms after valid WRITE to this register. Initial count, DLY[3:0] is decremented every 10ms to zero count and then Temp ADC is enabled. This allows for linearization and excitation analog circuitry to settle before applying temperature compensation.

OEN[7:0]: Output Enable Counter for One-Wire Interface/V_{OUT} Multiplexed mode.

V_{OUT} is enabled after a valid WRITE to this register. Any non-zero value = V_{OUT} Enable initial count, decremented every 10ms to zero count, and then V_{OUT} is disabled. After V_{OUT} is disabled, a one-second internal timer is set. If serial communication takes place from an outside controller on either the One-Wire interface (PRG pin) or Two-Wire interface, then V_{OUT} will remain disabled as long as the PGA309 is addressed at least once per second.

DLY3 [11]	DLY2 [10]	DLY1 [9]	DLY0 [8]	DECIMAL EQUIVALENT (INITIAL COUNTER VALUE)	TEMP ADC DELAY(1) (ms)
0	0	0	0	0	0
0	0	0	1	1	10
0	0	1	0	2	20
0	0	1	1	3	30
0	1	0	0	4	40
0	1	0	1	5	50
0	1	1	0	6	60
0	1	1	1	7	70
1	0	0	0	8	80
1	0	0	1	9	90
1	0	1	0	10	100
1	0	1	1	11	110
1	1	0	0	12	120
1	1	0	1	13	130
1	1	1	0	14	140
1	1	1	1	15	150

(1) Temp ADC Delay = Initial Counter Value x 10ms

Table 48. Temp ADC—Delay After V_{OUT} Enable

DIGITAL INPUT OEN7……OEN0 [7……0] (BINARY)	DECIMAL EQUIVALENT (INITIAL COUNTER VALUE)	V_{OUT} ENABLE TIMEOUT(1) (ms)
0000 0000	0	0 (V_{OUT} disabled)
0010 0000	32	320
0100 0000	64	640
0110 0000	96	960
1000 0000	128	1280
1010 0000	160	1600
1100 0000	192	1920
1110 0000	224	2240
1111 1111	255	2550

(2) V_{OUT} Enable Timeout = Initial Counter Value x 10ms

Table 49. Output Enable Counter for One-Wire Interface/V_{OUT} Multiplexed Mode

Register 8: Alarm Status Register (Read Only, Address Pointer = 01000)

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	X	X	X	X	X	X	X	ALM8	ALM7	ALM6	ALM5	ALM4	ALM3	ALM2	ALM1	ALM0
POR VALUE	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X	X

Bit Descriptions:

ALM[8:0]: Fault Monitor Comparator Outputs (1 = Fault Condition)

See Fault Monitor Circuit Section.

ALM8 — A1SAT_HI
ALM7 — A1SAT_LO
ALM6 — A2SAT_HI
ALM5 — A2SAT_LO
ALM4 — A3_VCM
ALM3 — INN_HI
ALM2 — INN_LO
ALM1 — INP_HI
ALM0 — INP_LO

PGA309 EXTERNAL EEPROM—REGISTER CONFIGURATION DATA

Checksum1 = 0xFFFF − Sum(Addr0 to Addr12); 16-bit wide, carry over bits are ignored.

EXTERNAL EEPROM ADDRESS (DECIMAL)	PGA309 INTERNAL REGISTER ADDRESS	PGA309 INTERNAL REGISTER DESCRIPTION	DATA (LSBs) (MSBs)	D7 D15	D6 D14	D5 D13	D4 D12	D3 D11	D2 D10	D1 D9	D0 D8
0			Programmed Flag Value (LSBs)(1)	0	1	0	0	1	0	0	1
1			Programmed Flag Value (LSBs)(1)	0	1	0	1	0	1	0	0
2			Unused(1)								
3			Unused(1)								
4			Unused(1)								
5			Unused(1)								
6	00011 (LSBs)	Register 3− Reference Control and Linearization		LD7	LD6	LD5	LD4	LD3	LD2	LD1	LD0
7	00011 (MSBs)	Register 3− Reference Control and Linearization		0	TM1	BG	SD	EXS	EXEN	RS	REN
8	00100 (LSBs)	Register 4− PGA Coarse Offset and Gain/Output Amp Gain		0	CFG6	CFG2	OS4	OS3	OS2	OS1	OS0
9	00100 (MSBs)	Register 4− PGA Coarse Offset and Gain/Output Amp Gain		OWD	GO2	GO1	GO0	GI3	GI2	GI1	GI0
10	00101 (LSBs)	Register 5− PGA Configuration and Over/Under-Scale Limit		0	OUEN	HL2	HL1	HL0	LL2	LL1	LL0
11	00101 (MSBs)	Register 5− PGA Configuration and Over/Under-Scale Limit		0	0	0	0	EXTEN	INTEN	EXTPOL	INTPOL
12	00110 (LSBs)	Register 6− Temp ADC Control		RV1	RV0	M1	M0	G1	G0	R1	R0
13	00110 (MSBs)	Register 6− Temp ADC Control		0	0	ADC2X	ADCS	ISEN	CEN	TEN	AREN
14			Checksum [LSBs]	1CS7	1CS6	1CS5	1CS4	1CS3	1CS2	1CS1	1CS0
15			Checksum [MSBs]	1CS15	1CS14	1CS13	1CS12	1CS11	1CS10	1CS9	1CS8
16			Temperature Index Value T0 (LSBs)	T0−D7	T0−D6	T0−D5	T0−D4	T0−D3	T0−D2	T0−D1	T0−D0
17			Temperature Index Value T0 (MSBs)	T0−D15	T0−D14	T0−D13	T0−D12	T0−D11	T0−D10	T0−D9	T0−D8
18			Zero Adjustment DAC Value for T0 and below (LSBs)	Z0−D7	Z0−D6	Z0−D5	Z0−D4	Z0−D3	Z0−D2	Z0−D1	Z0−D0
19			Zero Adjustment DAC Value for T0 and below (MSBs)	Z0−D15	Z0−D14	Z0−D13	Z0−D12	Z0−D11	Z0−D10	Z0−D9	Z0−D8
20			Gain Adjustment DAC Value for T0 and below (LSBs)	G0−D7	G0−D6	G0−D5	G0−D4	G0−D3	G0−D2	G0−D1	G0−D0
21			Gain Adjustment DAC Value for T0 and below (MSBs)	G0−D15	G0−D14	G0−D13	G0−D12	G0−D11	G0−D10	G0−D9	G0−D8

(1) While these values are not used to configure the PGA309, they are included in Checksum calculations.

Table 50. PGA309 External EEPROM—Register Configuration Data Checksum1

PGA309 EXTERNAL EEPROM—REGISTER CONFIGURATION DATA

Checksum2 = 0xFFFF − Sum(Addr16 to AddrZME); 16-bit wide, carry over bits are ignored.

EXTERNAL EEPROM ADDRESS (DECIMAL)	PGA309 INTERNAL REGISTER ADDRESS	PGA309 INTERNAL REGISTER DESCRIPTION	DATA (LSBs) (MSBs)	D7 D15	D6 D14	D5 D13	D4 D12	D3 D11	D2 D10	D1 D9	D0 D8
112			Temperature Index Value T16 (LSBs)	T16−D7	T16−D6	T16−D5	T16−D4	T16−D3	T16−D2	T16−D1	T16−D0
113			Temperature Index Value T16 (MSBs)	T16−D15	T16−D14	T16−D13	T16−D12	T16−D11	T16D10	T16−D9	T16−D8
114			Zero Adjustment DAC Scale Factor for T16 and below (LSBs)	ZM−D7	ZM−D6	ZM−D5	ZM−D4	ZM−D3	ZM−D2	ZM−D1	ZM−D0
115			Zero Adjustment DAC Scale Factor for T16 and below (MSBs)	ZM−D15	ZM−D14	ZM−D13	ZM−D12	ZM−D11	ZM−D10	ZM−D9	ZM−D8
116			Gain Adjustment DAC Scale Factor for T16 and below (LSBs)	GM−D7	GM−D6	GM−D5	GM−D4	GM−D3	GM−D2	GM−D1	GM−D0
117			Gain Adjustment DAC Scale Factor for T16 and below (LSBs)	GM−D15	GM−D14	GM−D13	GM−D12	GM−D11	GM−D10	GM−D9	GM−D8
118			T_{END} (End of Look-up Table) LSBs(1)	1	1	1	1	1	1	1	1
119			T_{END} (End of Look-up Table) MSBs(1)	0	1	1	1	1	1	1	1
120			ZME (End of Look-up Table) LSBs(1)	0	0	0	0	0	0	0	0
121			ZME (End of Look-up Table) MSBs(1)	0	0	0	0	0	0	0	0
122			GME (End of Look-up Table)−Checksum2 LSBs	GME-D7	GME-D6	GME-D5	GME-D4	GME-D3	GME-D2	GME-D1	GME-D0
123			GME (End of Look-up Table)−Checksum2 MSBs	GME-D15	GME-D14	GME-D13	GME-D12	GME-D11	GME-D10	GME-D9	GME-D8

(1) While these values are not used to configure the PGA309, they are included in Checksum calculations.

Table 51. PGA309 External EEPROM—Register Configuration Data Checksum2

DETAILED BLOCK DIAGRAM

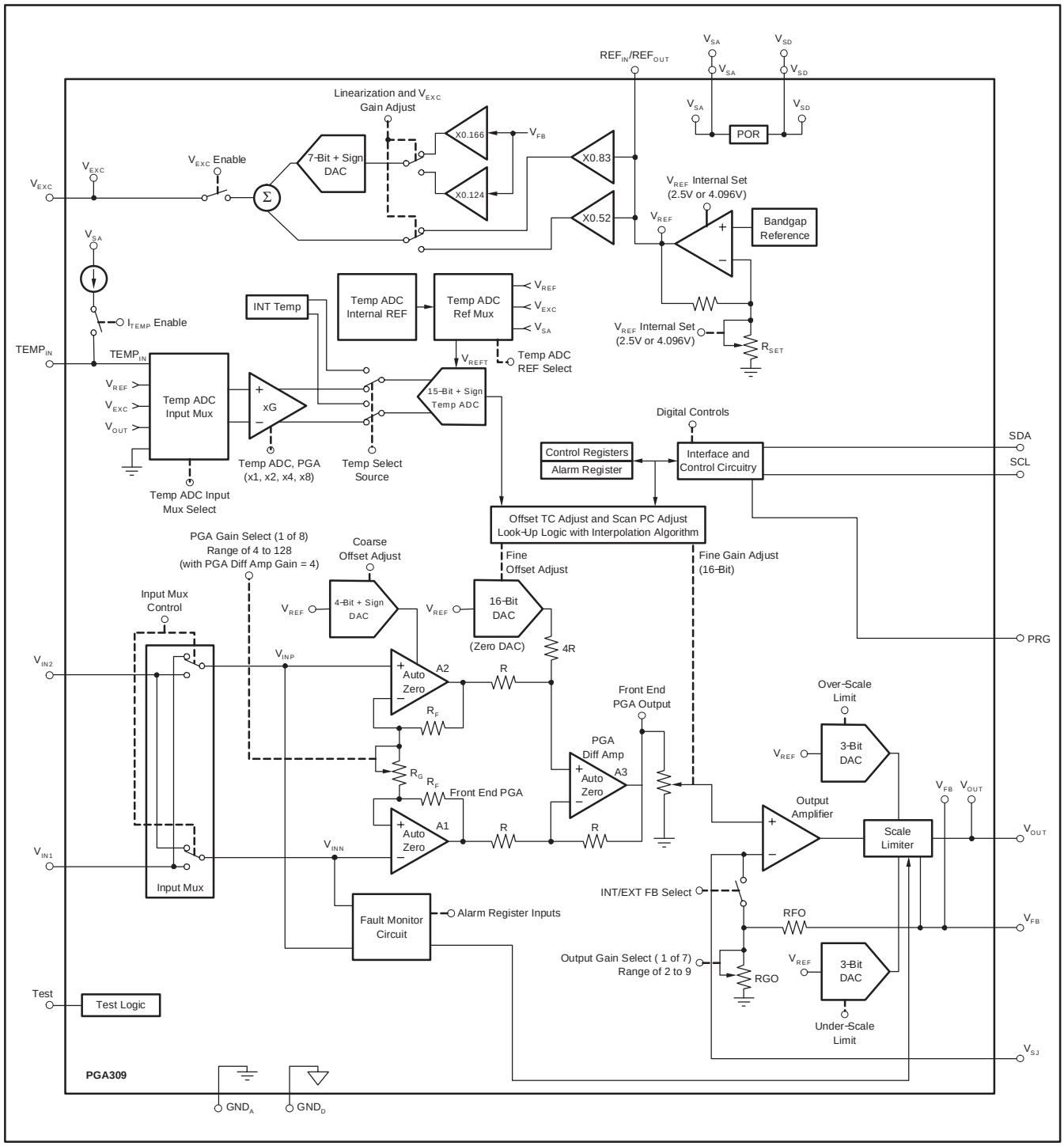
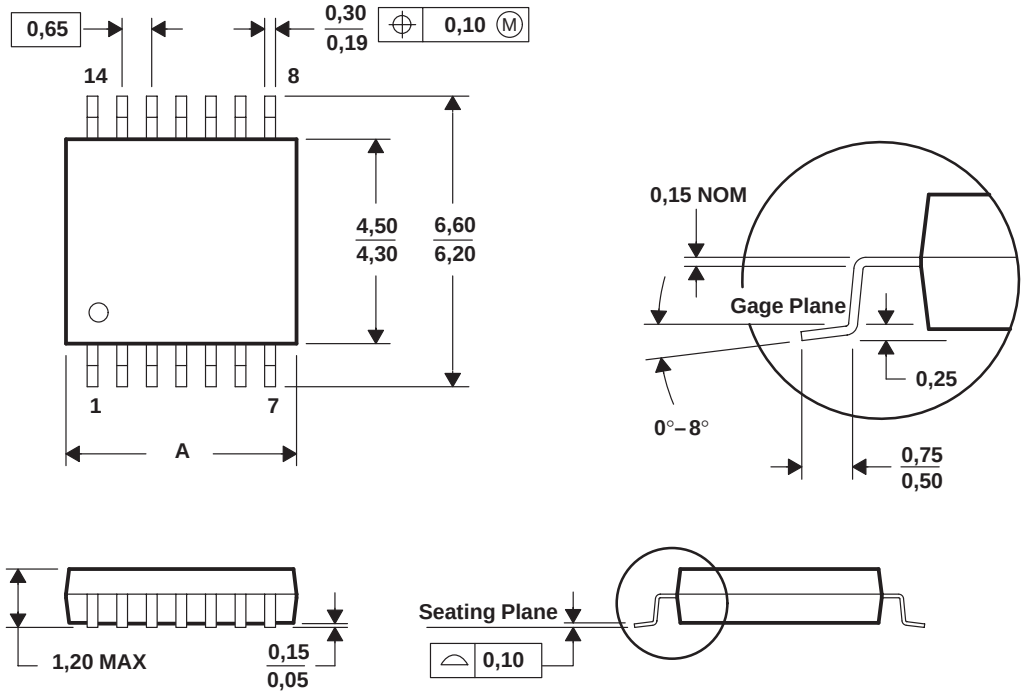


Figure 75. Detailed Block Diagram

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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Mailing Address: Texas Instruments
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