ZARLINK SEMICONDUCTOR

MT352
COFDM Demodulator
Data Sheet

July 2004

Features

- Nordig II and ETSI 300 744 compliant
- Superior Single Frequency Network performance
- Unique active Impulse-Noise filtering
- Single SAW operation
- Automatic co-channel and adjacent-channel interference suppression
- Clock generation from single low-cost 20.48 MHz crystal or external 4 or 27 MHz clock
- IF sampling at 4.57, 36.17 or 43.5 MHz from a single crystal frequency
- Channel bandwidth of 6, 7 & 8 MHz
- Blind acquisition capability (including 2 K / 8 K mode detect)
- Automatic spectral inversion detection
- Fast auto-scan and acquisition technology
- Very low software overhead
- Dual AGC control option
- Access to channel SNR, pre- and post-Viterbi bit error rates
- Compact 64 pin LQFP
- Less than 0.22 W power consumption
- Standby and sleep options

Applications

- Set-top boxes
- Integrated digital televisions
- Personal video recorders
- Terrestrial PC reception
- Mobile and portable applications

Ordering Information

MT352/CG/GP1N	64 PIN LQFP
MT352/CG/GP1Q	64 Pin LQFP
MT352/CG/GP2Q	64 Pin LQFP*

* Pb free

0°C to +70°C

Zarlink evaluation kits include application board, TNIM and supporting software based on industry standard operating systems. Device drivers are also available enabling rapid product development and reduction in time to market.

Description

MT352 is a superior third generation Coded Orthogonal Frequency Division Multiplex (COFDM) television demodulator that is both Nordig II and DVB (as defined in ETS 300 744 specification) compliant. It can be used in either 2 K or 8 K modes with 6, 7 or 8 MHz channels and is capable of addressing all modes of transmission.

The device includes a high performance 10-bit A/D converter capable of accepting direct IF at 36.17 or 43.75 MHz. Sampling rates required for both these frequencies in 6,7 or 8 MHz OFDM channels can be generated from a single 20.48 MHz crystal. Alternatively, there is provision to replace this crystal with a 4 or 27 MHz external clock input.

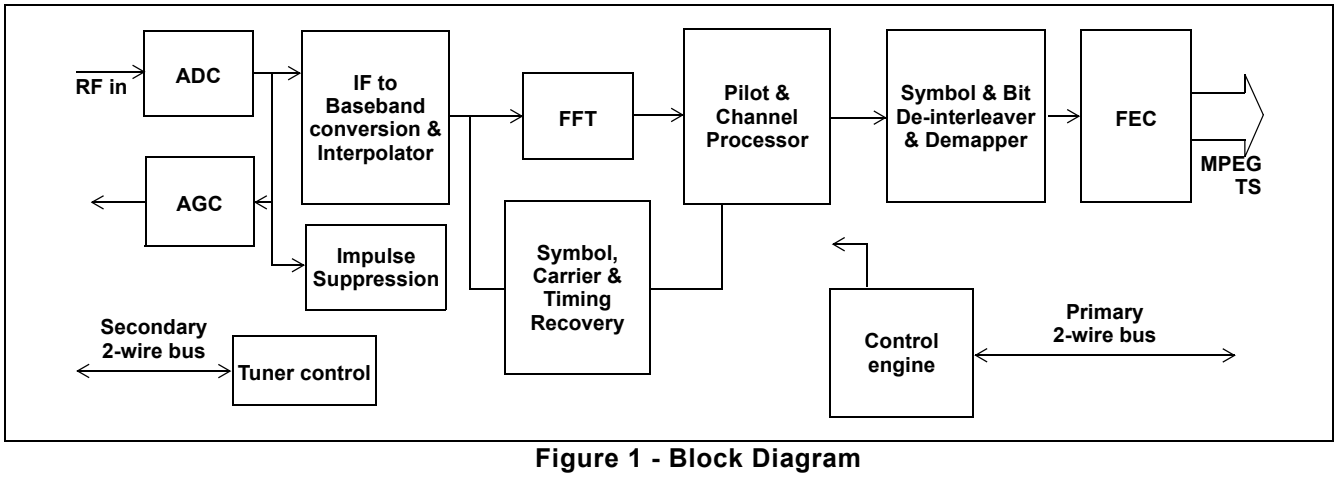

Figure 1 - Block Diagram

Unique algorithms that actively filter out impulse noise, without affecting normal performance, have been implemented. This reduces the interference effect from vehicles and electrical appliances, which is known to have significant detrimental effect on the quality of digital TV reception.

Programming is simplified utilising a high level command driven interface. A sophisticated engine controls all acquisition and tracking operations as well as controlling the tuner via a 2-wire bus. Any frequency range can be automatically scanned for digital TV channels. This mechanism ensures minimal interaction, maximum flexibility, fastest acquisition and the fastest auto scan capability of any chip in the market.

Blind acquisition mode enables automatic detection of all OFDM signal parameters, including mode, guard and spectral inversion. The frequency capture range is sufficient to compensate for the combined offset introduced by the tuner and broadcaster.

The device is packaged in a 64-pin LQFP and consumes less than 220 mW of power.

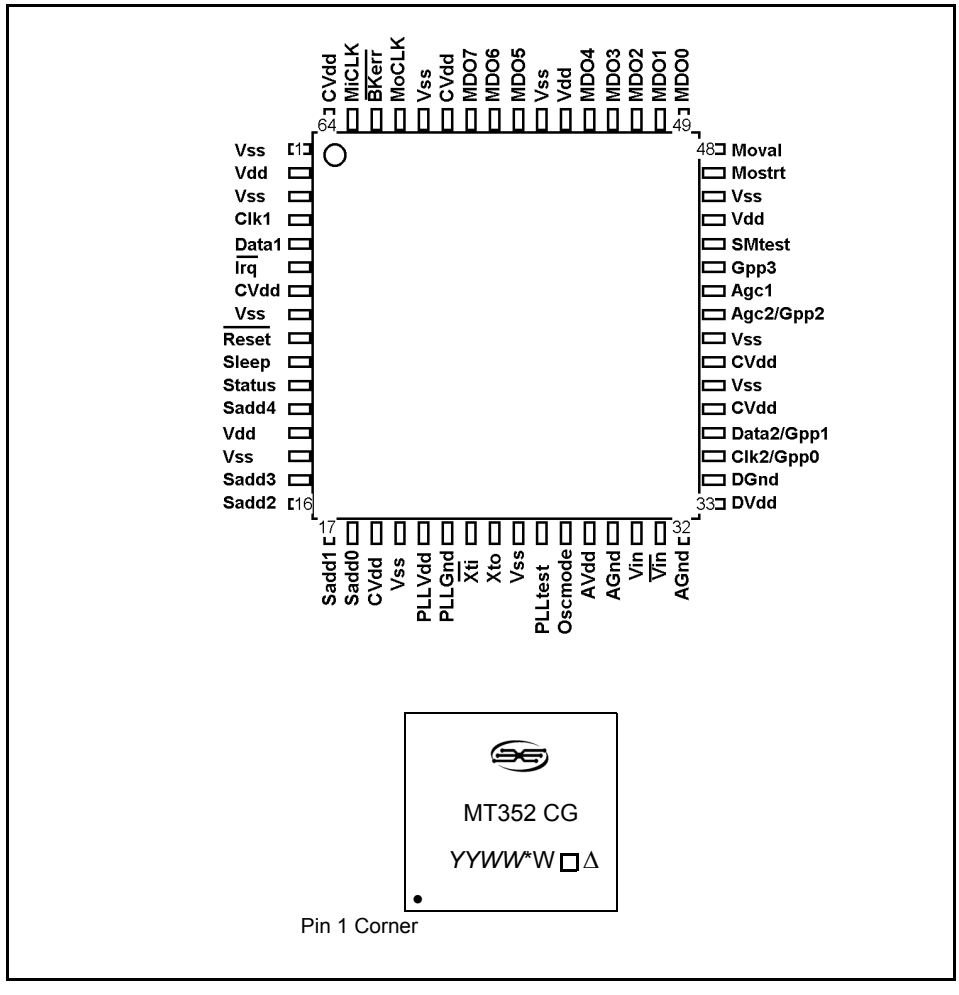

Figure 2 - Package Outline

Pin Description

Pin Description Table

Pin No	Name	Pin Description	I/O	Type	V	mA
MPEG pins						
47	MOSTRT	MPEG packet start	O	CMOS Tristate	3·3	1
48	MOVAL	MPEG data valid	O		3·3	1
49-53, 56-58	MDO(0:7)	MPEG data bus	O		3·3	1
61	MOCLK	MPEG clock out	O		3·3	1
62	$\overline{\text{BKERR}}$	Block error	O		3·3	1
63	MICLK	MPEG clock in	I	CMOS	3·3	
11	STATUS	Status output	O		3·3	1
6	$\overline{\text{IRQ}}$	Interrupt output	O	Open drain	5	6
Control pins						
4	CLK1	Serial clock	I	CMOS	5	
5	DATA1	Serial data	I/O	Open drain	5	6
23	$\overline{\text{XTI}}$	Low phase noise oscillator	I	CMOS		
24	XTO		O			
10	SLEEP	Device power down	I		3·3	
12, 15-18	SADD(4:0)	Serial address set	I		3·3	
44	SMTEST	Scan mode enable	I		3·3	
35	CLK2/GPP0	Serial clock tuner	I/O	Open drain	5	6
36	DATA2/GPP 1	Serial data tuner	I/O		5	6
42	AGC1	Primary AGC	O		5	6
41	AGC2/GPP 2	Secondary AGC	I/O		5	6
43	GPP(3)	General purpose I/O	I/O		5	6
9	$\overline{\text{RESET}}$	Device reset	I	CMOS	5	
27	OSCMODE	Crystal oscillator mode	I	CMOS	3·3	
26	PLLTEST	PLL analogue test	O			
Analog inputs						
30	VIN	positive input	I			

Pin Description Table (continued)

Pin No	Name	Pin Description	I/O	Type	V	mA
31	$\overline{\text{VIN}}$	negative input	I			
Supply pins						
21	PLLVDD	PLL supply	S		1·8	
22	PLLGND		S		0	
7, 19, 37, 39, 59, 64	CVDD	Core logic power	S		1·8	
2, 13, 45, 54,	VDD	I/O ring power	S		3·3	
1, 3, 8, 14, 20, 25, 38, 40, 46, 55, 60	GND	Core and I/O ground	S		0	
28	AVDD	ADC analog supply	S		1·8	
29, 32	AGND		S		0	
33	DVDD	ADC digital supply	S		1·8	
34	DGND		S		0	

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1.0 Functional Description

A functional block diagram of the MT352 OFDM demodulator is shown in Figure 3. This accepts an IF analogue signal and delivers a stream of demodulated soft decision data to the on-chip Viterbi decoder. Clock, timing and frequency synchronisation operations are all digital and there are no analogue control loops except the AGC. The frequency capture range is large enough for all practical applications. This demodulator has novel algorithms to combat impulse noise as well as co-channel and adjacent channel interference. If the modulation is hierarchical, the OFDM outputs both high and low priority data streams. Only one of these streams is FEC-decoded, but the FEC can be switched from one stream to another with minimal interruption to the transport stream.

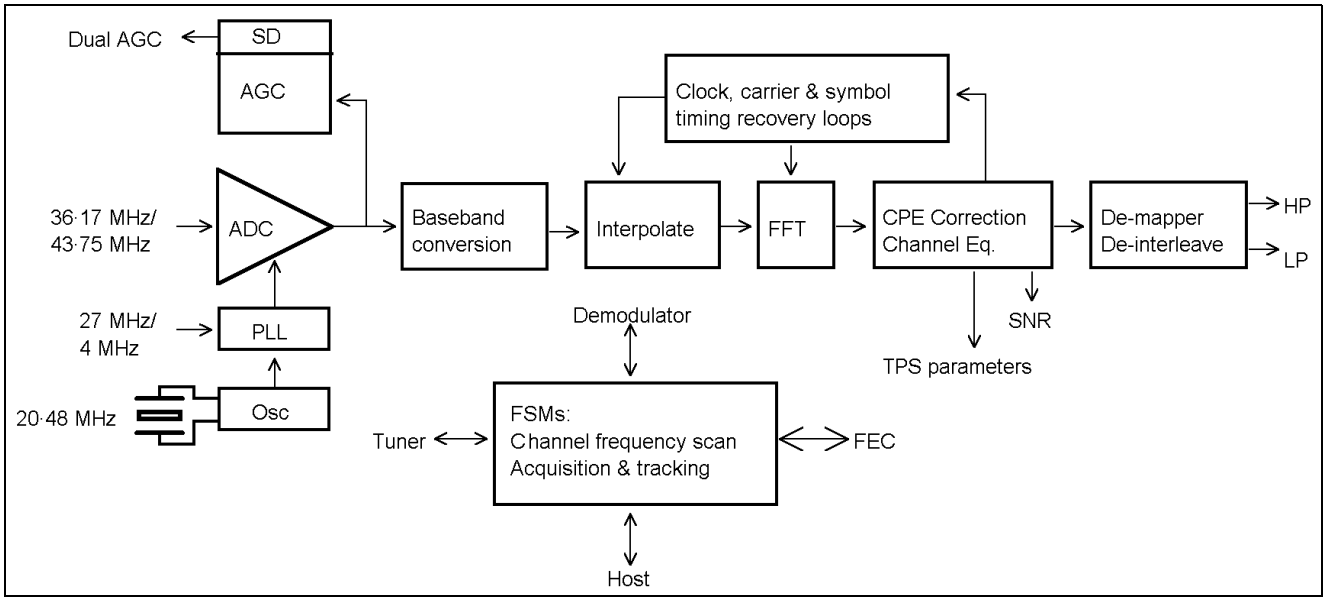


Figure 3 - OFDM Demodulator Diagram

The FEC module shown in Figure 4 consists of a concatenated convolutional (Viterbi) and Reed-Solomon decoder separated by a depth-12 convolutional de-interleaver. The Viterbi decoder operates on 5-bit soft decisions to provide the best performance over a wide range of channel conditions. The trace-back depth of 128 ensures minimum loss of performance due to inevitable survivor truncation, especially at high code rates. Both the Viterbi and Reed-Solomon decoders are equipped with bit-error monitors. The former provides the bit error rate (BER) at the OFDM output. The latter is the more useful measure as it gives the Viterbi output BER. The error collecting intervals of these are programmable over a very wide range.

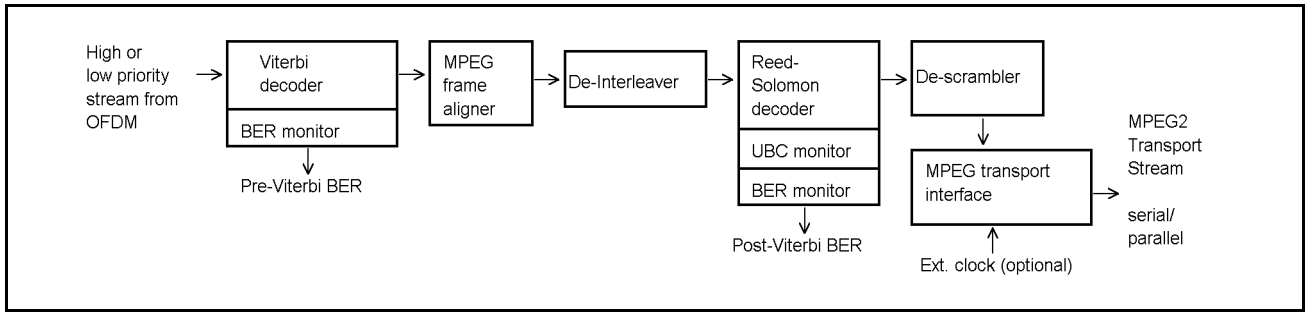


Figure 4 - FEC Block Diagram

The FSM controller shown in Figure 3 above controls both the demodulator and the FEC. It also drives the 2-wire bus to the tuner. The controller facilitates the automated search of all parameters or any sub-set of parameters of the received signal. It can also be used to scan any defined frequency range searching for OFDM channels. This

mechanism provides the fast channel scan and acquisition performance, whilst requiring minimal software overhead in the host driver.

The algorithms and architectures used in the MT352 have been heavily optimised to minimise hardware and chip area. This is proven by its 220 mW (typical) power consumption, which is the lowest of any OFDM device in the market today.

1.1 Analogue-to-Digital Converter

The MT352 has a high performance 10-bit analogue-to-digital converter (ADC) which can sample a 6, 7 or 8 MHz

bandwidth OFDM signal, with its spectrum centred at :

- 4.57 MHz near-zero IF
- 36.17 MHz IF
- 43.75 MHz IF

The ADC can be clocked using :

- Crystal oscillator with a 20.48 MHz crystal
- 4 MHz or 27 MHz clock input

An on-chip programmable phase locked loop (PLL) is used to generate the ADC sampling clock. The crystal frequency of 20.48 MHz is used for 36.17 MHz IF sampling and 19.6267 MHz is used for 43.75 MHz IF sampling. Note that this 19.6267 MHz sampling clock can be generated from the 20.48 MHz crystal by appropriately programming the PLL. Hence the same 20.48 MHz crystal can support 6, 7 and 8 MHz OFDM as well as 36.17 and 43.75 MHz IF.

1.2 Automatic Gain Control

An AGC module compares the absolute value of the digitised signal with a programmable reference. The error signal is filtered and is used to control the gain of the amplifier. A sigma-delta modulated output is provided, which has to be RC low-pass filtered to obtain the voltage to control the amplifier. Upper and lower limits can be set to the AGC control voltage using registers.

The programmable AGC reference has been optimised. A large value for the reference leads to excessive ADC clipping and a small value results in excessive quantisation noise. Hence the optimum value has been determined assuming the input signal amplitude to be Gaussian distributed. The latter is justified by applying the central limit theorem in statistics to the OFDM signal, which consists of a large number of randomly modulated carriers. This reference or target value may have to be lowered slightly for some applications. Slope control bits have been provided for the AGCs and these have to be set correctly depending on the Gain-versus-Voltage slope of the gain control amplifiers.

The bandwidth of the AGC is set to a large value for quick acquisition then reduced to a small value for tracking. The AGC is free running during OFDM channel changes and locks to the new channel while the tuner lock is being established. This is one of the features of MT352 used to minimise acquisition time. A robust AGC lock mechanism is provided and the other parts of the MT352 begin to acquire only after the AGC has locked. Two AGC control outputs are available, one to drive an RF amplifier and the other to control an IF amplifier. The parameters for both loops are programmable. In the default mode, only the IF AGC loop is activated.

1.3 IF to Baseband Conversion

Sampling a 36.17 MHz IF signal at 20.48 MHz results in a spectrally inverted OFDM signal centred at 4.79 MHz.

Sampling a 43.75 MHz IF signal at 19.6267 MHz gives a non-inverted signal at 4.5 MHz. The first step of the demodulation process is to convert this signal to a complex (in-phase and quadrature) signal in baseband. A correction for spectral inversion is implemented during this conversion process. Note also that the MT352 has control mechanisms to search automatically for an unknown spectral inversion status.

1.4 Adjacent Channel Filtering

Adjacent channels, in particular the Nicam digital sound signal associated with analogue channels, are filtered prior to the FFT.

1.5 Interpolation and Clock Synchronisation

MT352 uses digital timing recovery and this eliminates the need for an external VCXO. The ADC samples the signal at a fixed rate, for example, 20.48 MHz. Conversion of the 20.48 MHz signal to the OFDM sample rate is achieved using the time-varying interpolator. The OFDM sample rate is 64/7 MHz for 8 MHz and this is scaled by factors 6/8 and 7/8 for 6 and 7 MHz channel bandwidths. The nominal ratio of the ADC to OFDM sample rate is programmed in a MT352 register (defaults are for 20.48 MHz sampling and 8 MHz OFDM). The clock recovery phase locked loop in the MT352 compensates for inaccuracies in this ratio due to uncertainties of the frequency of the sampling clock.

1.6 Carrier Frequency Synchronisation

There can be frequency offsets in the signal at the input to OFDM, partly due to tuner step size and partly due to broadcast frequency shifts, typically 1/6 MHz. These are tracked out digitally, without the need for an analogue frequency control (AFC) loop.

The default frequency capture range has been set to ±285 kHz in the 2 K mode and ±142 kHz in the 8 K mode. However, these values can be doubled, if necessary, by programming an on-chip register. It is recommended that this larger capture range be used for channel scan in order to find channels with broadcast frequency shifts, without having to adjust the tuner.

After the OFDM module has locked, the frequency offset can be read from an on-chip register.

1.7 Symbol Timing Synchronisation

This module computes the optimum sample position to trigger the FFT in order to eliminate or minimise inter-symbol interference in the presence of multi-path distortion. Furthermore, this trigger point is continuously updated to dynamically adapt to time-variations in the transmission channel.

1.8 Fast Fourier Transform

The FFT module uses the trigger information from the timing synchronisation module to set the start point for an FFT. It then uses either a 2 K or 8K FFT to transform the data from the time domain to the frequency domain. An extremely hardware-efficient and highly accurate algorithm has been used for this purpose.

1.9 Common Phase Error Correction

This module subtracts the common phase offset from all the carriers of the OFDM signal to minimise the effect of the tuner phase noise on system performance.

1.10 Channel Equalisation

This consists of two parts. The first part involves estimating the channel frequency response from pilot information. Efficient algorithms have been used to track time-varying channels with a minimum of hardware. The second part involves applying a correction to the data carriers based on the estimated frequency response of the channel. This module also generates dynamic channel state information (CSI) for every carrier in every symbol.

1.11 Impulse Filtering

MT352 contains several mechanisms to reduce the impact of impulse noise on system performance.

1.12 Transmission Parameter Signalling (TPS)

An OFDM frame consists of 68 symbols and a superframe is made up of four such frames. There is a set of TPS carriers in every symbol and all these carry one bit of TPS. These bits, when combined, include information about the transmission mode, guard ratio, constellation, hierarchy and code rate, as defined in ETS 300 744. In addition, the first eight bits of the cell identifier are contained in even frames and the second eight bits of the cell identifier are in odd frames. The TPS module extracts all the TPS data, and presents these to the host processor in a structured manner.

1.13 De-Mapper

This module generates soft decisions for demodulated bits using the channel-equalised in-phase and quadrature components of the data carriers as well as per-carrier channel state information (CSI). The de-mapping algorithm depends on the constellation (QPSK, 16QAM or 64QAM) and the hierarchy α = 0, 1, 2 or 3). Soft decisions for both low- and high-priority data streams are generated.

1.14 Symbol and Bit De-Interleaving

The OFDM transmitter interleaves the bits within each carrier and also the carriers within each symbol. The de-interleaver modules consist largely of memory to invert these interleaving functions and present the soft decisions to the FEC in the original order.

1.15 Viterbi Decoder

The Viterbi decoder accepts the 5-bit soft decision data from the OFDM demodulator and outputs a decoded bit-stream. The decoder does the de-puncturing of the input data for all code rates other than 1/2. It then evaluates the branch metrics and passes these to a 64-state path-metric updating unit, which in turn outputs a 64-bit word to the survivor memory. The Viterbi decoded bits are obtained by tracing back the survivor paths in this memory. A trace-back depth of 128 is used to minimise any loss in performance, especially at high code rates.

The decoder re-encodes the decoded bits and compares these with received data (delayed) to compute bit errors at its input, on the assumption that the Viterbi output BER is significantly lower than its input BER.

1.16 MPEG Frame Aligner

The Viterbi decoded bit stream is aligned into 204-byte frames. A robust synchronisation algorithm is used to ensure correct lock and to prevent loss of lock due to noise impulses.

1.17 De-interleaver

Errors at the Viterbi output occur in bursts and the function of the de-interleaver is to spread these errors over a number of 204-byte frames to give the Reed-Solomon decoder a better chance of correcting these. The de-interleaver is a memory unit which implements the inverse of the convolutional interleaving function introduced by the transmitter.

1.18 Reed-Solomon Decoder

Every 188-byte transport packet is encoded by the transmitter into a 204-byte frame, using a truncated version of a systematic (255,239) Reed-Solomon code. The corresponding (204,188) Reed-Solomon decoder is capable of correcting up to eight byte errors in a 204-byte frame. It may also detect frames with more than eight byte errors. In addition to efficiently performing this decoding function, the Reed-Solomon decoder in MT352 keeps a count of the number of bit errors corrected over a programmable period and the number of uncorrectable blocks. This information can be used to compute the post-Viterbi BER.

1.19 De-scrambler

The de-scrambler de-randomises the Reed-Solomon decoded data by generating the exclusive-OR of this with a pseudo-random bit sequence (PRBS). This outputs 188-byte MPEG transports packets. The TEI bit of the packet header is set to indicate uncorrectable packets.

1.20 MPEG Transport Interface

MPEG data can be output in parallel or serial mode. The output clock frequency is automatically chosen to present the MPEG data as uniformly spaced as possible to the transport processor. This frequency depends on the guard ratio, constellation, hierarchy and code rate. There is also an option for the data to be extracted from the MT352 with a clock provided by the user.

2.0 Software control

Acquisition of an OFDM channel and frequency scan for OFDM channels are controlled by an on-chip state machine, which minimises the software requirement in the host processor. To acquire a channel, the host programs the channel frequency in the MT352. The on-chip state machine then writes the frequency information to the tuner, awaits tuner lock and acquires the OFDM channel to generate the transport stream. The controller can be made to automatically search for every parameter in the OFDM signal, including spectral inversion status. Furthermore, this controller will re-acquire the channel in the event of an interruption to the incoming signal.

To scan a frequency range, the host programs the start and end frequencies for the search as well as the step size, which defaults to 8 MHz. The MT352 then automatically scans the frequency range by appropriately programming the tuner and searching for OFDM signals. Once a channel has been located, the host is interrupted to read the channel information from the MT352. Then MT352 continues the search. By default, only the channels which can generate a reliable transport stream are reported, but there is also provision for locating very weak channels. The frequency capture range of MT352 can be maximised to capture channels with frequency offsets without re-programming the tuner, in both 2 K and 8 K modes.

The above approach to channel acquisition and scan has resulted in very fast acquisition and scan times whilst minimising software overhead in the host processor. Furthermore, all this functionality has very efficiently been mapped into hardware to result in a device consuming less than 220 mW of power.

3.0 Interfaces

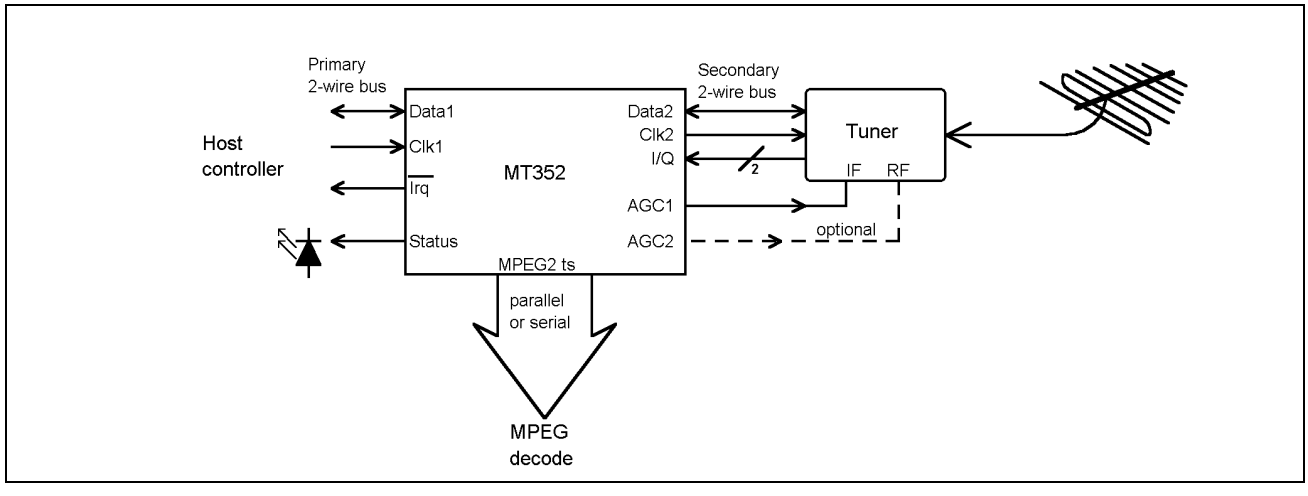


Figure 5 - Primary Interfaces

The MT352 interfaces to other parts of a terrestrial receiver system can be partitioned into three groups: the host controller, the tuner and the MPEG decoder. One other pin, the Status output, is multi-functional and can directly

drive a LED to show the status of a range of different internal lock flags. Alternatively, it can drive an audio transducer to give an audio frequency that is dependent upon the error rate of the received signal.

This feature can be used for faster installation of a system where the aerial may need to be adjusted, as signal strength is not the best guide for the optimum aerial position for COFDM reception.

3.1 2-Wire Bus

3.2 Host

The primary 2-wire bus serial interface uses pins:

- DATA1 (pin 5) serial data, the most significant bit is sent first.
- CLK1 (pin 4) serial clock.

The 2-wire bus address is determined by applying VDD or VSS to the SADD[4:0] pins.

In the current TNIM evaluation application, the 2-wire bus address is 0001 111 R/ $\overline{W}$ with the pins connected as follows:

ADDR[7]	ADDR[6]	ADDR[5]	ADDR[4]	ADDR[3]	ADDR[2]	ADDR[1]
Not programmable		SADD[4]	SADD[3]	SADD[2]	SADD[1]	SADD[0]
VSS	VSS	VSS	VDD	VDD	VDD	VDD

Table 1 - Programmable Address Details for 2-Wire Bus in TNIM Evaluation Application

When the MT352 is powered up, the $\overline{\text{RESET}}$ pin 28 should be held low for at least 50ms after VDD has reached normal operation levels. As the $\overline{\text{RESET}}$ pin goes high, the logic levels on SADD[4:0] are latched as the 2-wire bus address. ADDR[0] is the R/ $\overline{W}$ bit.

The circuit works as a slave transmitter with the lsb set high or as a slave receiver with the lsb set low. In receive mode, the first data byte is written to the RADD virtual register, which forms the register sub-address. The RADD register takes an 8-bit value that determines which of 256 possible register addresses is written to by the following byte. Not all addresses are valid and many are reserved registers that must not be changed from their default values. Multiple byte reads or writes will auto-increment the value in RADD, but care should be taken not to access the reserved registers accidentally.

Following a valid chip address, the 2-wire bus STOP command resets the RADD register to 00. If the chip address is not recognised, the MT352 will ignore all activity until a valid chip address is received. The 2-wire bus START command does NOT reset the RADD register to 00. This allows a combined 2-wire bus message, to point to a particular read register with a write command, followed immediately with a read data command. If required, this could next be followed with a write command to continue from the latest address. RADD would not be sent in this case. Finally, a STOP command should be sent to free the bus.

When the 2-wire bus is addressed (after a recognised STOP command) with the read bit set, the first byte read out is the contents of register 00.

3.2.1 Tuner

The MT352 has a General Purpose Port that can be configured to provide a secondary 2-wire bus. Master control mode is selected by a single register control bit.

The allocation of the pins is: GPP0 pin 35 = CLK2, GPP1 pin 36 = DATA2.

3.2.2 Examples of 2-Wire Bus Messages

KEY:	S	Start Condition	W	Write (=0)
	P	Stop condition	R	Read (= 1)
	A	Acknowledge	NA	NOT Acknowledge
	Italics	MT352 output	RADD	Register Address

Write operation - as a slave receiver:

S	DEVICE ADDRESS	W	A	RADD (n)	A	DATA (reg n)	A	DATA (reg n+1)	A	P

Read operation - MT352 as a slave transmitter:

S	DEVICE ADDRESS	R	A	DATA (reg 0)	A	DATA (reg 1)	A	DATA (reg 2)	NA	P

Write/read operation with repeated start - MT352 as a slave transmitter:

S	DEVICE ADDRESS	W	A	RADD (n)	A	S	DEVICE ADDRESS	R	A	DATA (reg n)	A	DATA (reg n+1)	NA	P

3.2.3 Primary 2-Wire Bus Timing

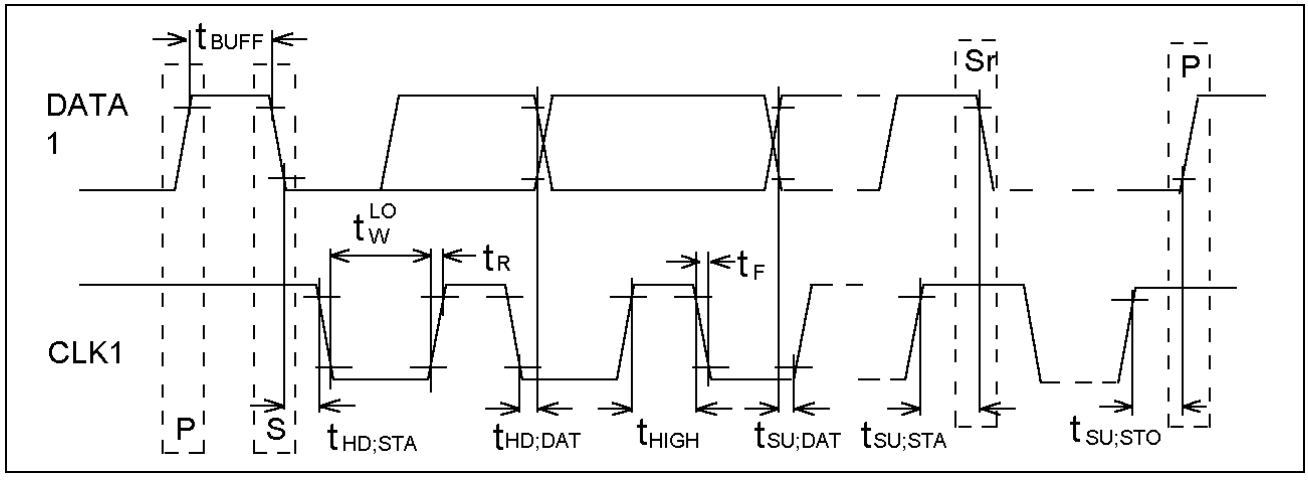


Figure 6 - Primary 2-Wire Bus Timing

Where: S = Start

Sr = Restart, i.e., start without stopping first.

P = Stop.

Parameter	Symbol	Value		Unit
		Min.	Max.	
CLK clock frequency (Primary)	f_{CLK}	0	450	kHz
Bus free time between a STOP and START condition	t_{BUFF}	200		ns
Hold time (repeated) START condition	$t_{HD;STA}$	200		ns
LOW period of CLK clock	t_{LOW}	1300		ns
HIGH period of CLK clock	t_{HIGH}	600		ns
Set-up time for a repeated START condition	$t_{SU;STA}$	200		ns
Data hold time (when input)	$t_{HD;DAT}$	100		ns
Data set-up time	$t_{SU;DAT}$	100		ns
Rise time of both CLK and DATA signal.	t_R		note 1	ns
Fall time of both CLK and DATA signals, (100 pF to ground)	t_F	20		ns
Set-up time for a STOP condition	$t_{SU;STO}$	200		ns

Table 2 - Timing of 2-Wire Bus

Note 1. The rise time depends on the external bus pull up resistor. Loading prevents full speed operation.

3.3 MPEG

3.3.1 Data Output Header Format

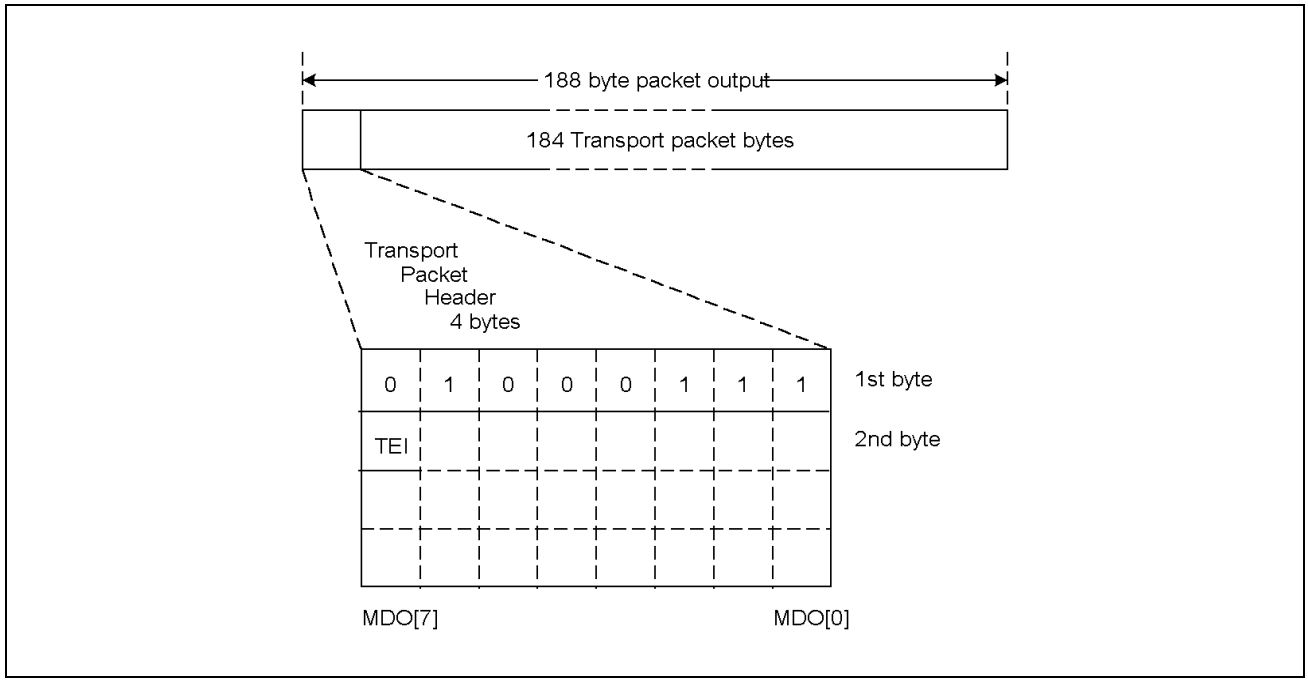


Figure 7 - DVB Transport Packet Header Byte

After decoding the 188-byte MPEG packet, it is output on the MDO pins in 188 consecutive clock cycles. Additionally when the ENTEI bit in the CONFIG register (0x8A) is set high (default), the TEI bit of any uncorrectable packet will automatically be set to '1'. If ENTEI bit is low then TEI bit will not be changed (but note that if this bit is already 1, for example, due to a channel error which has not been corrected, it will remain high at output).

3.3.2 MPEG data output signals

The $\overline{\text{MPEGEN}}$ bit in the CONFIG register must be set low to enable the MPEG data. The maximum movement in the packet synchronization byte position is limited to ±1 output clock period. MOCLK will be a continuously running clock once symbol lock has been achieved, and is derived from the symbol clock. In Figure 8, MOCLK is shown in with MOCLKINV = '1', the default state.

All output data and signals (MDO[7:0], MOSTRT, MOVAL & $\overline{\text{BKERR}}$) change on the negative edge of MOCLK

(MOCLKINV = 1) to present stable data and signals on the positive edge of the clock.

A complete packet is output on MDO[7:0] on 188 consecutive clocks and the MDO[7:0] pins will remain low during the inter-packet gaps. MOSTRT goes high for the first byte clock of a packet. MOVAL goes high on the first byte of a packet and remains high until the last byte has been clocked out. $\overline{\text{BKERR}}$ goes low on the first byte of a packet where uncorrectable bytes are detected and will remain low until the last byte has been clocked out.

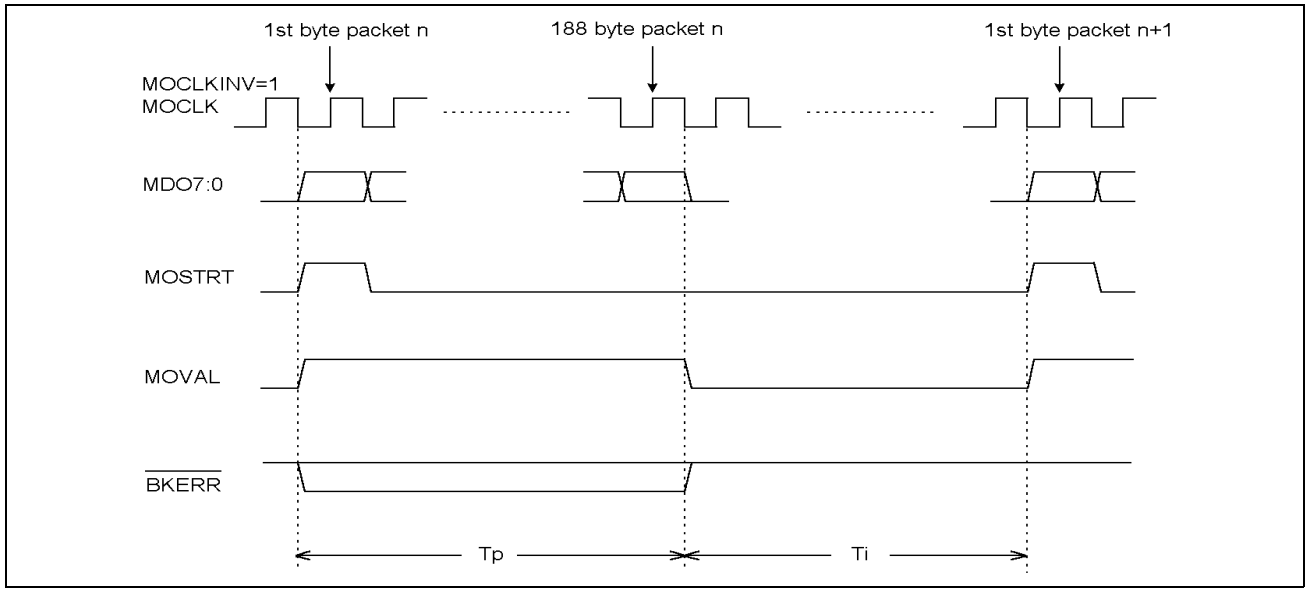


Figure 8 - MPEG Output Data Waveforms

3.3.3 MPEG Output Timing

Maximum delay conditions: VDD = 3.0 V, CVDD = 1.62 V, Tamb = 70^{o}C, Output load = 10 pF

Minimum delay conditions: VDD = 3.6 V, CVDD = 1.98 V, Tamb = 0^{o}C, Output load = 10 pF

MOCLK frequency = 61.44 MHz.

3.3.3.1 MOCLKINV = 1

Parameter	Maximum Delay Conditions	Minimum Delay Conditions
Data output delay t_D	7 ns	0.3 ns
Setup Time t_{SU}	0.5 ns	5 ns
Hold Time t_H	8 ns	8 ns

Table 3 - MOCLKINV = 1

The setup time is due to the delay on MOSTRT, MOVAL and $\overline{\text{BKERR}}$. MDO[0] is faster since it uses a stronger output driver cell.

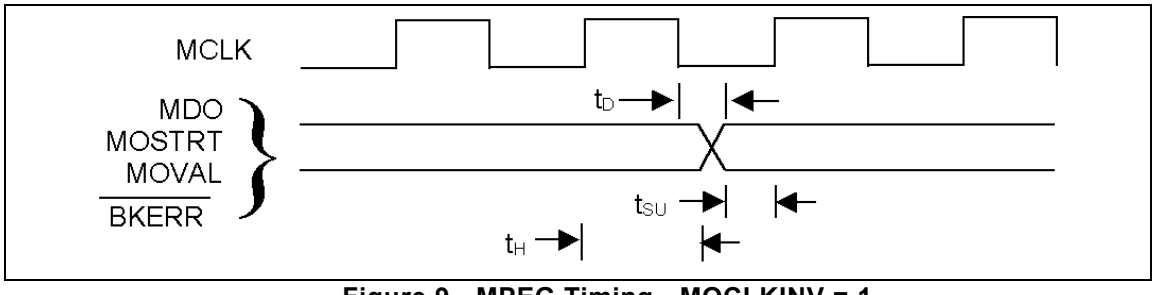


Figure 9 - MPEG Timing - MOCLKINV = 1

3.3.3.2 MOCLKINV = 0

MDOSWAP = 0

Parameter	Maximum Delay Conditions	Minimum Delay Conditions
Data output delay t_D	8 ns	0.7 ns
Setup Time t_{SU}	8 ns	15 ns
Hold Time t_H	1.5 ns	0.5 ns

Table 4 - MDOSWAP = 0

The hold time is due to the fast output on MDO[0]. If MDOSWAP is set to 1 the data output is on MDO[7] which has a slower driver. This improves the hold time:

MDOSWAP = 1

Parameter	Maximum Delay Conditions	Minimum Delay Conditions
Data output delay t_D	8 ns	0.7 ns
Setup Time t_{SU}	8 ns	15 ns
Hold Time t_H	3 ns	1.2 ns

Table 5 - MDOSWAP = 1

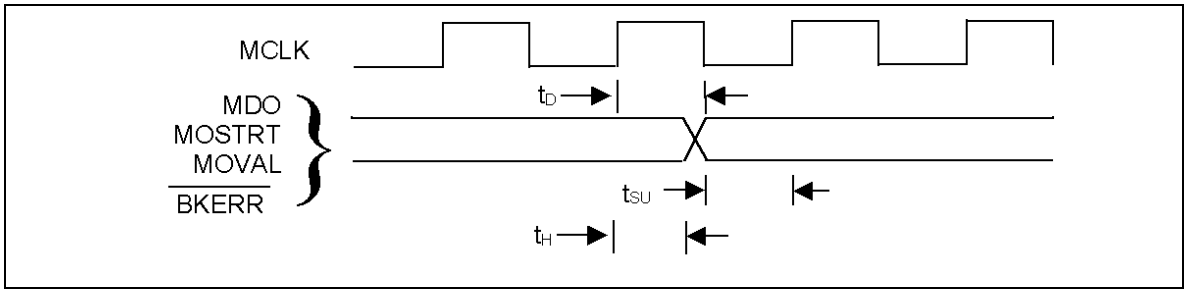


Figure 10 - MPEG Timing - MOCLKINV = 0

4.0 Electrical Characteristics

4.1 Recommended Operating Conditions

Recommended Operating Conditions Table

Parameter		Symbol	Min.	Typ.	Max.	Units
Power supply voltage:	periphery	VDD	3·0	3·3	3·6	V
	core	CVDD	1·62	1·8	1·98	V
Power supply current:	periphery [1]	IDD_P		1		mA
	core	IDD_C		120		mA
Input clock frequency [2]		XTI	16·00	20·48	25·00	MHz
CLK1 primary serial clock frequency		fCLK			450	kHz
Ambient operating temperature			0		70	°C
ADC Input Impedance @ 36 MHz				2		kΩ

1. Current from the 3·3 VV supply will be mainly dependent on the external loads.
2. The min/max frequencies given are those supported by the oscillator cell. Frequencies outside these limits are acceptable with an external clock signal.

4.2 Absolute maximum ratings

Absolute Maximum Ratings Table

Parameter	Symbol	Min.	Max.	Unit
Power supply	VDD	-0.3	+3.6	V
	CVDD	-0.3	+2.0	V
Voltage on input pins (5 V rated)	VI	-0.3	5.5	V
Voltage on input pins (3.3 V rated)	VI	-0.3	VDD + 0.3	V
Voltage on output pins (5 V rated)	VO	-0.3	5.5	V
Voltage on output pins (3.3 V rated)	VO	-0.3	VDD + 0.3	V
Storage temperature	TSTG	-55	150	°C
Operating ambient temperature	TOP	0	70	°C
Junction temperature	TJ		125	°C

Note: Stresses exceeding these listed under absolute maximum ratings may induce failure. Exposure to absolute maximum ratings for extended periods may reduce reliability. Functionality at or above these conditions is not implied.

4.3 DC Electrical Characteristics

Parameter	Conditions	Pins	Symbol	Min.	Typ.	Max.	Unit
Operating periphery voltage			VDD	3.0	3.3	3.6	V
core			CVDD	1.62	1.8	1.98	V
Supply current	1.62 ≤ CVDD ≤ 1.98		IDD-CORE		120		mA
Supply current sleep mode					200		µA
Outputs							
Output levels	IOH 2 mA 3.0 ≤ VDD ≤ 3.6	MDO(7:0), MOVAL, MOSTRT, MOCLK, STATUS, $\overline{\text{BKERR}}$	VOH	2.4			V
	IOL 2 mA 3.0 ≤ VDD ≤ 3.6		VOL			0.4	V
	IOL 6 mA 3.0 ≤ VDD ≤ 3.6	GPP(3:0), DATA1, AGC1, AGC2, $\overline{\text{IRQ}}$	VOL			0.4	V
Output capacitance	Not including track	MDO(7:0), MOVAL, MOSTRT, MOCLK, STATUS, $\overline{\text{BKERR}}$			3.0		pF
		GPP(3:0), DATA1, AGC1, AGC2 $\overline{\text{IRQ}}$			3.6		pF
Output leakage (tri-state)						1	µA
Inputs							
Input levels	3.0 ≤ VDD ≤ 3.6 -0.5 ≥ Vin ≥ VDD+0.5 V	MICLK, SADD(4:0), SLEEP, OSC-MODE	VIH	2.0			V
Input levels	3.0 ≤ VDD ≤ 3.6 -0.5 ≥ Vin ≥ +5.5 V	GPP(3:0), CLK1, DATA1, $\overline{\text{RESET}}$	VIH	2.0			V
Input levels	3.0 ≤ VDD ≤ 3.6 Capacitances do not include track	All inputs	VIL			0.8	V
Input leakage Current		SLEEP, SMTEST, MICLK, CLK1, OSCMODE				±1	µA
Input capacitance					1.8		pF
Input capacitance		SADD(4:0), DATA1, GPP(3:0)			3.6		pF

4.4 Crystal Specification and External Clocking

Parallel resonant fundamental frequency (preferred)	20.4800 MHz
Tolerance over operating temperature range	± 25 ppm
Tolerance overall	± 50 ppm
Typical load capacitance	27 pF
Drive level	0.4 mW max.
Equivalent series resistance	<50 Ω

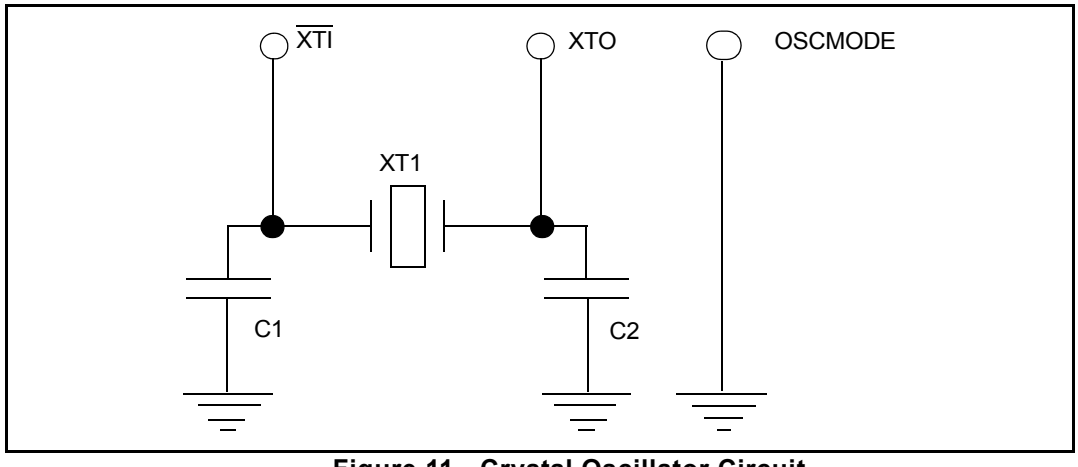


Figure 11 - Crystal Oscillator Circuit

5.0 Application Circuit

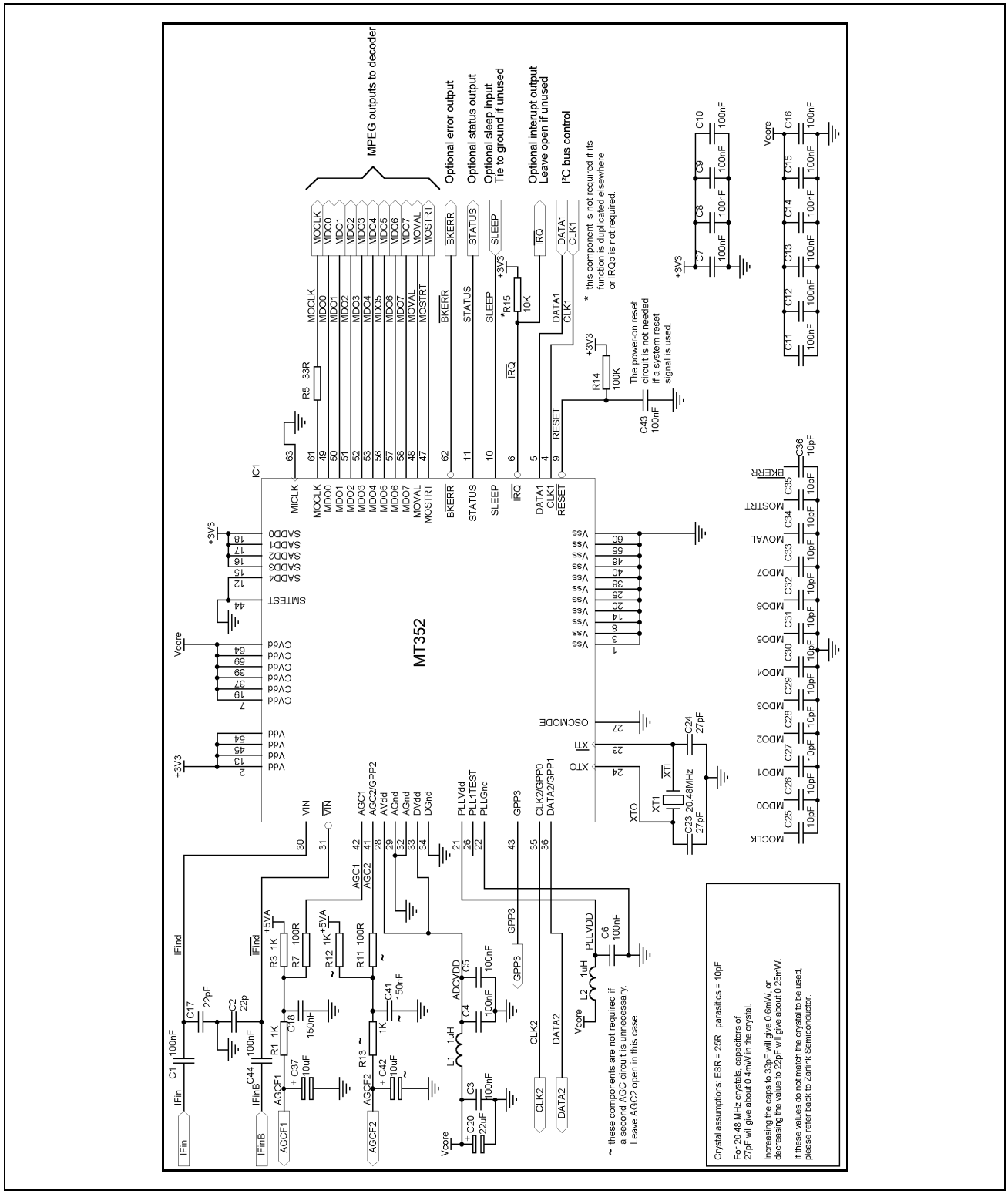
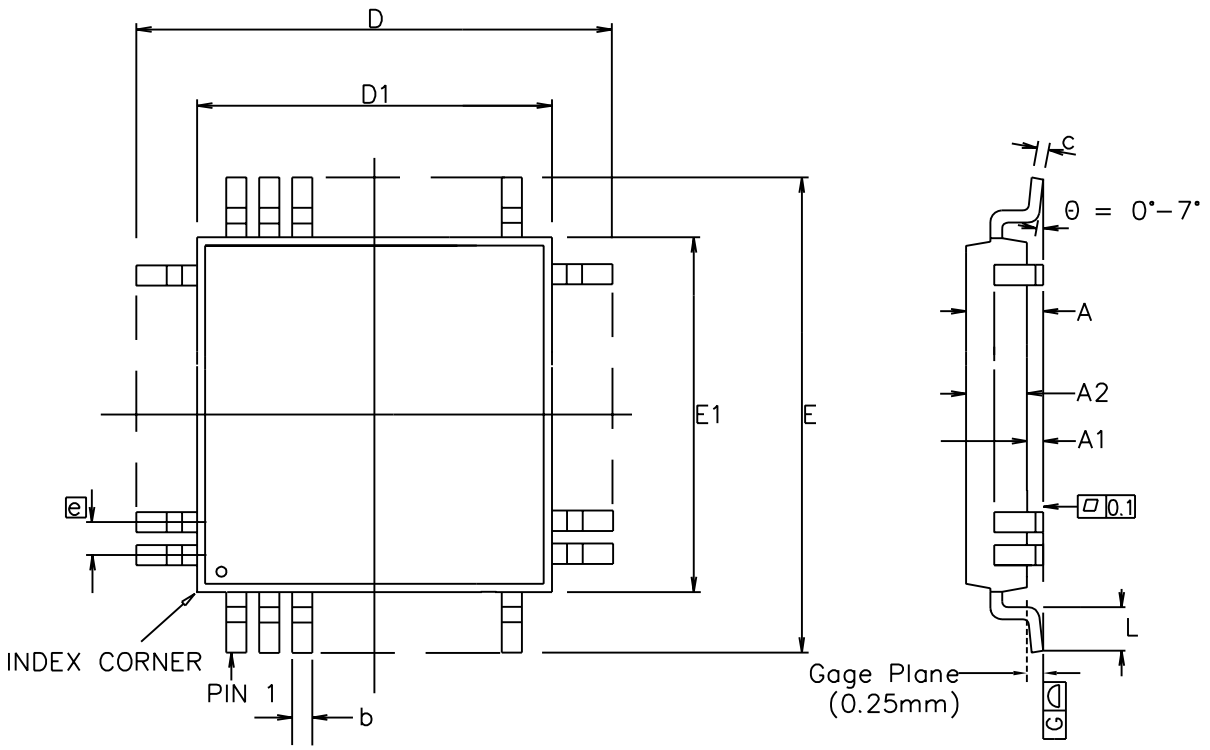


Figure 12 - Typical Application Circuit



Symbol	Control Dimensions in millimetres			Altern. Dimensions in inches	
	MIN	MAX		MIN	MAX
A	---	1.60		---	0.063
A1	0.05	0.15		0.002	0.006
A2	1.35	1.45		0.053	0.057
D	12.00 BSC			0.472 BSC	
D1	10.00 BSC			0.394 BSC	
E	12.00 BSC			0.472 BSC	
E1	10.00 BSC			0.394 BSC	
L	0.45	0.75		0.018	0.030
e	0.50 BSC			0.020 BSC	
b	0.17	0.27		0.007	0.011
c	0.09	0.20		0.004	0.008
	Pin features				
N	64				
ND	16				
NE	16				
NOTE	SQUARE				

Conforms to JEDEC MS-026 BCD Iss. C

Notes:
1. Pin 1 indicator may be a corner chamfer, dot or both.
2. Controlling dimensions are in millimeters.
3. The top package body size may be smaller than the bottom package body size by a max. of 0.15 mm.
4. Dimension D1 and E1 do not include mould protusion.
5. Dimension b does not include dambar protusion.
6. Coplanarity, measured at seating plane G, to be 0.08 mm max.

This drawing supersedes 418/ED/51210/018 (Swindon)

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ZARLINK SEMICONDUCTOR

Previous package codes

GP / B

Package Code QC

Package Outline for 64 lead LQFP (10 x 10 x 1.4mm) 2.0mm Footprint

GPD00254

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