MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

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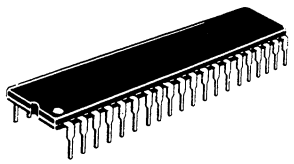
MC68HC24

Advance Information

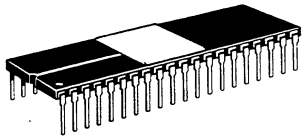
Port Replacement Unit (PRU)

The MC68HC24 is a peripheral device which replaces ports B and C of the MC68HC11 microcomputer (MCU). These ports are lost when the MCU is placed in the expanded or special test modes of operation. Port B is a general purpose output port. Port C is a general purpose input/output port complemented by full handshake capability. This device can also be used in an emulator as a replacement for port B, port C, STRA, and STRB. Applications requiring external memory in early production or top of the line models can also use the MC68HC24 for parallel I/O. When used in these expanded systems, a later switch to a single chip solution will be transparent to software.

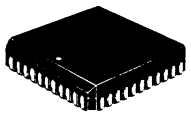
The MC68HC24 is not restricted to simply replacing MC68HC11 ports. The MC68HC24 should be considered as a cost-effective solution for any CMOS microcomputer system requiring I/O expansion, parallel printer interface, or interprocessor communications in multiple MCU systems.



CASE 711
PLASTIC



CASE 715
CERAMIC



CASE 777A
PLCC

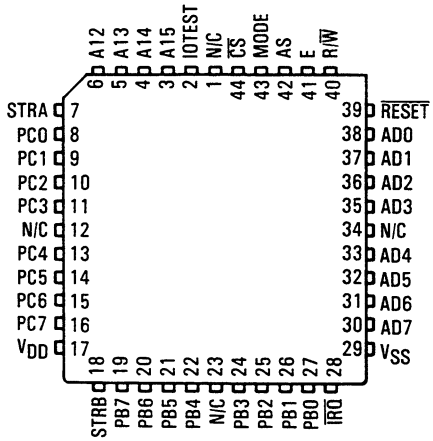
Hardware Features

- Supports All Handshake and I/O Modes of the MC68HC11 Ports
- Automatic Conformance to the MC68HC11 Variable Memory Map
- Multiplexed Address/Data Bus
- 3.0- to 5.5-Volt Operation
- Can Be Used with the MC68HC11, MC68HC01, MC146805E2, MC146805E3, and other CMOS Microcomputers
- 0- to 2.1-MHz Operation

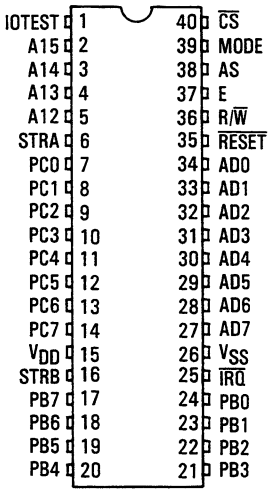
Software Features

- Software Compatible to MC68HC11 in Single-Chip Mode
- Minimizes Software Overhead for Parallel I/O Handshake Protocols

PIN ASSIGNMENT
(QUAD)



PIN ASSIGNMENT
(DUAL-IN-LINE)



This document contains information on a new product. Specifications and information herein are subject to change without notice.

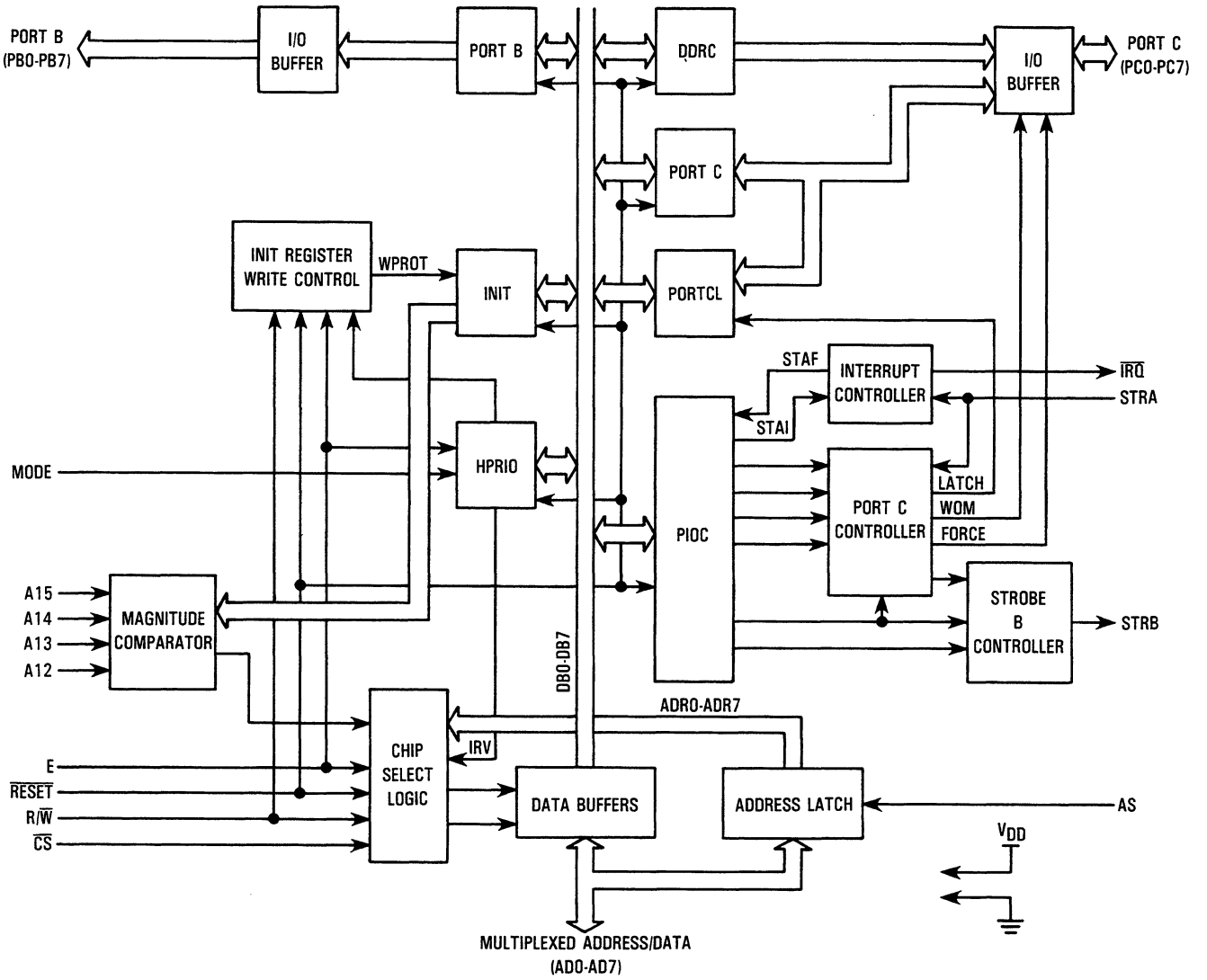


Figure 1. Block Diagram

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0.5 to +7.0	V
Input Voltage	V_{in}	V_{SS} −0.5 to V_{DD} +0.5	V
Current Drain per Pin	I_{IK}	25	mA
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

This device contains circuitry which protects the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

THERMAL CHARACTERISTICS

Characteristics	Symbol	Value	Unit
Thermal Resistance	θ_{JA}		°C/W
Ceramic 40-Pin DIP		50	
Plastic 40-Pin DIP		100	
Plastic 44-Pin Quad Pack		TBD	

POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

Where:

$T_A \equiv$ Ambient Temperature, °C

$\theta_{JA} \equiv$ Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D \equiv P_{INT} + P_{PORT}$

$P_{INT} \equiv I_{CC} \times V_{CC}$, Watts — Chip Internal Power

$P_{PORT} \equiv$ Port Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{PORT} \ll P_{INT}$ and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P_D and T_J (if P_{PORT} is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

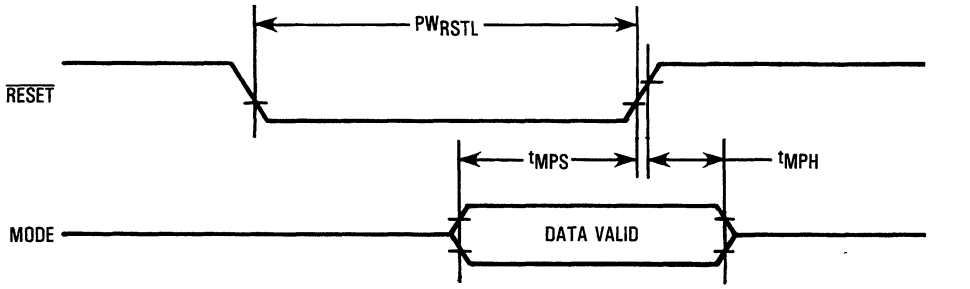
$$K = T_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

MODE SELECTION ELECTRICAL CHARACTERISTICS

(V_{DD} = 5.0 V ± 10%, V_{SS} = 0 Vdc, T_A = 25°C unless otherwise noted)(see Figure 2)

Characteristic	Symbol	Min	Typ	Max	Unit
Mode Programming Voltage Low	V_{MPL}	0	—	$0.2 \times V_{DD}$	V
Mode Programming Voltage High	V_{MPH}	$0.7 \times V_{DD}$	—	V_{DD}	V
$\overline{\text{RESET}}$ Low Input Pulse Width	PW_{RSTL}	2	—	—	E_{cyc}
Mode Programming Setup Time	t_{MPS}	2	—	—	E_{cyc}
Mode Programming Hold Time	t_{MPH}	0	—	—	E_{cyc}



NOTE: Measurement points are V_{OL}, V_{OH}, V_{IL}, V_{IH}.

Figure 2. Mode Selection Timing

DC ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0 V ± 10%, V_{SS} = 0 Vdc, T_A = −40°C to +85°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Output Voltage (I_{Load} = ±10 μA) All Outputs	V_{OL}	—	0.1	V
All Outputs Except $\overline{IRQ}$ (see Note 1)	V_{OH}	$V_{DD}-0.1$	—	
Output Low Voltage (I_{Load} = 1.6 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{Load} = −0.8 mA, V_{DD} = 4.5 V) All Outputs Except $\overline{IRQ}$ (see Note 1)	V_{OH}	$V_{DD}-0.8$	—	V
Input Low Voltage All Inputs	V_{IL}	V_{SS}	$0.2\times V_{DD}$	V
Input High Voltage All Inputs	V_{IH}	$0.7\times V_{DD}$	V_{DD}	V
I/O Ports, 3-State Leakage (V_{in} = V_{DD} or V_{SS}) PB0-PB7, PC0-PC7, AD0-AD7	I_{OZ}	—	±10	μA
Input Current (V_{in} = V_{DD} or V_{SS}) E, AS, R/$\overline{W}$, $\overline{CS}$, MODE, A12-A15, IOTEST, STRA	I_{IN}	—	±1	μA
Total Supply Current (see Note 2)	I_{DD}	—	5	mA
Input Capacitance E, AS, R/$\overline{W}$, $\overline{CS}$, MODE A12-A15, IOTEST, STRA	C_{in}	—	8.0	pF
PB0-PB7, PC0-PC7, AD0-AD7		—	12.0	
Power Dissipation	P_D	—	25	mW

NOTES:
1. V_{OH} specification for $\overline{IRQ}$ is not applicable because it is an open-drain output pin.
2. Test conditions for total supply current are as follows:
   a. C_L = 90 pF on Port B and AD0 through AD7, no dc loads, t_{cyc} = 500 ns.
   b. Port C programmed as inputs.
   c. V_{IL} = V_{SS} + 0.2 V for PC0-PC7, AD7-AD2 and AD0 (during E = V_{IL}), $\overline{CS}$
      V_{IH} = V_{DD} − 0.2 V for $\overline{RESET}$, R/$\overline{W}$, AD1 (during E = V_{IL}), MODE.
   d. The E input is a squarewave from V_{SS} + 0.2 V to V_{DD} − 0.2 V.
   e. AS input is 25% duty cycle from V_{SS} + 0.2 V to V_{DD} − 0.2 V.

PERIPHERAL PORT TIMING

(V_{DD} = 5.0 V ± 10%, all timing is shown with respect to 20% V_{DD} and 70% V_{DD} unless otherwise noted)

Characteristics	Symbol	Min	Max	Unit	Fig. No.
Peripheral Data Setup Time (Port C)	t_{PDSU}	200	—	ns	4
Peripheral Data Hold Time (Port C)	t_{PDH}	10	—	ns	4
Delay Time, E Negative Transition to Peripheral Data Valid (Ports B and C, see Note 1)	t_{PWD}	—	100	ns	3
Input Data Setup Time (Port C)	t_{IS}	50	—	ns	6, 7
Input Data Hold Time (Port C)	t_{IH}	10	—	ns	6, 7
Delay Time, E Positive Transition to STRB Asserted (see Note 1)	t_{DEB}	—	80	ns	5, 8, 9
Delay Time, E Positive Transition to STRB Negated Handshake Mode (see Note 1)	t_{DEBN}	—	80	ns	7, 9
Setup Time, STRA Asserted to E Negative Transition (see Note 2)	t_{AES}	0	—	ns	7, 8, 9
Delay Time, STRA Asserted to Port C Data Out Valid (see Note 3)	t_{PCD}	—	100	ns	9
Hold Time, STRA Negated to Port C Data	t_{PCH}	10	—	ns	9
Three-State Hold Time	t_{PCZ}	—	150	ns	9
STRA Cycle Time	t_{Scyc}	2	—	E_{cyc}	6, 7

NOTES:
1. The method of calculating the timing for this characteristic differs from the MC68HC11.
2. If this setup time is met, STRB will be acknowledged in the next cycle. If it is not met, the response will be delayed one more cycle.
3. Port C timing is only valid for active drive (CWOM bit is not set in PIOC).

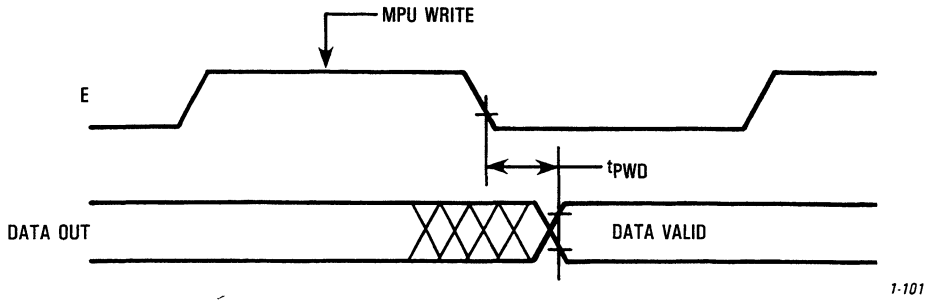


Figure 3. Port Write Timing

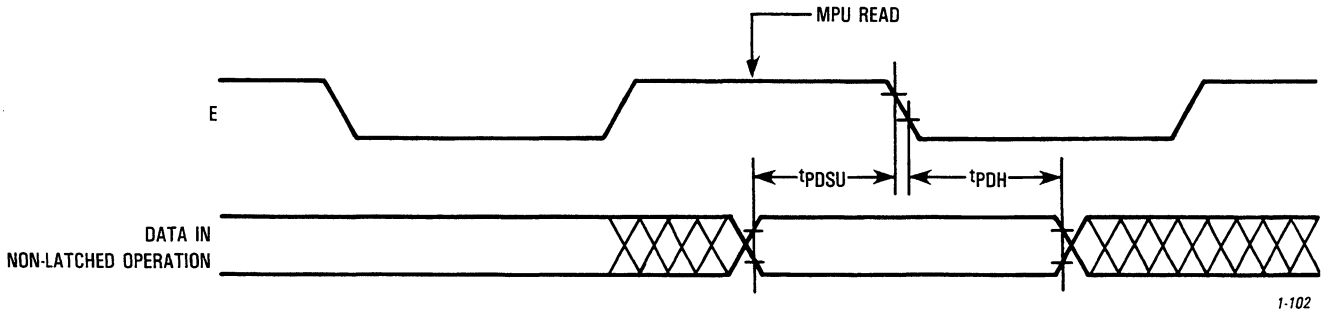


Figure 4. Port C Static Read Timing

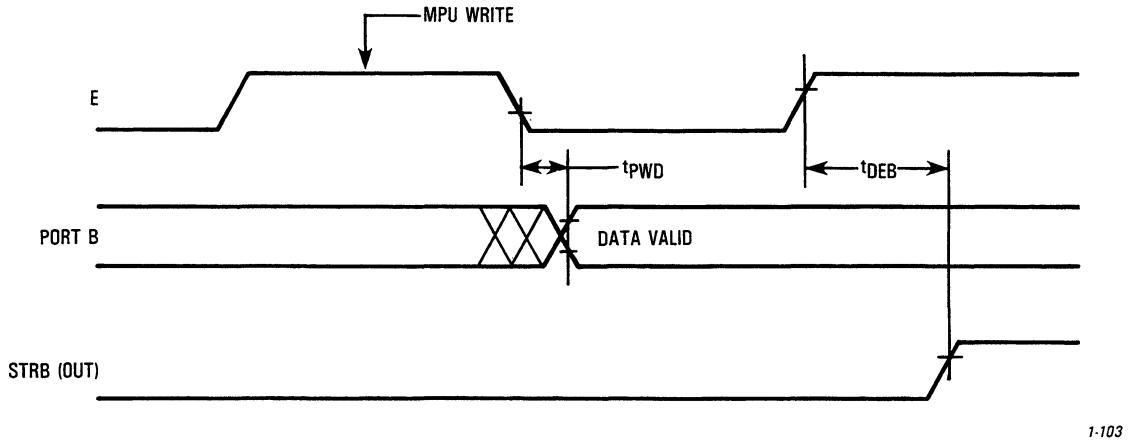


Figure 5. Simple Output Strobe Timing

NOTE: Measurement points are V_{OL}, V_{OH}, V_{IL}, and V_{IH}

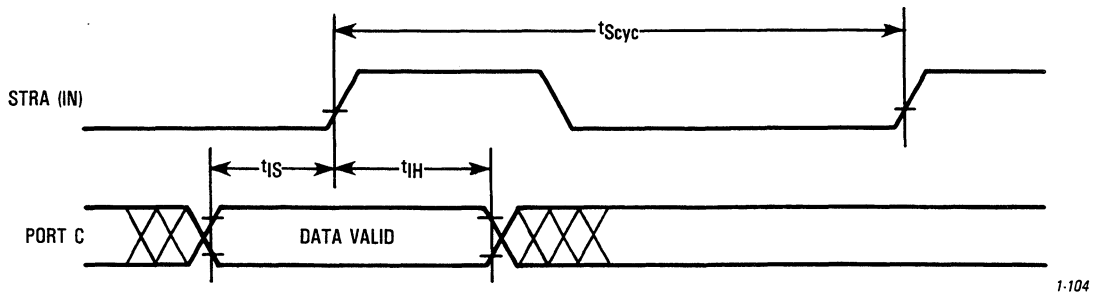


Figure 6. Simple Input Strobe Timing

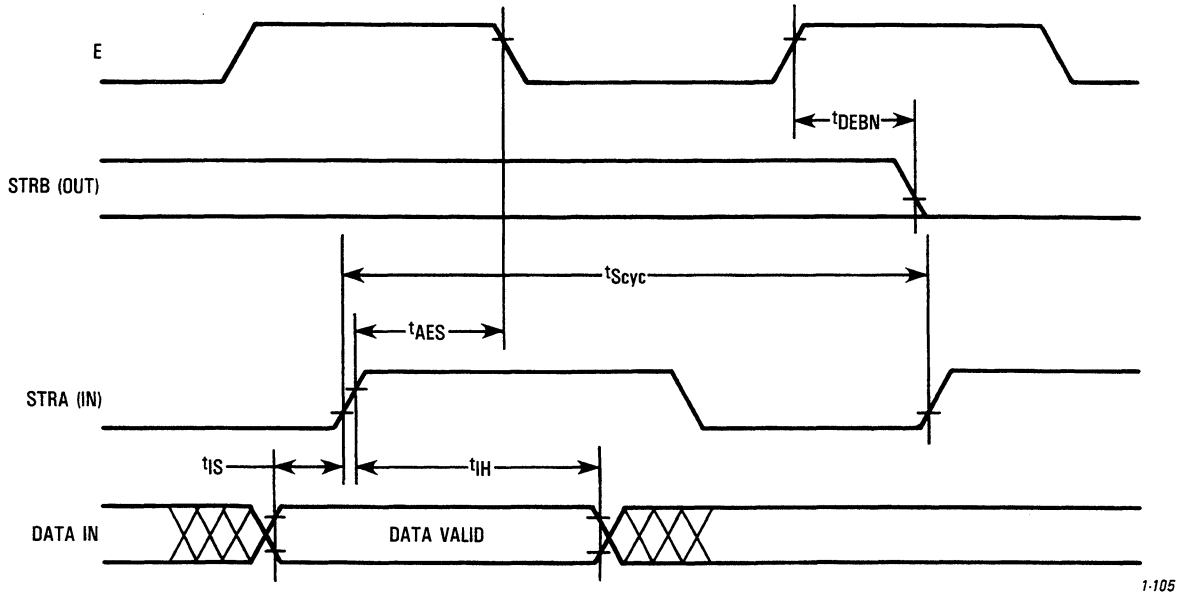


Figure 7. Port C Input Handshake Timing

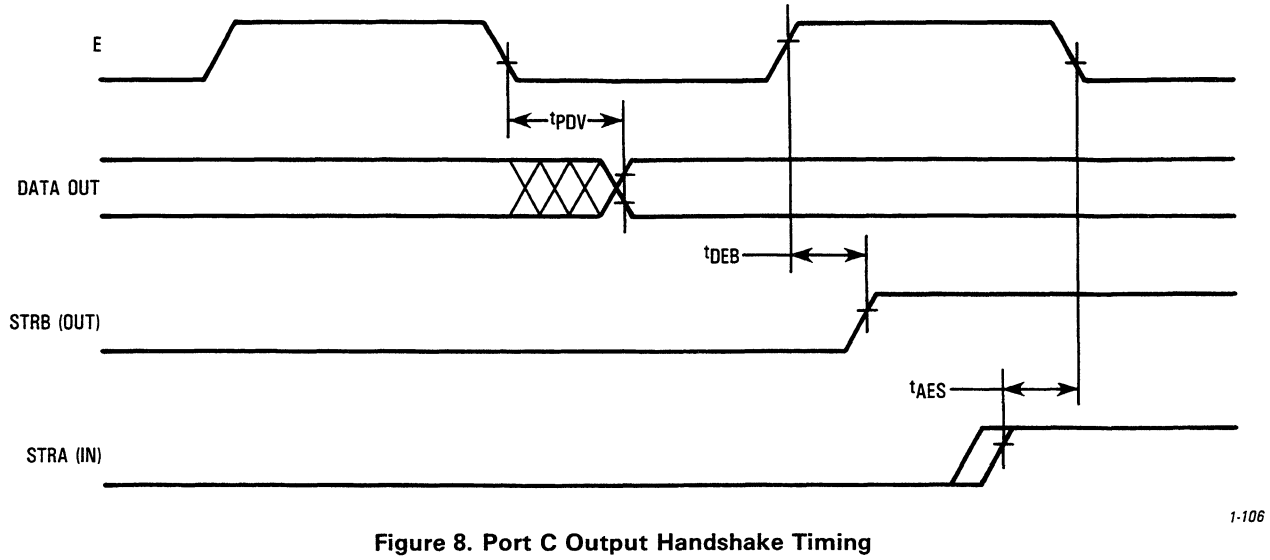
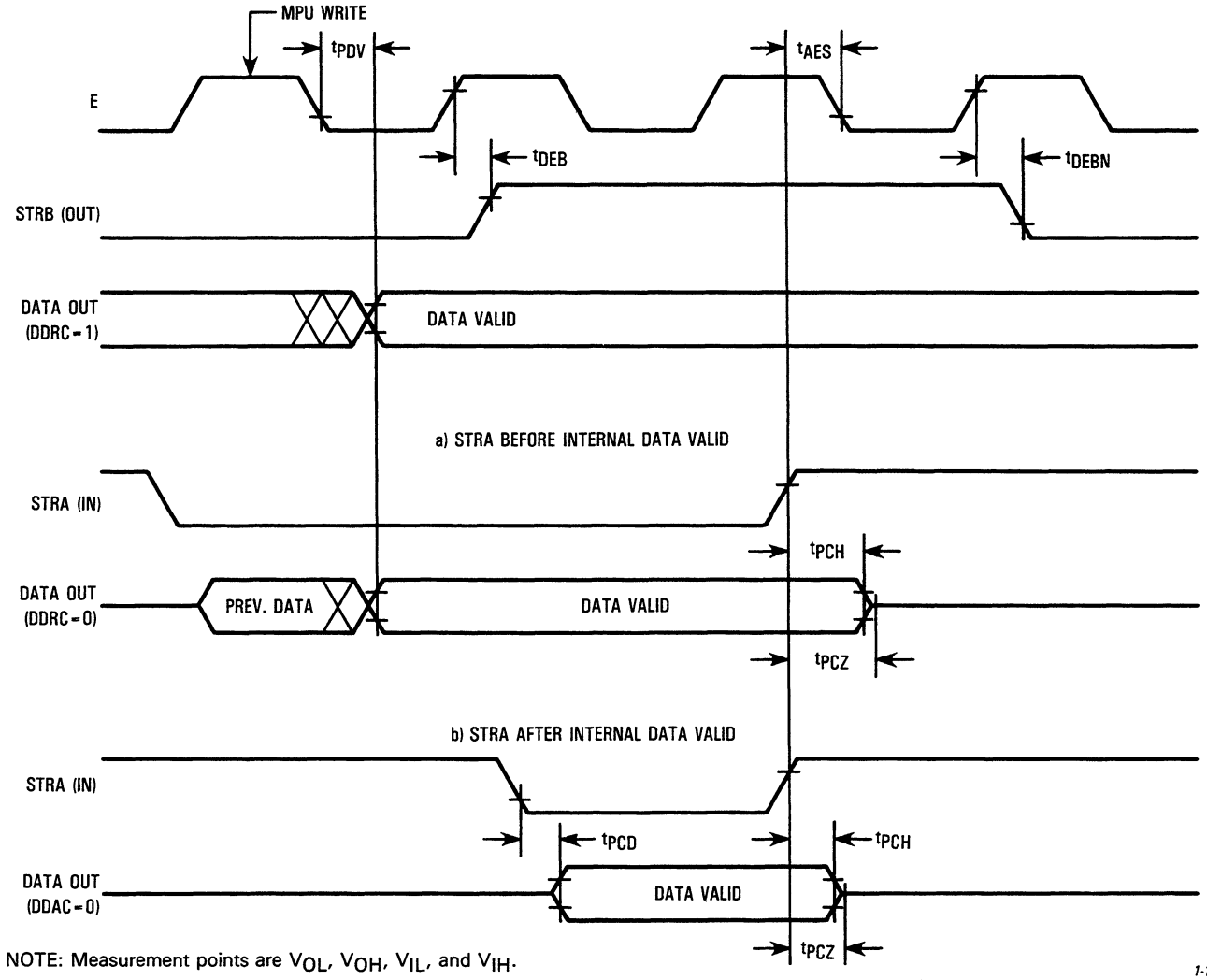


Figure 8. Port C Output Handshake Timing

NOTE: Measurement points are V_{OL}, V_{OH}, V_{IL}, and V_{IH}.



NOTE: Measurement points are V_{OL}, V_{OH}, V_{IL}, and V_{IH}.

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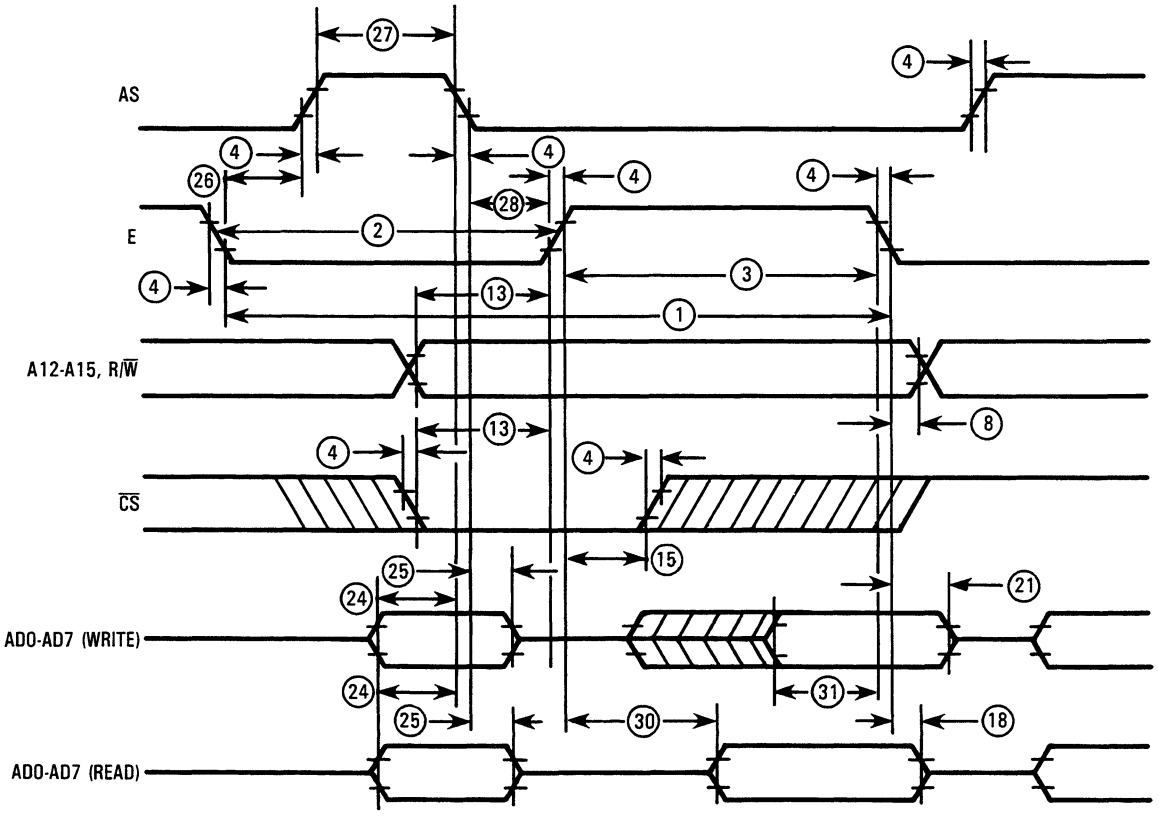
Figure 9. Port C Three-State Output Handshake Timing

BUS TIMING CHARACTERISTICS

(V_{DD} = 5.0 V ± 10%, V_{SS} = 0 Vdc, T_A = −40° to +85°C unless otherwise noted; see Figure 10 for detailed timing diagrams)

Ident. Number	Characteristic	Symbol	1 MHz		2.1 MHz		Unit
			Min	Max	Min	Max	
1	Cycle Time	t_{cyc}	1000	—	476	—	ns
2	Pulse Width, E Low	PW_{EL}	430	—	200	—	ns
3	Pulse Width, E High	PW_{EH}	450	—	210	—	ns
4	Input and Clock Rise and Fall Time	t_r, t_f	—	25	—	20	ns
8	R/$\overline{W}$ Hold Time	t_{RWH}	20	—	10	—	ns
13	Setup Time Before Rising Edge of E (R/$\overline{W}$, $\overline{CS}$)	t_{RWS}	100	—	50	—	ns
15	Chip Select Hold Time ($\overline{CS}$)	t_{CSH}	20	—	20	—	ns
18	Read Data Hold Time	t_{DHR}	10	75	10	75	ns
21	Write Data Hold Time	t_{DHW}	10	—	10	—	ns
24	Muxed Address Valid Time to AS Fall	t_{ASL}	60	—	30	—	ns
25	Muxed Address Hold Time	t_{AHL}	40	—	20	—	ns
26	Delay Time, E Fall to AS Rise	t_{ASD}	60	—	30	—	ns
27	AS Pulse Width High	t_{WASH}	150	—	75	—	ns
28	AS Fall to E Rise	t_{ASED}	60	—	30	—	ns
30	Peripheral Output Data Delay Time from E Rise (Read)	t_{DDR}	20	240	10	120	ns
31	Peripheral Data Setup Time (Write)	t_{DSW}	150	—	75	—	ns



NOTE: Measurement points are V_{OL}, V_{OH}, V_{IL}, and V_{IH}.

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Figure 10. Bus Timing Diagram

PIN DESCRIPTION

The input and output pins for the port replacement unit are described in the following paragraphs.

V_{DD} AND V_{SS}

Power is supplied to the peripheral using these two pins. Power is V_{DD} and ground is V_{SS}.

RESET ($\overline{RESET}$)

This active-low control input pin is used to initialize the MC68HC24 to a known start-up state. The system state after a reset is detailed in **STATE AFTER RESET**. This pin must remain at a low level for a minimum of two E-clock cycles to be recognized.

ENABLE (E)

The E clock input is the basic MPU/MCU clock. This clock provides most timing reference information to the MC68HC24. In general, when E is low, an internal process is taking place. When E is high, data is being accessed.

The E-clock runs at the external bus rate of the MPU/MCU and may range in frequency from dc to the maximum operating frequency of the device (i.e., this peripheral part is static). More information on the timing relationships between the various signals may be found in **PERIPHERAL PORT TIMING** and **BUS TIMING CHARACTERISTICS**.

ADDRESS STROBE (AS)

The AS input pulse serves to demultiplex the address/data bus. The falling edge of AS causes the addresses AD0 through AD7 to be latched within the MC68HC24.

READ/WRITE (R/$\overline{W}$)

The read/write pin is a high-impedance input signal which is used to control the direction of data flow along the multiplexed address/data bus. When the device is selected and the R/$\overline{W}$ input is high, the data output buffers are enabled and a selected register is read.

Data is written into the selected register when the chip is selected with R/$\overline{W}$ low. R/$\overline{W}$ signal is not latched by the MC68HC24. In order to guarantee that register contents are not corrupted, R/$\overline{W}$ must be stable prior to the rising edge of the E clock and must remain stable throughout the E clock high time.

CHIP SELECT ($\overline{CS}$)

This input pin serves as the device chip select. The MC68HC24 is selected when 1) $\overline{CS}$ is low, 2) the contents of the INIT register match address lines A12 through A15, and 3) the lower order address lines (AD0 through AD7) select an internal register address. All three of these conditions must be met to access the internal registers. The $\overline{CS}$ signal is latched on the rising edge of the E clock and must be stable prior to that edge.

No action will take place within the MC68HC24 during bus cycles in which 1) $\overline{CS}$ is not asserted, 2) the A12 through A15 address lines do not match the contents of the INIT register, or 3) an internal register is not addressed.

ADDRESS AND DATA BUS (AD0 through AD7)

Multiplexed bus microprocessors save pins by presenting the address during the first portion of the bus cycle and using those same pins during the second portion of the bus cycle for data. Address and data multiplexing does not slow the access time of the MC68HC24 since the bus reversal from address to data occurs during the internal register access time.

The low-order address must be stable (valid) prior to the fall of AS at which time the MC68HC24 latches the address present on AD0 through AD7. If the latched address is decoded, if $\overline{CS}$ is asserted, and if A12 through A15 match the contents of the INIT register, a selected register will be accessed.

Although a 64-byte register block is reserved for the registers, only seven of the locations are currently implemented. See **INTERNAL REGISTER DESCRIPTION** for details about specific addresses.

Valid write data must be presented by the MPU/MCU during the E high period of the write cycle. In a read cycle, the MC68HC24 outputs eight bits of data during the second half of the read bus cycle and then ceases driving the bus (returns to a high-impedance state) after the falling edge of E.

HIGH-ORDER ADDRESS (A12 through A15)

The address lines, A12 through A15, are the nonmultiplexed high-order address lines of the MPU/MCU. These signals are used internally to establish a partial decoding for the chip select. They are latched by the rising edge of the E clock and must be stable prior to this edge. A magnitude comparator checks the value of these lines against a value stored in the INIT register. If they match, $\overline{CS}$ is asserted, and an internal register is addressed, the device will be accessed during the current bus cycle.

PORT B (PB0 through PB7)

Port B (PB0 through PB7) is an 8-bit general purpose output port. In the simple strobed mode of operation, STRB is pulsed for each write to port B. See **I/O PORTS** for more information.

PORT C (PC0 through PC7)

Each line of port C is individually programmable as either an input or an output via its data direction register (DDRC). An I/O pin is an input when its corresponding DDR bit is a logic zero and an output when the DDR bit is a logic one. Several handshake modes are available on this port (see **I/O PORTS**).

STROBE A (STRA)

Strobe A is an edge detecting input used by port C. In the simple strobed and input handshake modes of operation, the programmed edge on STRA will latch the data on the port C inputs into PORTCL. In the output handshake mode, STRA is an edge-sensitive acknowledge input signal indicating that port C output data has been accepted by the external device.

STROBE B (STRB)

While operating in the simple strobed I/O mode, Strobe B is a strobe output which pulses for each write to port B. In the full handshake mode of parallel I/O, STRB acts as a handshake output line. The STRB pin is a READY output in the

input handshake mode, inhibiting the external device from strobing new data into port C. In the output handshake mode, STRB is again a READY output; however, in this case it indicates that new data has been written to port C by the microprocessor.

INTERRUPT REQUEST ($\overline{IRQ}$)

The $\overline{IRQ}$ output pin is an open-drain active-low signal that may be used to interrupt the microprocessor with a service request. The open drain output allows multiple devices to be wire-ORed together. This configuration requires an external resistor to V_{DD} as no internal pullup is provided.

The MC68HC11 I/O port interrupts share the same vector address as $\overline{IRQ}$. As a result, an expanded MC68HC11 system incorporating an MC68HC24 (to replace the displaced I/O features) will appear to the software as a single chip solution. Refer to the **INTERNAL REGISTER DESCRIPTION—PIOC** and **I/O PORTS—FULL HANDSHAKE I/O** for additional information.

I/O TEST (IOTEST)

This is a factory test feature and the IOTEST pin must be tied directly to V_{SS} for normal operation.

I/O PORTS

There are two 8-bit parallel I/O ports on the MC68HC24. Port B is a general purpose output-only port, whereas port C may be used as general purpose input and/or output pins as specified by DDRC. In conjunction with STRA and STRB, ports B and C may be used for special strobed and handshake modes of parallel I/O as well as general purpose I/O.

GENERAL PURPOSE I/O (PORT C)

When used as general purpose I/O signals, each bit has associated with it one bit in the PORTC data register and one bit in the corresponding position in the data direction register (DDRC). The DDRC is used to specify the primary direction of data on the I/O pin; however, specification of a line as an output does not disable the ability to read the line as a latched input.

When a bit which is configured as an output is read, the value returned will be the value at the input to the pin driver. When a pin is configured as an input (by clearing the DDRC bit) the pin becomes a high-impedance input. When writing to a bit that is configured as an input, the value will not affect the I/O pin; however, the bit will be stored to an internal latch so that if the line is later recognized as an output this value will appear at the I/O pin.

This operation can be used to preset a value for an output port prior to configuring it as an output, so that glitches of an output state which are not defined for the external system may be avoided. Reset configures the port for input by clearing both the DDR and the data register.

FIXED DIRECTION I/O (PORT B)

Port B is a general purpose output-only port. The data direction is fixed in order to properly emulate the operation of the MC68HC11 port B. Reads of port B return the levels sensed at the input of the pin drivers. Write data is stored in an internal latch which directly drives the output pin driver. Reset clears the data register forcing the outputs low.

SIMPLE STROBED I/O

The simple strobed mode of parallel I/O is controlled by the parallel I/O control (PIOC) register. This mode is selected when the HNDS bit in the PIOC register is clear. This mode forces PORTCL to be a strobed input port with the STRA pin used as the edge detecting latch command input. Also, port B becomes a strobed output port with the STRB pin acting as the output strobe.

Strobed Input Port C

In this mode, there are two addresses where port C may be read—PORTC data register and PORTCL latch register. Even when the strobed input mode is selected, one or all of the bits in port C may be used as general purpose I/O lines. In other words, the DDRC register still controls the data direction of all port C pins.

The STRA pin is used as an edge-detecting input. Either falling or rising edges may be specified as the significant edge by use of the EGA bit in PIOC. Whenever the selected active edge is detected at the STRA pin, the current logic levels at port C are latched into the PORTCL register and the strobe A flag (STAF) bit in PIOC is set.

If the STAI bit in PIOC is also set, then an interrupt sequence is requested on the $\overline{IRQ}$ pin. The STAF flag is automatically cleared by reading the PIOC register (with STAF set) followed by a read of the PORTCL register. Additional active edges of STRA continue to latch new data into PORTCL regardless of the state of the STAF flag. Consecutive active edges on STRA must be a minimum of two E-clock cycles apart.

Reads of the PORTCL register return the last value latched, while reads of PORTC return the static level of the port C pins (inputs) or the level at the input to the pin driver (outputs).

Strobed Output Port B

In this mode, the STRB pin is a strobe output which is pulsed each time there is a write to port B. Data written to PORTB is stored in a latch which drives the port B pin drivers. Reads of port B return the levels at the inputs of those pin drivers.

The INVB bit in the PIOC register controls the polarity of the pulse out of the STRB pin. If the INVB bit is set, the strobe pulse will be a high going pulse (two E-clock periods long) on a normally low line. If the INVB bit is clear, the strobe pulse will be low-going pulse (two E-clock periods long) on a normally high line.

FULL HANDSHAKE I/O

The full handshake modes of parallel I/O involve port C, STRA, and STRB. There are two basic modes (input and output) and an additional variation on the output handshake mode that allows for three-state operation of port C. In all handshake modes, STRA is an edge detecting input and STRB is a handshake output line. The effect of DDRC is discussed in **Input Handshake Protocol, Output Handshake Protocol, Three State Variation**, and **Interaction of Handshake and General Purpose I/O.**

Input Handshake Protocol

In the handshake scheme, port C is a latching input port, STRA is an edge-sensitive latch command from the external system that is driving port C and STRB is a READY output line controlled by logic in the MC68HC24.

In a typical system, an external device wishing to pass data to port C would test the READY line (STRB). When a ready condition was recognized, the external device would place data on the port C inputs followed by a pulse on the STRA input to the MC68HC24. The active edge on the STRA line would latch the port C data into the PORTCL register, set the STAF flag (optionally causing an interrupt), and deassert the READY line (STRB). Deassertion of the READY line would automatically inhibit the external device from strobing new data into port C. Reading the PORTCL latch register, after reading PIOC with STAF set, clears the STAF flag. Whenever PORTCL is read, the READY (STRB) line is asserted indicating that new data may now be strobed into port C.

The STRB line can be configured (with the PLS control bit) to be a pulse output (pulse mode) or a static output (interlocked mode). The only difference between the pulse and interlock modes is that in pulse mode, the READY line pulses (asserts) for only two E-clock periods after the latched data becomes available. While in interlock mode, the asserted state of the READY line lasts until new data is strobed into port C via the STRA input line.

The port C DDR bits should be cleared (input) for each bit that is to be used as a latched input bit. It is, however, possible to use some port C bits as latched inputs with the input handshake protocol and at the same time use other port C bits as static inputs and still other port C bits as static output bits.

The input handshake protocol has no effect on the use of port C bits as static inputs or static outputs. Reads of the PORTC register always return the static logic level at the port C pins (for lines configured as input) or at the inputs to the pin drivers (for lines configured as outputs). Data latched into PORTCL always reflects the level at the port C pins. Writes to either the PORTC address or the PORTCL address will write information to the port C output register without affecting the input handshake strobes.

NOTE

After programming PIOC to enter the input handshake mode, STRB will remain in the inactive state. This precaution has been taken to ensure that the external system will not strobe data into PORTCL before all intialization is complete. When ready to accept data, the MPU/MCU should perform a dummy read of the PORTCL address. This operation will assert STRB initiating the input handshake protocol.

Output Handshake Protocol

In the output handshake scheme, port C is an output port, STRB is a READY output, and STRA is an edge-sensitive acknowledge input signal indicating that port C output data has been accepted by the external device. In a variation of this output handshake operation, STRA is used as an output enable input as well as an edge-sensitive acknowledge input.

In a typical system, the controlling processor writes to the MC68HC24, placing data in the port C output latch. Stable data on the port C pins is indicated by the automatic assertion of the MC68HC24 READY (STRB) line. The external device then processes the available data and pulses the STRA input to indicate that new data may be placed on the port C output lines. The active edge on STRA causes the READY (STRB) line to be automatically deasserted and the STAF status flag to be set (optionally causing an interrupt). In response to STAF being set, the program puts out new data on port C as required.

There are two addresses associated with the port C data register, the normal PORTC data address and a second address (PORTCL) that accesses the input latch on reads and the normal port on writes. On writes to the second address (PORTCL), the data goes to the same port output register as it would on a write to the PORTC address but the STAF flag bit is cleared (provided PIOC was first read with the STAF bit set). This allows an automatic clearing mechanism in output handshake modes to co-exist with normal port C outputs.

All eight bits in port C must be used as outputs while the output handshake protocol is selected. That is, part of port C may not be used for static or latched inputs while the remaining bits are being used for output handshake. The following paragraphs cover this limitation in more detail.

Output Handshake Protocol, Three-State Variation

There is a variation to the output handshake protocol that allows three-state operation of port C. It is possible to directly interconnect this 8-bit parallel port to other 8-bit three-state devices with no additional external parts.

The STRA signal is used as an acknowledge/enable input whose sense is controlled by the EGA bit in the PIOC register. The EGA bit specifies the transition from the asserted to the deasserted state of the STRA input signal. If EGA is zero, the asserted state is high and falling edges are interpreted as acknowledge signals. If EGA is one, the asserted state is low and rising edges are interpreted as acknowledge signals.

As long as the STRA input pin is negated, all port C bits obey the data direction specified by DDRC. Bits which are configured as inputs (DDR bit equals zero) will be high impedance. When the STRA input is asserted, all port C lines are forced to be outputs regardless of the data in DDRC.

This operation limits the ability to use some port C bits as static inputs while using others as handshake outputs. However, it does not interfere with the use of some port C bits as static outputs while others are being used as three-state handshake outputs. Port C bits which are to be used as static outputs or normal handshake outputs should have their corresponding DDRC bits set. Bits which are to be used as three-state handshake outputs should have their corresponding DDRC bits clear.

Interaction of Handshake and General Purpose I/O

There are two addresses associated with the port C data register: the normal PORTC address and a second address (PORTCL) that accesses the input latch on reads and the normal port on writes. On writes to the second address (PORTCL), the data goes to the same port output register as it would on a write to the port output address. When operating in the output handshake mode, writing to PORTC will not clear

the STAF bit whereas writing to PORTCL will clear it. This allows an automatic clearing mechanism to co-exist with normal port C outputs.

When full input handshake protocol is specified, both general purpose input and/or general purpose output can co-exist at port C. However, the three-state feature of the output handshake mode interferes with general purpose inputs in two ways.

First, in full output handshake, the port C pins are forced to be driven outputs during any period in which STRA is in its active state regardless of the state of the DDRC bits. This potentially conflicts with any device trying to drive port C unless the external device has an open-drain type output driver.

Secondly, the value returned on reads of port C is the state at the inputs to the pin drivers regardless of the state of the DDRC bits. This allows data written for output handshake to be read even if the pins are in a three-state condition.

The following is an example of port C being used for full input handshake, general purpose input, and general purpose output all at the same time. Assume that the PIOC and DDRC control registers are set up as follows:

```
PIOC=0111 0000    /STAF/STAI/CWOM/HNDS/ /OIN/PLS/EGA/INVB/
DDRC=0000 1100    /MSB...  ...LSB/
```

In this example, port C bits b7 through b4 will be used for input handshake, bits b3 and b2 will be used as open-drain type general purpose outputs, and bits b0 and b1 will be used as general purpose inputs. The DDRC register is configured such that bits b2 and b3 are outputs and the rest of the port C bits are inputs. The PIOC register is configured such that full-input handshake is specified (HNDS equals one and OIN equals zero). CWOM equals one so any pins in port C which are configured as outputs will behave as open-drain type outputs. The other bits in PIOC are not important for the discussion of this example.

When data is latched into PORTCL according to the input handshake protocol, all eight bits are captured although only the four MSBs are of interest to the input handshake software. The data latched into all eight bits of PORTCL will be the levels present at port C pins.

Software driving the bits b2 and b3 general-purpose outputs would perform writes to PORTC which would not affect the handshake protocol or the latching of data into PORTCL. Data written to port C bits b0, b1, and b4 through b7 would also be latched into the internal port C output latch but since the corresponding DDRC bits are zeros, the corresponding port C pins would remain unaffected.

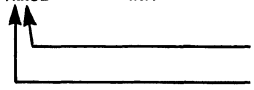
Bit manipulation and read-modify-write instructions could be used on PORTC because reads of PORTC do not affect the input handshake functions. Although writes to PORTCL would also cause data to be written to port C, this address should not be used for general purpose output. This is because bit manipulation and read-modify-write instructions read the location before writing to it and this read would interfere with the input handshake protocol.

Finally, to use bits 0 and 1 for general purpose inputs, simply read PORTC which will return the desired information and will not interfere with the input handshake protocol. Note that the current state of the port C bits b4 through b7 are also read; therefore, even the pins which are being used for input handshake can be read at any time without disturbing the input handshake function.

INTERNAL REGISTER DESCRIPTION

A 64-byte address space is reserved for internal register access, although not all 64 addresses are used. The ABSOLUTE locations where these addresses will appear are specified by the reset initialization software and chip select logic provided by the end user (see INIT register). The following list summarizes the register mnemonics and their associated addresses.

$xx02	PIOC	PARALLEL I/O CONTROL REGISTER
$xx03	PORTC	I/O PORT C
$xx04	PORTB	OUTPUT PORT B
$xx05	PORTCL	ALTERNATE LATCHED PORT C
$xx07	DDRC	PORT C DATA DIRECTION REGISTER
$xx3C	HPRIO	HIGHEST PRIORITY I-BIT INTERRUPT AND MISCELLANEOUS
$xx3D	INIT	I/O MAPPING REGISTER



SPECIFIED BY CHIP SELECT DECODING

SPECIFIED BY BITS 0 THROUGH 3 OF THE INIT REGISTER

PARALLEL I/O CONTROL REGISTER (PIOC)

The PIOC register is an 8-bit read/write register except for bit 7 which is a read-only flag bit.

b7	b6	b5	b4	b3	b2	b1	b0	
STAF	STAI	CWOM	HNDS	OIN	PLS	EGA	INVB	$xx02
0	0	0	0	0	0	1	1	RESET

b7, STAF — The STAF (strobe A interrupt status flag) bit is set when a selected active edge is detected by the STRA input pin. If b6 (STAI) is set, then an interrupt sequence using the $\overline{IRQ}$ output pin will also be requested whenever the STAF flag is set. This bit is cleared by reset to indicate no interrupt request is pending.

There is an automatic clearing mechanism on this flag bit (STAF) which depends on the operating mode selected. There are three basic strobed modes (see b4, HNDS and b3, OIN).

When HNDS is zero, the simple strobed mode is specified and the OIN bit has no meaning or effect. In this mode, the STAF flag is automatically set by detection of the selected edge on the STRA input pin indicating that new data is available in the port C latch. The

STAF flag is automatically cleared by a read of the PIOC register (with STAF set) followed by a read of the PORTCL latch register.

When HNDS is one and OIN is zero, the input handshake mode is specified. In this mode, the STAF flag is automatically set by detection of the selected edge on the STRA input pin indicating that new data is available in the port C latch. The STAF bit is automatically cleared by a read of the PIOC register (with STAF set) followed by a read of the PORTCL latch register.

When HNDS is one and OIN is one, the output handshake mode is specified. In this mode, the STAF flag is automatically set by detection of the selected edge on the STRA input pin indicating that data from port C has been accepted by the external system. The STAF flag is automatically cleared by a read of the PIOC register (with STAF set) followed by a write to the PORTCL latch register.

b6, STAI — The STAI (strobe A interrupt enable mask) bit is used to specify whether or not a hardware interrupt sequence is to be requested whenever STAF is set. To request a hardware interrupt, both the STAI interrupt enable bit and the STAF flag bit must be set. This bit is cleared by $\overline{\text{RESET}}$ so that parallel I/O interrupts are inhibited. The user must write this bit to a one in order to use the strobed and handshake I/O functions in an interrupt-driven, rather than a polled, environment.

b5, CWOM — When the CWOM (port C wire-OR mode) bit is zero, the port C output pins operate normally. When this bit is set to one, the port C outputs behave as open-drain type drivers allowing wired-OR type external connections. When CWOM equals one, the top driver device is disabled so that pins may be driven low by writing zeros or become three-state by writing ones. With an external pull-up resistor, the non-driven lines are pulled to logic ones.

This permits port C output pins to be safely wired in parallel with similar CMOS output drivers without fear of contentions which could otherwise cause destructive latch-up. This bit is cleared by $\overline{\text{RESET}}$ so port C pins which are configured as outputs will operate normally.

b4, HNDS — When HNDS (handshake mode) bit is clear, the STRA pin acts as a simple input strobe to latch incoming data into the PORTCL latch register and the STRB pin acts as a simple output strobe that pulses after any write to port B. When HNDS is set, it specifies that a handshake protocol involving port C, STRA, and STRB is in effect. In all modes, STRA is an edge-sensitive input and STRB is an output. This bit is cleared by $\overline{\text{RESET}}$. The strobe and handshake modes are described in greater detail in **I/O PORTS**.

b3, OIN — The OIN (output or input handshake) bit has no meaning or effect unless HNDS is set to one. When this bit is zero, input handshake protocol is specified. When this bit is a one, output handshake protocol is specified. See **I/O PORTS** for a more detailed description of the handshake protocols.

b2, PLS — The PLS (pulse/interlocked handshake) bit has no meaning or effect unless HNDS is set to one. When this bit is zero, interlocked handshake operation is specified. When this bit is one, pulse mode handshake operation is specified.

In interlocked modes, the STRB output line, once activated, remains active indefinitely until the selected edge is detected on the STRA input line. In pulse modes, the STRB output line, once activated, remains active for only two MCU E-clock cycles and then automatically reverts to the inactive state. This bit is cleared by $\overline{\text{RESET}}$. For more details on the handshake protocols, see **I/O PORTS**.

b1, EGA — The EGA (active edge for STRA) bit is used to specify which edge (rising or falling) on the STRA input pin is to be considered the active edge. When this bit is zero, the active edge is the falling edge and when this bit is one, the active edge is the rising edge. This bit is set to one by $\overline{\text{RESET}}$.

When output handshake mode is specified, this bit is used to control the PORTC three-state variation as well as select the active acknowledge edge. In the three-state variation, the EGA bit specifies the trailing edge polarity for the STRA input pin which is interpreted as the enable/acknowledge signal. Assertion of STRA overrides the DDRC specification to force port C to be outputs and the edge of negation is the active edge acknowledge command.

If EGA is zero, the falling edge at STRA is the active edge which causes STAF to be set and STRB to be negated. Additionally, if EGA is zero, port C bits obey the DDRC specification while STRA is low but port C is forced to be an output when STRA is high.

If EGA is one, the rising edge at STRA is the active edge. This causes STAF to be set and STRB to be negated. In addition, port C bits obey the DDRC specification while STRA is high, but port C is forced to be an output when STRA is low.

b0, INVB — The INVB (Invert Strobe B) bit is used to specify whether or not to invert the normal strobe B (STRB) logic output levels. When this bit is one, no inversion is specified and the active level on the strobe B output line is logic one. When this bit is zero, inversion is specified and the active level on the strobe B output line is logic zero. This bit is set to one by $\overline{\text{RESET}}$ so that the STRB output will initially be in the low state out of reset. For a more detailed description of the handshake protocols, see the **I/O PORTS** section.

PORT C DATA REGISTER (PORTC)

b7	b6	b5	b4	b3	b2	b1	b0	
PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	$xx03
0	0	0	0	0	0	0	0	RESET

Port C (PORTC) is a general purpose input/output port complemented by full handshake capability. For bits that are configured as inputs, reads of this address return the level sensed at the pin. For bits configured as outputs, reads return the level sensed at the input to the pin driver. When a port C pin is being used for the three-state variation of parallel output handshake, reads return the level sensed at the input to the pin driver even if the DDR bits suggest that the pin is configured as an input.

Writes to port C cause the value to be latched in the 8-bit port C data register. (Note that this is not the same register as the PORTCL latch register described later.) When the corresponding DDRC bit is set, the value in the port C data register is driven out of the port C pin. This data latch allows the programmer to initialize the data prior to turning on the output drivers by setting bits in the DDRC. The PORTC register is cleared by $\overline{\text{RESET}}$.

PORTB (PORT B DATA REGISTER)

b7	b6	b5	b4	b3	b2	b1	b0	
PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	$xx04
0	0	0	0	0	0	0	0	RESET

Port B (PORTB) is a general purpose output-only port. Reads of this address return the level sensed at the input to the pin driver. Writes to Port B cause the value to be latched in the 8-bit Port B data register. The PORTB register is set to zero by $\overline{\text{RESET}}$.

PORT C LATCHED DATA REGISTER (PORTCL)

b7	b6	b5	b4	b3	b2	b1	b0	
PCL7	PCL6	PCL5	PCL4	PCL3	PCL2	PCL1	PCL0	$xx05
U	U	U	U	U	U	U	U	RESET

The port C latch register (PORTCL) allows alternate access to port C information. This register is used in conjunction with the strobed parallel I/O modes. Input data is latched into the PORTCL register on each selected edge on the STRA pin. The latched data is the level at the pins regardless of the operating mode selected. Reads of PORTCL return the contents of the port C input latch. Reads also act as part of an automatic flag clearing sequence in the input handshake modes of port C.

Writes to the PORTCL register are equivalent to writes to the PORTC register except the PORTCL writes are used as part of an automatic flag clearing sequence in the output handshake modes of port C. For more information on the port C strobed and handshake modes, see **I/O PORTS**. The contents of PORTCL are not affected by $\overline{\text{RESET}}$.

DATA DIRECTION REGISTER C (DDRC)

b7	b6	b5	b4	b3	b2	b1	b0	
DDRC7	DDRC6	DDRC5	DDRC4	DDRC3	DDRC2	DDRC1	DDRC0	$xx07
0	0	0	0	0	0	0	0	RESET

The data direction register C (DDRC) is a read/write register used in conjunction with port C to specify the direction of data flow at each of the port C pins. A port C pin is an input if the corresponding bit in DDRC is zero. The pin is an output if the corresponding bit in DDRC is set to one. During reset, all bits in the DDRC are cleared to zero. The effects of DDRC are overridden in the three-state variation of the output handshake mode. For additional information, see **I/O PORTS, Output Handshake Protocol, Three-State Variation.**

HIGHEST PRIORITY INTERRUPT REGISTER (HPRIO)

b7	b6	b5	b4	b3	b2	b1	b0	
–	SMOD	–	IRV	–	–	–	–	$xx3C
0	–	0	–	0	0	0	0	RESET

NOTE

Reset condition of SMOD and IRV depend on initialization mode.

b7, b5, b3, b2, b1, b0—Not implemented

These bits are not implemented. Writes have no meaning or effect on them. Reads of these bits will always return a logic zero value.

b6, SMOD — The SMOD (Special Test Mode) bit is a read only bit which reflects the operating mode of the peripheral as selected by the MODE input. The inverted state of MODE is latched in SMOD by the rising edge of $\overline{\text{RESET}}$. When SMOD equals zero (MODE equals one), the peripheral is operating in normal mode. When SMOD equals one (MODE equals zero), the special test mode is selected.

The special test mode may be exited under software control by writing SMOD from a one to a zero. However,the special test mode may not be reentered by writing the bit back to one. This SMOD bit becomes write-protected once written to zero. This implies that the normal operating mode can be entered either through a hardware reset or through software while the special test mode may only be entered through a hardware reset.

b4, IRV

The IRV (Internal Read Visibility) control bit eliminates potential bus conflict problems when this device is used in conjunction with the MC68HC11. To allow a logic analyzer to monitor the internal bus activity of the MC68HC11, provisions have been made for the MPU to selectively drive the external data bus during internal reads as well as writes. The selection of this feature is controlled by the IRV bit.

The state following reset and the programming characteristics of the MC68HC24 IRV bit are the same as the MC68HC11 IRV bit. However, the functional characteristics are the opposite. The MC68HC24 IRV functions as follows:

Logic 0—Reads of the INIT and HPRIO registers will enable the multiplexed address/data buffers, placing the contents of the selected register on the bus.

Logic 1—Reads of the INIT and HPRIO registers do *not* enable the multiplexed address/data bus drivers.

This bit may be read at any time, although the multiplexed address/data bus will remain high-impedance during reads when IRV equals one. Only one write will be acknowledged and then only if SMOD equals one. The IRV bit is forced to zero (reads of HPRIO and INIT enabled) when SMOD is written from a one to a zero (entering normal mode). Reset clears this bit in the normal mode and sets this bit in the special test mode.

INIT (I/O MAPPING REGISTER)

b7	b6	b5	b4	b3	b2	b1	b0	
–	–	–	–	REG3	REG2	REG1	REG0	$xx3D
0	0	0	0	0	0	0	1	RESET

The INIT (I/O Mapping) register is a special purpose 8-bit register that is used (optionally) during initialization to change the default locations of the MC68HC24 internal registers in the MPU/MCU memory map. The lower four bits of the MC68HC24 INIT register are duplicates of the MC68HC11 INIT register. These four bits are used to specify the active state of the four high order address bits to the register address decoding logic. This register functions identically to the MC68HC11 INIT register with the following exceptions: 1) only the lower four bits are implemented, and 2) the protection mechanism is not time dependent.

The default starting address of the 64-byte internal register space is $1x00 (i.e., INIT is initialized to $01). Initialization software can move registers to any 4K boundary within the memory map. External decoding of A8 through A11 specifies where in the 4K block (on 256-byte boundaries) the 64-byte register space is located. As an example, assume that the initialization software wrote the value $09 to the INIT register and that $\overline{CS}$ was true when A8 through A11 were low. This would place the registers from $9000 through $903F in the memory map. Decoding A8 through A11 so that the chip is selected when all four address lines are low maps the MC68HC24 registers to the same address as the MC68HC11 registers.

The INIT register is special in that there is a write-protect mechanism associated with it. In the normal mode, the register may be written once at any time after reset. This *differs* from the operation of the MC68HC11 INIT register which becomes write protected after the first 64 E-clock cycles, whether or not a write to the register has occurred. After the first write, the MC68HC24 INIT register becomes write-protected and thereafter is a read-only register.

While in the special test mode (SMOD equals one), the protection mechanism is overridden and the INIT register may be written repeatedly as long as SMOD remains a one. When SMOD is written to a zero (to enter the normal operating mode), the write-protect mechanism is enabled. One additional write, regardless of the number of writes performed while in the special test mode, is allowed after entering normal operating mode. Writes to the upper four bits of the INIT register have no effect on the register contents and reads will always return zeros in the most significant bit positions.

SYSTEM CONFIGURATION

The MC68HC24 allows an end user to configure the peripheral to his specific MCU system through the use of hard wired options such as the mode select pin (MODE) and by the use of internal registers under software control. The following section describes those options which are fixed through hardware. Other configuration options, which can be changed dynamically, are discussed in the sections entitled **I/O PORTS** and **MODES OF OPERATION.**

MODE SELECTION

A dedicated mode select pin (MODE) determines which of two operating modes the MC68HC24 enters out of $\overline{RESET}$. Both modes properly emulate the action of Ports B and C of the MC68HC11. The modes are the normal and special test modes. Another dedicated pin (IOTEST) is used to test the output buffers.

The state of the mode select pin (MODE) is latched into the peripheral by the rising edge of $\overline{RESET}$ with the inverse of the latched value reflected in the SMOD bit of the HPRIO register. Normal mode is indicated by SMOD equals zero (MODE equals one). Special Test mode is indicated by SMOD equals one (MODE equals zero). The difference between these two modes is limited to the operation of the INIT and HPRIO registers.

The MODE input corresponds (in function, but not voltage levels) to the MODB/VPGM input of the MC68HC11. The MC68HC11 requires either V_{DD} or a level $1.8 \times V_{DD}$ on the MODB pin to select the operating mode; whereas, the MC68HC24 requires only logic level signals. The $1.8 \times V_{DD}$ level required by the MC68HC11 corresponds to a logic low on the MC68HC24. The V_{DD} level required by the MC68HC11 corresponds to a logic high on the MC68HC24. In normal operation, the special test mode is not used and the mode pin on both the MC68HC11 and the MC68HC24 can be tied to V_{DD}.

STATE AFTER RESET

When a low level is sensed on the $\overline{\text{RESET}}$ pin, the MC68HC24 enters the reset state. Most of the registers and control bits are forced to a specific state during reset and, if a user requires a different configuration, he must write the desired values into these registers in his initialization software. For detailed information about the options available, see **INTERNAL REGISTER DESCRIPTION**.

Note that $\overline{\text{RESET}}$ is synchronized to the system clock (E) before being used internally. For this reason, $\overline{\text{RESET}}$ must be held low for a minimum of two E-clock cycles to be recognized. Once recognized, the peripheral is initialized as described below.

Most of the configuration state after reset is independent of the selected operating mode. The STAF, STAI, and HNDS bits in the PIOC register are initialized to zeros so that no interrupt is pending or enabled and the simple strobed mode (rather than full handshake modes) of parallel I/O is selected. The CWOM bit is initialized to zero (Port C not operating in wired-OR mode). Port C is initialized as a general purpose, high-impedance input port (DDRC equals $00), STRA as an edge-sensitive strobe input, and the active edge is initially configured to detect rising edges (EGA bit set to one by $\overline{\text{RESET}}$). The STRB strobe output is initially a zero (INVB bit is initialized to one), while Port B is initialized with all outputs forced low.

The SMOD and IRV bits in the HPRIO register reflect the status of the MODE input at the rising edge of $\overline{\text{RESET}}$. Reset also deselects the chip and forces the multiplexed address/data bus to high impedance inputs.

MODES OF OPERATION

SPECIAL TEST MODE

The special test mode is selected with MODE equal to zero at the rising of edge of $\overline{\text{RESET}}$. Initialization into this mode loads HPRIO with $50 (SMOD and IRV equal one) and disables the INIT register write-protect mechanism.

While in special test mode (SMOD bit equals one), the INIT register write-protect mechanism is overridden and INIT remains writable as long as SMOD remains one. When SMOD is written to a zero (to enter the normal operating mode), the write-protect mechanism is enabled. One additional write is allowed after entering normal operating mode regardless of the number of writes perfomed while in the special test mode.

The reset state of IRV is one in the special test mode. An attempted read of either the INIT or HPRIO register with IRV equal to one will leave the data bus in a high impedance state with the output buffers disabled. If IRV equals zero, the data buffers are enabled and the contents of the selected register are placed on the data bus. The IRV bit is writable only one time while in the special test mode. Entering the normal mode forces the IRV bit to zero, enabling the data bus output buffers on reads of these two addresses. Table 1 summarizes the chip select options.

Table 1. MC68HC24 Chip Select Action Summary

$\overline{\text{CS}}$	IRV	Action Taken
0	0	Chip selected. HPRIO and INIT reads enabled.
0	1	Chip selected. HPRIO and INIT reads disabled.
1	X	Chip not selected.

NORMAL MODE

Normal mode is selected when the MODE input is at a logic high level at the rising edge of $\overline{\text{RESET}}$. The HPRIO register is initialized to $00 (SMOD and IRV equal zero). The INIT register write-protect mechanism is enabled, allowing only a single write to INIT. Reads of both the INIT and HPRIO register enable the output buffers, thus providing visibility into the contents of these registers. The HPRIO register is write-protected while in the normal mode. A reset sequence must be initiated to change the contents of this register.

NOTE

A write to the INIT register must be included in the initialization software whether or not the registers are to be relocated. This write will ensure that an accidental write to register at a later time will not cause the registers to be remapped. THIS IS ONE OF THE FUNCTIONAL DIFFERENCES BETWEEN THE MC68HC11 PORTS AND THE MC68HC24 IMPLEMENTATION.

MC68HC11 AND MC68HC24 OPERATIONAL DIFFERENCES

INIT REGISTER WRITE-PROTECT MECHANISM

The MC68HC11 INIT register write-protect mechanism automatically disables writes to the INIT register 64 E clock cycles after the rising edge of $\overline{\text{RESET}}$. The MC68HC24 write-protect circuitry IS NOT TIME DEPENDENT. Only a write to the INIT register will disable further writes. Both the MC68HC11 and MC68HC24 INIT registers can be written repeatedly in the special test mode of operation (see **SPECIAL TEST MODE**) or once in the normal mode.

This difference dictates that the user should not rely on the timeout feature of the MC68HC11 to write-protect the INIT register if he plans to utilize the same software with the MC68HC24. Instead, a write to the INIT register should be done during initialization, even if the remapping feature is not going to be used.

STRA PULSE WIDTH

Due to differences in implementation technology, the MC68HC24 incorporates an additional level of synchronization (over the MC68HC11) on the STRA input. Under normal operating conditions, the end user will be unaware of this anomaly. Only systems which continually strobe new data into PORTCL are affected.

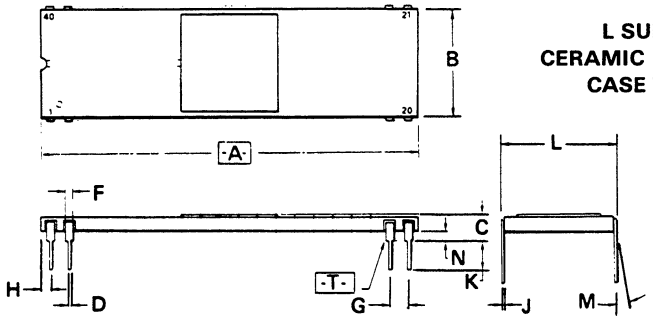
In order to allow the STRA signal to propagate through the internal feedback mechanism, a minimum delay of two E clock cycles between active edges has been specified. This delay should not concern most users, since the time required to acknowledge the receipt of data and to read the data is much greater that two cycles.

STRB SYNCHRONIZATION

The MC68HC11 synchronizes changes of port B, port C, and STRB data to an internal quadrature clock. This method of implementation makes internal buffer delays transparent to the end user. This internal clock is generated from the 4X clock, and as a result, cannot be duplicated by the MC68HC24. Port B and port C data are synchronized to the E clock and become valid t_{PWD} *after* the falling edge of E instead of a setup time before the falling edge of E.

The most noticeable change involves STRB. The STRB signal is synchronized to the rising edge of E instead of the quadrature clock as in the MC68HC11. At slow clock rates (much less than 1 MHz), the delay between valid data on the port pins and the assertion of STRB could be considerable.

PACKAGE DIMENSIONS



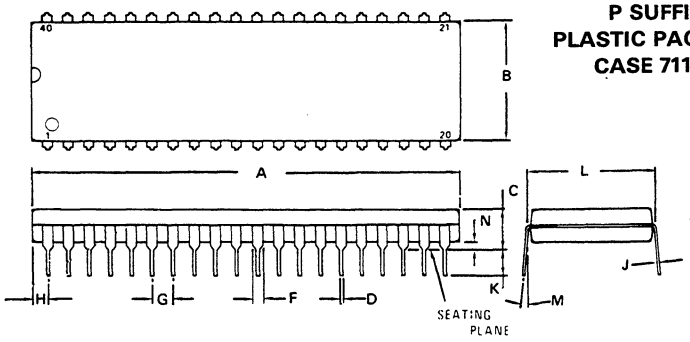
L SUFFIX
CERAMIC PACKAGE
CASE 715-05

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	50.29	51.31	1.980	2.020
B	14.63	15.49	0.576	0.610
C	2.79	4.32	0.110	0.170
D	0.38	0.53	0.015	0.021
F	0.76	1.52	0.030	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.33	0.008	0.013
K	2.54	4.57	0.100	0.180
L	14.99	15.65	0.590	0.616
M	–	10°	–	10°
N	1.02	1.52	0.040	0.060

NOTES:
1. DIMENSION -A- IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS:

   ⌖ 0.25 (0.010) Ⓜ T A Ⓜ

3. -T- IS SEATING PLANE.
4. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

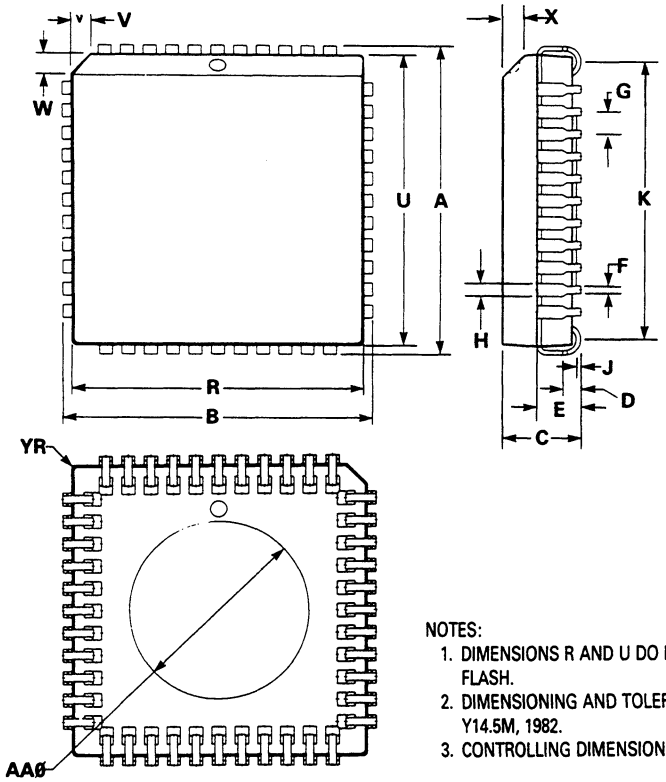


P SUFFIX
PLASTIC PACKAGE
CASE 711-03

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0 015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0^0	15^0	0^0	15^0
N	0.51	1.02	0.020	0.040

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

SUFFIX
PCC QUAD PACKAGE
CASE 777A-01



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	17.40	17.65	0.685	0.695
B	17.40	17.65	0.685	0.695
C	4.19	4.57	0.165	0.180
D	0.64	1.01	0.025	0.040
E	2.16	2.79	0.085	0.110
F	0.33	0.53	0.013	0.021
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.13	0.38	0.005	0.015
K	14.99	16.00	0.590	0.630
R	16.51	16.66	0.650	0.656
U	16.51	16.66	0.650	0.656
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.046
Y	0.00	0.50	0.000	0.020
AA	9.86	10.33	0.388	0.407

NOTES:
1. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: INCH

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MC68HC24/D

A18615-2 PRINTED IN USA (1994) MPS/POD