LTC1597

16-Bit Parallel, Low Glitch Multiplying DAC with 4-Quadrant Resistors

September 1998

FEATURES

- **True 16-Bit Performance over Industrial Temperature Range**
- **DNL and INL: 1LSB Max**
- **On-Chip 4-Quadrant Resistors Allow Precise 0V to 10V, 0V to –10V or ±10V Outputs**
- **Asynchronous Clear Pin**
  - **LTC1597: Reset to Zero Scale**
  - **LTC1597-1: Reset to Midscale**
- **Glitch Impulse < 2nV-s**
- 28-Lead SSOP Package
- Low Power Consumption: 10µW Typ
- Power-On Reset

APPLICATIONS

- Process Control and Industrial Automation
- Direct Digital Waveform Generation
- Software-Controlled Gain Adjustment
- Automatic Test Equipment

DESCRIPTION

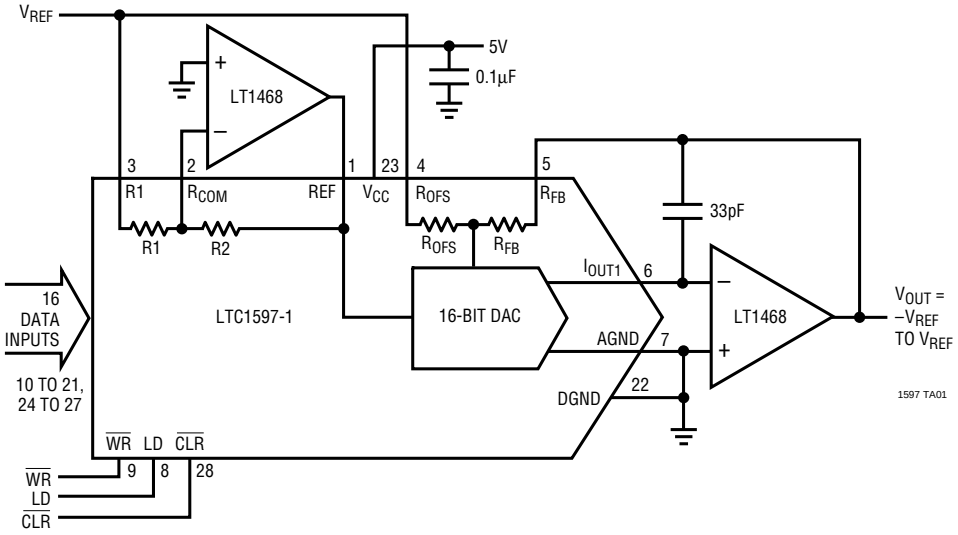
The LTC®1597 is a parallel input 16-Bit multiplying current output DAC that operates from a single 5V supply. INL and DNL are accurate to 1LSB over the industrial temperature range in both 2- and 4-quadrant multiplying modes. True 16-bit 4-quadrant multiplication is achieved with on-chip 4-quadrant multiplication resistors.

The LTC1597 is available in 28-pin SSOP package and is specified over the commercial and industrial temperature ranges. The device includes an internal deglitcher circuit that reduces the glitch impulse to less than 2nV-s (typ). The asynchronous $\overline{CLR}$ pin resets the LTC1597 to zero scale and the LTC1597-1 to midscale.

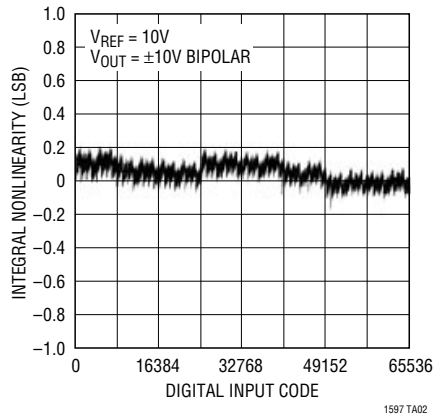
For serial interface 16-bit current output DACs refer to the LTC1595/LTC1596 data sheet.

TYPICAL APPLICATION

16-Bit, 4-Quadrant Multiplying DAC with a Minimum of External Components



LTC1597/LTC1597-1
Integral Nonlinearity

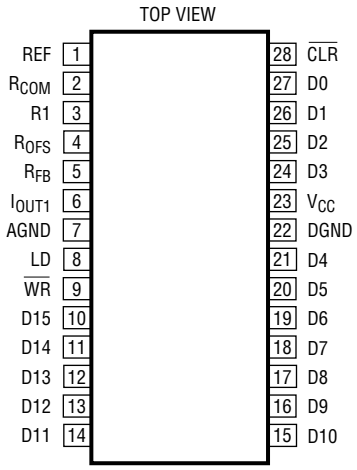


ABSOLUTE MAXIMUM RATINGS

(Note 13)

V_{CC} to AGND ..... –0.5V to 7V
V_{CC} to DGND ..... –0.5V to 7V
AGND to DGND ..... V_{CC} + 0.5V
DGND to AGND ..... V_{CC} + 0.5V
REF, R_{OFS}, R_{FB}, R1, R_{COM} to AGND, DGND ..... ±25V
Digital Inputs to DGND ..... –0.5V to (V_{CC} + 0.5V)
I_{OUT1} to AGND ..... –0.5V to(V_{CC} + 0.5V)
Maximum Junction Temperature ..... 125°C
Operating Temperature Range
LTC1597/LTC1597-1C ..... 0°C to 70°C
LTC1597/LTC1597-1I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
28-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 95°C/W

ORDER PART NUMBER
LTC1597ACG
LTC1597BCG
LTC1597AIG
LTC1597BIG
LTC1597-1ACG
LTC1597-1BCG
LTC1597-1AIG
LTC1597-1BIG

Consult factory for Military grade and PDIP parts.

ELECTRICAL CHARACTERISTICS

V_{DD} = 5V ±10%, V_{REF} = 10V, I_{OUT1} = AGND = DGND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1597A/LTC1597-1A MIN	TYP	MAX	LTC1597B/LTC1597-1B MIN	TYP	MAX	UNITS
Accuracy										
	Resolution		●	16			16			Bits
	Monotonicity		●	16			16			Bits
INL	Integral Nonlinearity	(Note 1) T_A = 25°C			±0.25	±1			±2	LSB
		T_{MIN} to T_{MAX}	●		±0.35	±1			±2	LSB
DNL	Differential Nonlinearity	T_A = 25°C			±0.2	±1			±1	LSB
		T_{MIN} to T_{MAX}	●		±0.2	±1			±1	LSB
GE	Gain Error	Unipolar Mode								
		(Note 2) T_A = 25°C			2	±16			±16	LSB
		T_{MIN} to T_{MAX}	●		3	±16			±24	LSB
		Bipolar Mode								
		(Note 2) T_A = 25°C			2	±16			±16	LSB
		T_{MIN} to T_{MAX}	●		3	±16			±24	LSB
	Gain Temperature Coefficient	(Note 3) ΔGain/ΔTemperature	●		1	2		1	2	ppm/°C
	Bipolar Zero Error	T_A = 25°C				±5			±10	LSB
		T_{MIN} to T_{MAX}	●			±8			±16	LSB
I_{LKG}	OUT1 Leakage Current	(Note 4) T_A = 25°C				±5			±5	nA
		T_{MIN} to T_{MAX}	●			±15			±15	nA
PSRR	Power Supply Rejection	V_{CC} = 5V ±10%	●		±1	±2		±1	±2	LSB/V

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, V_{REF} = 10V, I_{OUT1} = AGND = DGND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Input							
R_{REF}	DAC Input Resistance (Unipolar)	(Note 5)	●	4.5	6	10	kΩ
R1/R2	R1/R2 Resistance (Bipolar)	(Notes 5, 12)	●	9	12	20	kΩ
R_{OFS}, R_{FB}	Feedback and Offset Resistances	(Note 5)	●	9	12	20	kΩ
AC Performance (Note 3)							
	Output Current Settling Time	(Notes 6, 7)			1		µs
	Midscale Glitch Impulse	(Note 11)			2		nV-s
	Digital-to-Analog Glitch Impulse	(Note 8)			1		nV-s
	Multiplying Feedthrough Error	V_{REF} = ±10V, 10kHz Sine Wave			1		mV_{P-P}
THD	Total Harmonic Distortion	(Note 9)			108		dB
	Output Noise Voltage Density	(Note 10)			10		$nV/\sqrt{Hz}$
Analog Outputs (Note 3)							
C_{OUT}	Output Capacitance (Note 3)	DAC Register Loaded to All 1s: C_{OUT1} DAC Register Loaded to All 0s: C_{OUT1}	● ●		115 70	130 80	pF pF
Digital Inputs							
V_{IH}	Digital Input High Voltage		●	2.4			V
V_{IL}	Digital Input Low Voltage		●			0.8	V
I_{IN}	Digital Input Current		●		0.001	±1	µA
C_{IN}	Digital Input Capacitance	(Note 3) V_{IN} = 0V	●			8	pF
Timing Characteristics							
t_{DS}	Data to $\overline{WR}$ Setup Time		●	60	20		ns
t_{DH}	Data to $\overline{WR}$ Hold Time		●	0	–12		ns
t_{WR}	$\overline{WR}$ Pulse Width		●	60	25		ns
t_{LD}	LD Pulse Width		●	110	55		ns
t_{CLR}	Clear Pulse Width		●	60	40		ns
t_{LWD}	$\overline{WR}$ to LD Delay Time		●	0			ns
Power Supply							
V_{DD}	Supply Voltage		●	4.5	5	5.5	V
I_{DD}	Supply Current	Digital Inputs = 0V or V_{CC}	●			10	µA

The ● denotes specifications that apply over the full operating temperature range.

Note 1: ±1LSB = ±0.0015% of full scale = ±15.3ppm of full scale.

Note 2: Using internal feedback resistor.

Note 3: Guaranteed by design, not subject to test.

Note 4: $I_{(OUT1)}$ with DAC register loaded to all 0s.

Note 5: Typical temperature coefficient is 100ppm/°C.

Note 6: I_{OUT1} load = 100Ω in parallel with 13pF.

Note 7: To 0.0015% for a full-scale change, measured from the rising edge of LD.

Note 8: V_{REF} = 0V. DAC register contents changed from all 0s to all 1s or all 1s to all 0s.

Note 9: V_{REF} = $6V_{RMS}$ at 1kHz. DAC register loaded with all 1s.

Note 10: Calculation from $e_n = \sqrt{4kTRB}$ where: k = Boltzmann constant (J/°K), R = resistance (Ω), T = temperature (°K), B = bandwidth (Hz).

Note 11: Midscale transition code 0111 1111 1111 1111 to 1000 0000 0000 0000.

Note 12: R1 and R2 are measured between R1 and R_{COM}, REF and R_{COM}.

Note 13: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

PIN FUNCTIONS

REF (Pin 1): Reference Input and 4-Quadrant Resistor R2. Typically ±10V, accepts up to ±25V. 2-Quadrant mode reference input. 4-quadrant mode, driven by external inverting reference amplifier.

R_{COM} (Pin 2): Center Tap Point of the Two 4-Quadrant Resistors R1 and R2. Normally tied to the inverting input of an external amplifier in 4-quadrant operation, otherwise shorted to the REF pin. See Figures 1 and 2.

R1 (Pin 3): 4-Quadrant Resistor R1. In 2-quadrant operation short to the REF pin. In 4-quadrant mode tie to the reference input.

R_{OFS} (Pin 4): Bipolar Offset Resistor. Typically swings ±10V, accepts up to ±25V. 2-quadrant operation tie to R_{FB}. 4-quadrant operation tie to R1.

R_{FB} (Pin 5): Feedback Resistor. Normally tied to the output of the current to voltage converter op amp. Typically swings ±10V. Swings $\pm V_{REF}$.

I_{OUT1} (Pin 6): DAC Current Output. Tie to the inverting input of the current to voltage converter op amp.

AGND (Pin 7): Analog Ground. Tie to ground.

LD (Pin 8): DAC Digital Input Load Control Input. When LD is taken to a logic high, data is loaded from the input register into the DAC register, updating the DAC output.

$\overline{WR}$ (Pin 9):DAC Digital Write Control Input. When $\overline{WR}$ is taken to a logic low, data is loaded from the digital input pins into the 16-bit wide input register.

D15 to D4 (Pins 10 to 21): Digital Input Data Bits.

DGND (Pin 22): Digital Ground. Tie to ground.

V_{CC} (Pin 23): The Positive Supply Input. $4.5V \leq V_{CC} \leq 5.5V$. Requires a bypass capacitor to ground.

D3 to D0 (Pins 24 to 27): Digital Input Data Bits.

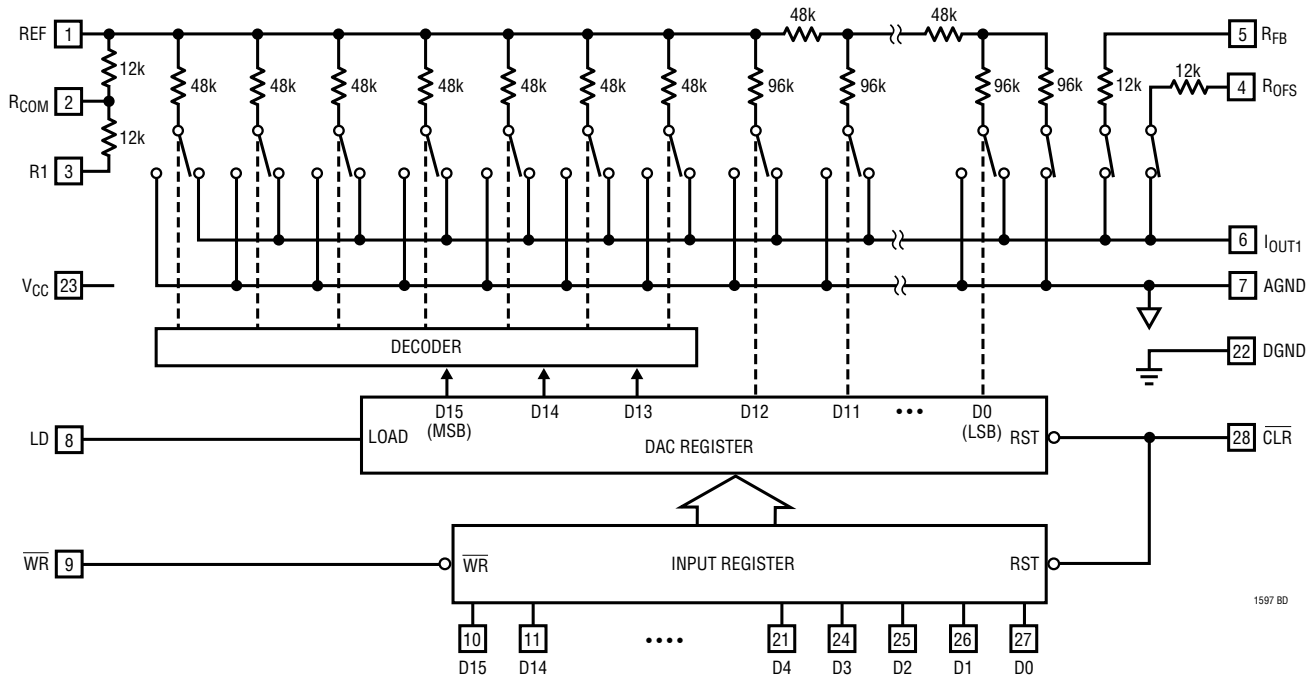
$\overline{CLR}$ (Pin 28): Digital Clear Control Function for the DAC. When $\overline{CLR}$ is taken to a logic low, it sets the DAC output and all internal registers to zero code for the LTC1597 and midscale code for the LTC1597-1.

TRUTH TABLE

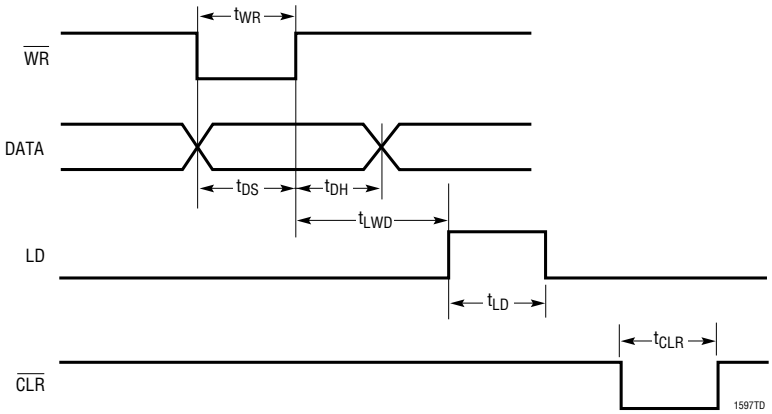
Table 1

CONTROL INPUTS			
$\overline{CLR}$	$\overline{WR}$	LD	REGISTER OPERATION
0	X	X	Reset Input and DAC Register to All 0s for LTC1597 and midscale for LTC1597-1 (Asynchronous Operation)
1	0	0	Load Input Register with All 16 Data Bits
1	1	1	Load DAC Register with the Contents of the Input Register
1	0	1	Input and DAC Register Are Transparent
1	↓↑	↓↑	CLK = LD and $\overline{WR}$ Tied Together. The 16 Data Bits Are Loaded into the Input Register on the Falling Edge of the CLK and Then Loaded into the DAC Register on the Rising Edge of the CLK
1	1	0	No Register Operation

BLOCK DIAGRAM



TIMING DIAGRAM



APPLICATIONS INFORMATION

Description

The LTC1597 is a 16-bit multiplying, current output DAC with a full parallel 16-bit digital interface. The device operates from a single 5V supply and provides both unipolar 0V to –10V or 0V to 10V and bipolar ±10V output ranges from a 10V or –10V reference input. It has three additional precision resistors on chip for bipolar operation. Refer to the block diagram regarding the following description.

The 16-bit DAC consists of a precision R-2R ladder for the 13LSBs. The 3MSBs are decoded into seven segments of resistor value R. Each of these segments and the R-2R ladder carries an equally weighted current of one eighth of full scale. The feedback resistor R_{FB} and 4-quadrant

APPLICATIONS INFORMATION

resistor R_{OFS} have a value of R/4. 4-quadrant resistors R1 and R2 have a magnitude of R/4. R1 and R2 together with an external op amp (see Figure 2) inverts the reference input voltage and applies it to the 16-bit DAC input REF, in 4-quadrant operation. The REF pin presents a constant input impedance of R/8 in unipolar mode and R/12 in bipolar mode. The output impedance of the current output pin I_{OUT1} varies with DAC input code. The I_{OUT1} capacitance due to the NMOS current steering switches also varies with input code from 70pF to 115pF. An added feature of the LTC1597, especially for waveform generation, is a proprietary deglitcher that reduces glitch energy to below 2nV-s over the DAC output voltage range.

Digital Section

The LTC1597 has a 16-bit wide, full parallel data input bus. The device is double-buffered with two 16-bit registers. The double-buffered feature permits the update of several DACs simultaneously. The input register is loaded directly from a 16-bit microprocessor bus when the $\overline{WR}$ pin is brought to a logic low level. The second register (DAC register) is updated with the data from the input register when the LD pin is brought to a logic high level. Updating the DAC register updates the DAC output with the new data. To make both registers transparent for flowthrough mode, tie $\overline{WR}$ low and LD high. However, this defeats the deglitcher operation and output glitch impulse may increase. The deglitcher is activated on the rising edge of the LD pin. The versatility of the interface also allows the use of the input and DAC registers in a master slave or edge-triggered configuration. This mode of operation occurs when $\overline{WR}$ and LD are tied together. The asynchronous clear pin resets the LTC1597 to zero scale and the LTC1597-1 to midscale. $\overline{CLR}$ resets both the input and DAC registers. The device also has a power-on reset. Table 1 shows the truth table for the device.

Unipolar Mode
(2-Quadrant Multiplying, V_{OUT} = 0V to $-V_{REF}$)

The LTC1597 can be used with a single op amp to provide 2-quadrant multiplying operation as shown in Figure 1. With a fixed –10V reference, the circuit shown gives a precision unipolar 0V to 10V output swing.

Bipolar Mode
(4-Quadrant Multiplying, $V_{OUT} = -V_{REF}$ to V_{REF})

The LTC1597 contains on chip all the 4-quadrant resistors necessary for bipolar operation. 4-quadrant multiplying operation can be achieved with a minimum of external components, a capacitor and a dual op amp, as shown in Figure 2. With a fixed 10V reference, the circuit shown gives a precision bipolar –10V to 10V output swing.

Op Amp Selection

Because of the extremely high accuracy of the 16-bit LTC1597, thought should be given to op amp selection in order to achieve the exceptional performance of which the part is capable. Fortunately, the sensitivity of INL and DNL to op amp offset has been greatly reduced compared to previous generations of multiplying DACs.

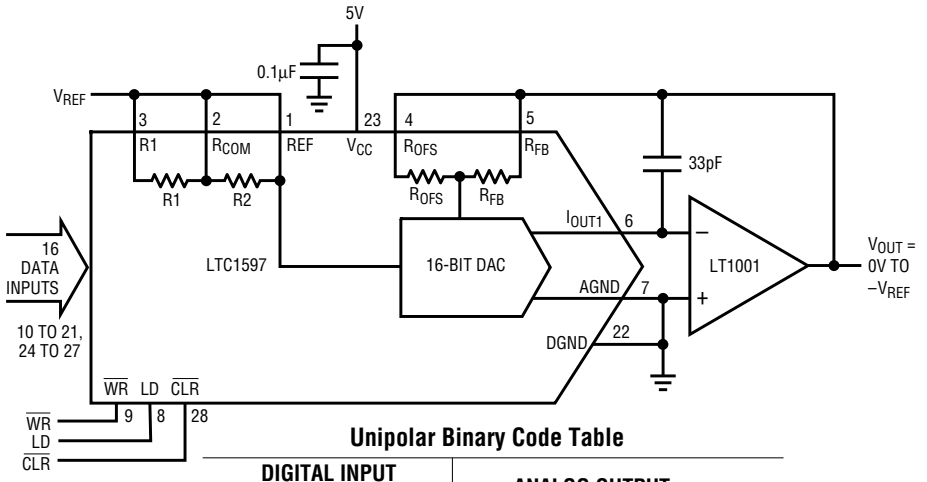
Op amp offset will contribute mostly to output offset and gain and will have minimal effect on INL and DNL. For the LTC1597, a 500μV op amp offset will cause about 0.55LSB INL degradation and 0.15LSB DNL degradation with a 10V full-scale range. The main effects of op amp offset will be a degradation of zero-scale error equal to the op amp offset, and a degradation of full-scale error equal to twice the op amp offset. For the LTC1597, the same 500μV op amp offset will cause a 3.3LSB zero-scale error and a 6.5LSB full-scale error with a 10V full-scale range.

Op amp input bias current (I_{BIAS}) contributes only a zero-scale error equal to $I_{BIAS}(R_{FB}//R_{OFS}) = I_{BIAS}(6k)$. For a thorough discussion of 16-bit DAC settling time and op amp selection, refer to Application Note 74,"*Component and Measurement Advances Ensure 16-Bit DAC Settling Time*."

Grounding

As with any high resolution converter, clean grounding is important. A low impedance analog ground plane and star grounding should be used. AGND must be tied to the star ground with as low a resistance as possible.

APPLICATIONS INFORMATION

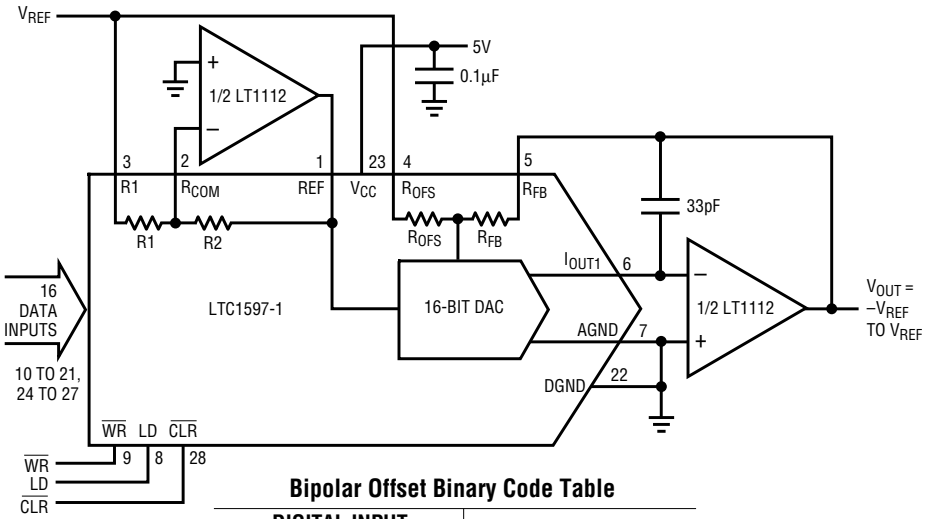


Unipolar Binary Code Table

DIGITAL INPUT BINARY NUMBER IN DAC REGISTER	ANALOG OUTPUT V_{OUT}
MSB LSB	
1111 1111 1111 1111	$-V_{REF}$ (65,535/65,536)
1000 0000 0000 0000	$-V_{REF}$ (32,768/65,536) = $-V_{REF}/2$
0000 0000 0000 0001	$-V_{REF}$ (1/65,536)
0000 0000 0000 0000	0V

1597 F01

Figure 1. Unipolar Operation (2-Quadrant Multiplication) V_{OUT} = 0V to $-V_{REF}$



Bipolar Offset Binary Code Table

DIGITAL INPUT BINARY NUMBER IN DAC REGISTER	ANALOG OUTPUT V_{OUT}
MSB LSB	
1111 1111 1111 1111	V_{REF} (32,767/32,768)
1000 0000 0000 0001	V_{REF} (1/32,768)
1000 0000 0000 0000	0V
0111 1111 1111 1111	$-V_{REF}$ (1/32,768)
0000 0000 0000 0000	$-V_{REF}$

1597 F02

Figure 2. Bipolar Operation (4-Quadrant Multiplication) $V_{OUT} = -V_{REF}$ to V_{REF}

TYPICAL APPLICATION

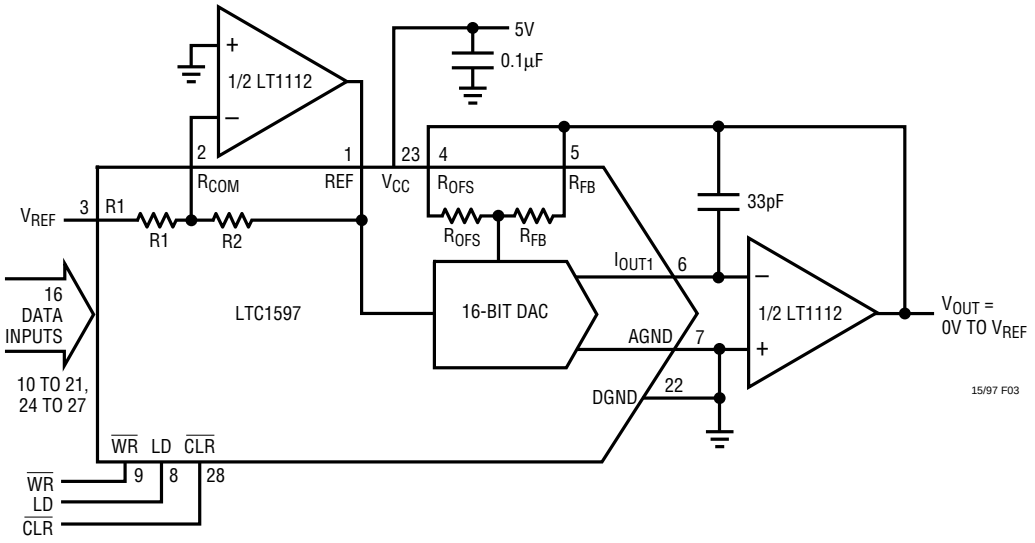
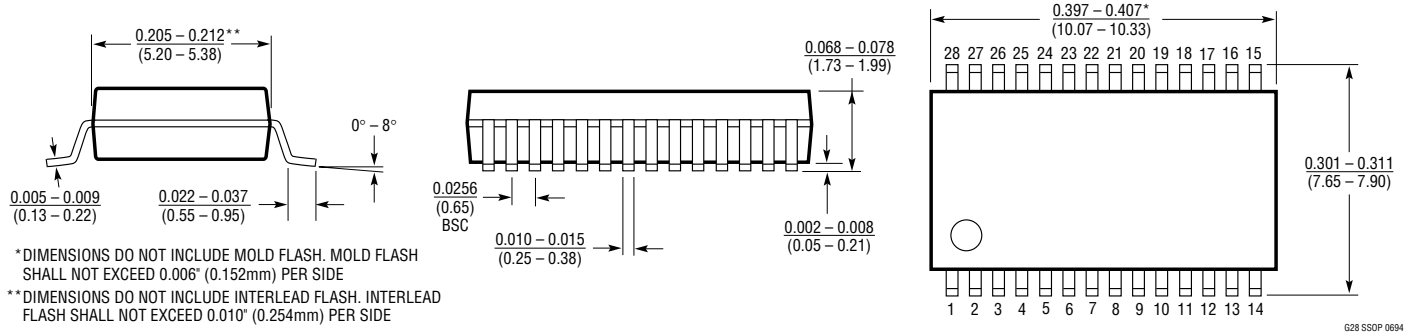


Figure 3. Noninverting Unipolar Operation (2-Quadrant Multiplication) V_{OUT} = 0V to V_{REF}

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

G Package
28-Lead Plastic SSOP (0.209)
(LTC DWG # 05-08-1640)



*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1001	Precision Operational Amplifier	Low Offset, Low Drift
LT1112	Dual Low Power, Precision Picoamp Input Op Amp	Low Offset, Low Drift
LT1468	90MHz, 22V/µs, 16-Bit Accurate Op Amp	Precise, 1µs Settling to 0.0015%
LTC1595/LTC1596	Serial 16-Bit Current Output DACs	Low Glitch, ±1LSB Maximum INL, DNL

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