Integrated Circuit Systems, Inc.

# ICS9DB206

## PCI EXPRESS™ JITTER ATTENUATOR

## GENERAL DESCRIPTION

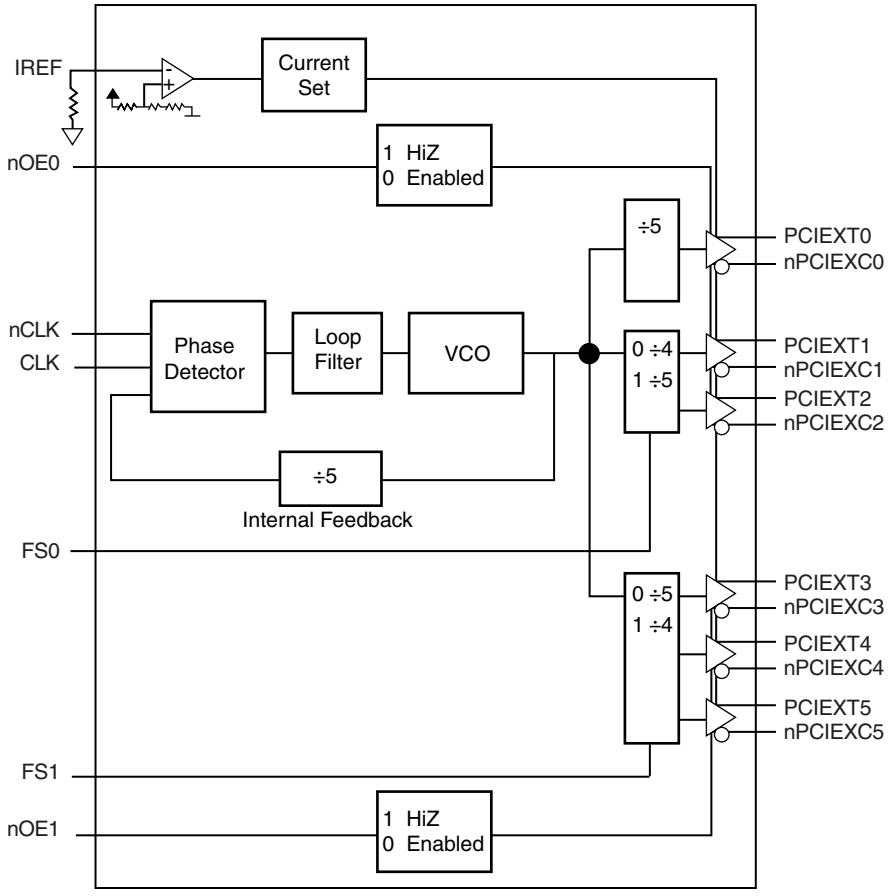
The ICS9DB206 is a high perfromance 1-to-6 Differential-to-HCSL Jitter Attenuator designed for use in PCI Express™ systems. In some PCI Express™ systems, such as those found in desktop PCs, the PCI Express™ clocks are generated from a low bandwidth, high phase noise PLL frequency synthesizer. In these systems, a jitter-attenuating device may be necessary in order to reduce high frequency random and deterministic jitter components from the PLL synthesizer and from the system board. The ICS9DB206 has two PLL bandwidth modes. In low bandwidth mode, the PLL loop bandwidth is 500kHz. This setting offers the best jitter attenuation and is still high enough to pass a triangular input spread spectrum profile. In high bandwidth mode, the PLL bandwidth is at 1MHz and allows the PLL to pass more spread spectrum modulation.

For serdes which have x10 reference multipliers instead of x12.5 multipliers, 5 of the 6 PCI Express™ outputs (PCIEX1:5) can be set for 125MHz instead of 100MHz by configuring the appropriate frequency select pins (FS0:1). Output PCIEX0 will always run at the reference clock frequency (usually 100MHz) in desktop PC PCI Express™ Applications.

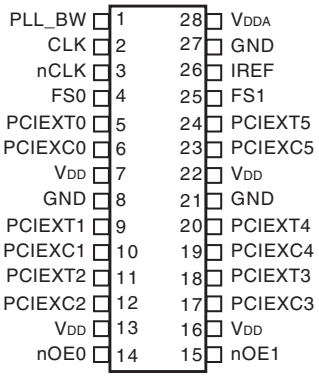
## Features

- Six 0.7V current mode differential HCSL output pairs
- 1 differential clock input
- CLK and nCLK supports the following input types: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Maximum output frequency: 140MHz
- Output skew: 110ps (maximum)
- Cycle-to-Cycle jitter: 110ps (maximum)
- RMS phase jitter @ 100MHz, (1.5MHz - 22MHz): 2.42ps (typical)
- 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request
- Lead-Free package fully RoHS compliant

## BLOCK DIAGRAM




## PIN ASSIGNMENT




**ICS9DB206**
**28-Lead TSSOP, 173-MIL**
4.4mm x 9.7mm x 0.92mm body package
**L Package**
Top View

**ICS9DB206**
**28-Lead, 209-MIL SSOP**
5.3mm x 10.2mm x 1.75mm body package
**F Package**
Top View

**TABLE 1. PIN DESCRIPTIONS**

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1 | PLL_BW | Input | Pullup | Selects PLL Bandwidth input. LVCMOS/LVTTL interface levels. |
| 2 | CLK | Input | Pulldown | Non-inverting differential clock input. |
| 3 | nCLK | Input | Pullup/ Pulldown | Inverting differential clock input. $V_{DD}/2$ default when left floating. |
| 4 | FS0 | Input | Pullup | Frequency select pin. LVCMOS/LVTTL interface levels. |
| 5, 6 | PCIEXT0, PCIEXC0 | Output | | Differential output pairs. HCSL interface levels. |
| 7, 13, 16, 22 | $V_{DD}$ | Power | | Core supply pins. |
| 8, 21 | GND | Power | | Power supply ground. |
| 9, 10 | PCIEXT1, PCIEXC1 | Output | | Differential output pairs. HCSL interface levels. |
| 11, 12 | PCIEXT2, PCIEXC2 | Output | | Differential output pairs. HCSL interface levels. |
| 14, 15 | nOE0, nOE1 | Input | Pulldown | Output enable. When HIGH, forces outputs to HiZ state. When LOW, enables outputs. LVCMOS/LVTTL interface levels. |
| 17, 18 | PCIEXC3, PCIEXT3 | Output | | Differential output pairs. HCSL interface levels. |
| 19, 20 | PCIEXC4, PCIEXT4 | Output | | Differential output pairs. HCSL interface levels. |
| 23, 24 | PCIEXC5, PCIEXT5 | Output | | Differential output pairs. HCSL interface levels. |
| 25 | FS1 | Input | Pulldown | Frequency select pin. LVCMOS/LVTTL interface levels. |
| 26 | IREF | Input | | A fixed precision resistor (475Ω) from this pin to ground provides a reference current used for differential current-mode PCIEX clock outputs. |
| 27 | GND | Power | | Power supply ground. |
| 28 | $V_{DDA}$ | Power | | Analog supply pin. Requires 24Ω series resistor. |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | 4 | | pF |
| $R_{PULLUP}$ | Input Pullup Resistor | | | 51 | | kΩ |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | 51 | | kΩ |

**TABLE 3A. RATIO OF OUTPUT FREQUENCY TO INPUT FREQUENCY FUNCTION TABLE, FS0**

| Inputs | Outputs | | |
|---|---|---|---|
| FS0 | PCIEX0 | PCIEX1 | PCIEX2 |
| 0 | 1 | 5/4 | 5/4 |
| 1 | 1 | 1 | 1 |

**TABLE 3B. RATIO OF OUTPUT FREQUENCY TO INPUT FREQUENCY FUNCTION TABLE, FS1**

| Inputs | Outputs | | |
|---|---|---|---|
| FS1 | PCIEX3 | PCIEX4 | PCIEX5 |
| 0 | 1 | 1 | 1 |
| 1 | 5/4 | 5/4 | 5/4 |

**TABLE 3C. OUTPUT ENABLE FUNCTION TABLE, nOE0**

| Inputs | Outputs |
|---|---|
| nOE0 | PCIEX0:2 |
| 0 | Enabled |
| 1 | HiZ |

**TABLE 3D. OUTPUT ENABLE FUNCTION TABLE, nOE1**

| Inputs | Outputs |
|---|---|
| nOE1 | PCIEX3:5 |
| 0 | Enabled |
| 1 | HiZ |

**TABLE 3E. PLL BANDWIDTH TABLE**

| Inputs | Bandwidth |
|---|---|
| PLL_BW | |
| 0 | 500kHz |
| 1 | 1MHz |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage, $V_{DD}$ | 4.6V |
| Inputs, $V_I$ | -0.5V to $V_{DD}$ + 0.5 V |
| Outputs, $V_O$ | -0.5V to $V_{DD}$ + 0.5V |
| Package Thermal Impedance, $\theta_{JA}$ | |
| 28 Lead TSSOP | 49.8°C/W (0 lfpm) |
| 28 Lead SSOP | 49°C/W (0 lfpm) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,** $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $T_A$ = 0°C TO 70°C, RREF = 475Ω

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{DDA}$ | Analog Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $I_{DD}$ | Power Supply Current | | | | 112 | mA |
| $I_{DDA}$ | Analog Supply Current | | | | 22 | mA |

**TABLE 4B. LVCMOS / LVTTL DC CHARACTERISTICS,** $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $T_A$ = 0°C TO 70°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | | 2 | | $V_{DD}$ + 0.3 | mV |
| $V_{IL}$ | Input Low Voltage | | | -0.3 | | 0.8 | mV |
| $I_{IH}$ | Input High Current | FS1, nOE0, nOE1 | $V_{DD} = V_{IN} = 3.465V$ | | | 150 | µA |
| | | FS0, PLL_BW | | | | 5 | µA |
| $I_{IL}$ | Input Low Current | FS1, nOE0, nOE1 | $V_{DD} = 3.465V$, $V_{IN} = 0V$ | -5 | | | µA |
| | | FS0, PLL_BW | | -150 | | | µA |

**TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS,** $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $T_A$ = 0°C TO 70°C, RREF = 475Ω

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $I_{IH}$ | Input High Current | CLK, nCLK | $V_{DD} = V_{IN} = 3.465V$ | | | 150 | µA |
| $I_{IL}$ | Input Low Current | CLK, nCLK | $V_{DD} = 3.465V$, $V_{IN} = 0V$ | | | 150 | µA |
| $V_{PP}$ | Peak-to-Peak Input Voltage | | | 0.15 | | 1.3 | V |
| $V_{CMR}$ | Common Mode Input Voltage; NOTE 1, 2 | | | GND + 0.5 | | $V_{DD}$ - 0.85 | V |

NOTE 1: Common mode voltage is defined as $V_{IH}$.
NOTE 2: For single ended applications, the maximum input voltage for CLK, nCLK is $V_{DD}$ + 0.3V.

**TABLE 4D. HCSL DC CHARACTERISTICS,** $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $T_A$ = 0°C TO 70°C, RREF = 475Ω

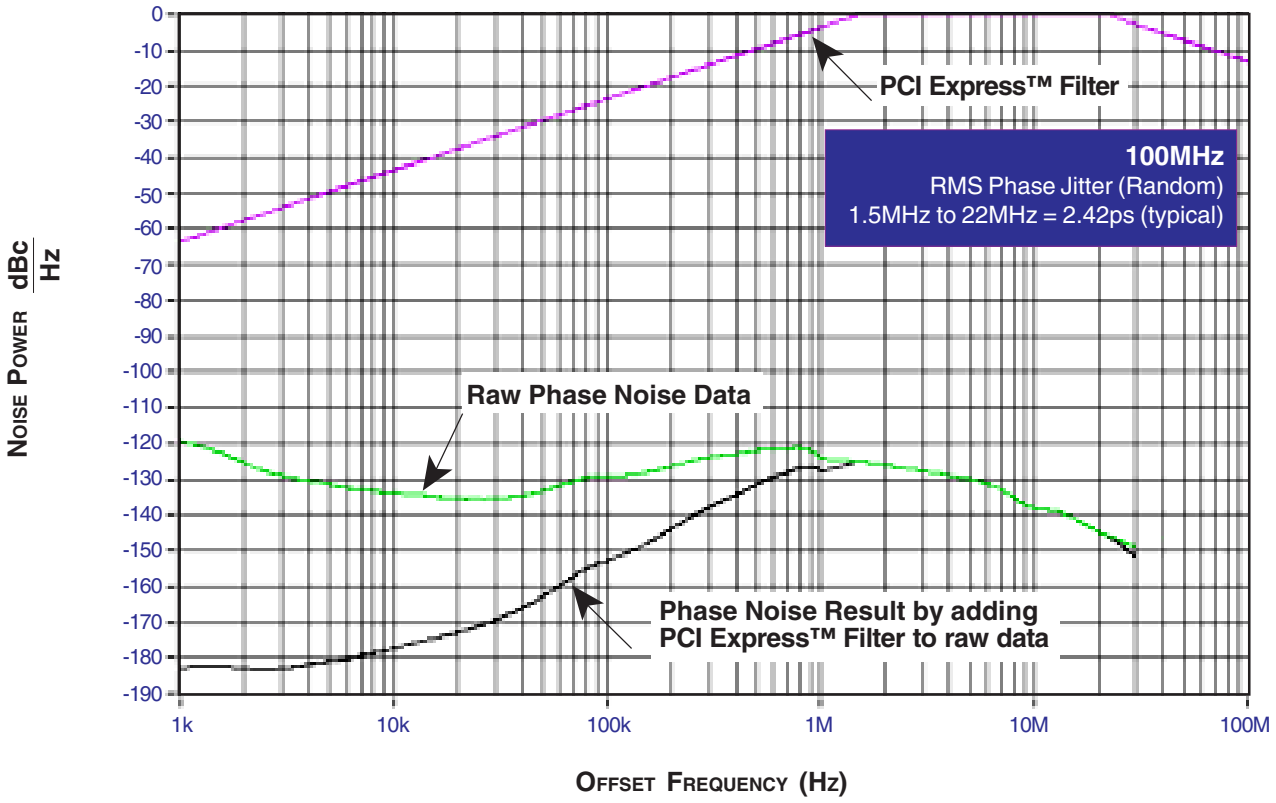
| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $I_{OH}$ | Output Current | | 12 | 14 | 16 | mA |
| $V_{OH}$ | Output High Voltage | | 610 | | 780 | mV |
| $V_{OL}$ | Output Low Voltage | | | | 65 | mV |
| $I_{OZ}$ | High Impedance Leakage Current | | -10 | | 10 | µA |
| $V_{OX}$ | Output Crossover Voltage | | 250 | | 550 | mV |

**TABLE 5. AC CHARACTERISTICS,** $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $T_A$ = 0°C TO 70°C, RREF = 475Ω

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $f_{MAX}$ | Output Frequency | | | | 140 | MHz |
| *t*sk(o) | Output Skew; NOTE 1, 2 | | | 50 | 110 | ps |
| *t*jit(cc) | Cycle-to-Cycle Jitter | Outputs @ Different Frequencies | | | 110 | ps |
| | | Outputs @ Same Frequencies | | | 50 | ps |
| *t*jit(Ø) | RMS Phase Jitter (Random); NOTE 3 | Integration Range: 1.5MHz - 22MHz | | 2.42 | | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time | 20% to 80% | 300 | | 1100 | ps |
| odc | Output Duty Cycle | | 48 | | 52 | % |

NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Please refer to the Phase Noise Plot following this section.

## TYPICAL PHASE NOISE AT 100MHZ

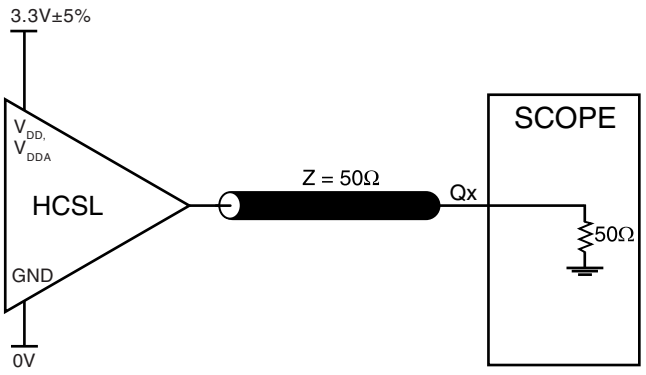



The illustrated phase noise plot was taken using a low phase noise signal generator, the noise floor of the signal generator is less than that of the device under test.

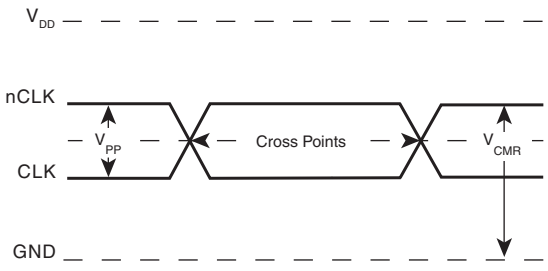
Using this configuration allows one to see the true spectral purity or phase noise performance of the PLL in the device under test.

Due to the tracking ability of a PLL, it will track the input signal up to its loop bandwidth. Therefore, if the input phase noise is greater than that of the PLL, it will increase the output phase noise performance of the device. It is recommended that the phase noise performance of the input is verified in order to achieve the above phase noise performance.

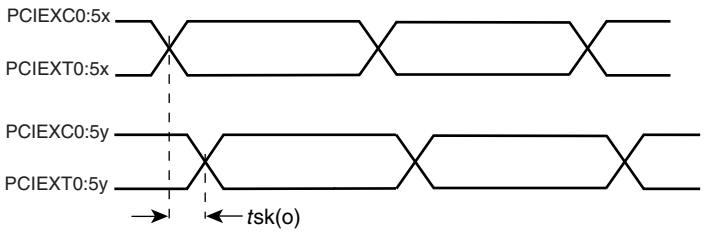
# PARAMETER MEASUREMENT INFORMATION



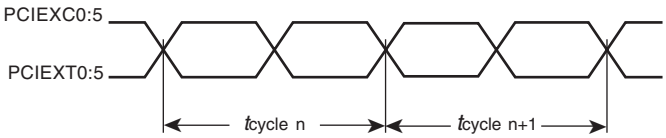

**3.3V HCSL OUTPUT LOAD AC TEST CIRCUIT**




**DIFFERENTIAL INPUT LEVEL**



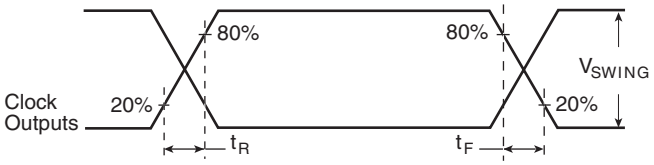

**OUTPUT SKEW**



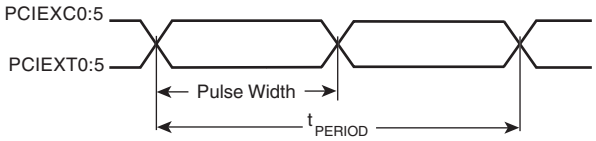

$t_{jit(cc)} = t_{cycle\ n} - t_{cycle\ n+1}$

1000 Cycles

**CYCLE-TO-CYCLE JITTER**




**HCSL OUTPUT RISE/FALL TIME**




$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

**OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD**

# APPLICATION INFORMATION

## POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS9DB206 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. $V_{DD}$ and $V_{DDA}$ should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 24Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each $V_{DDA}$ pin.

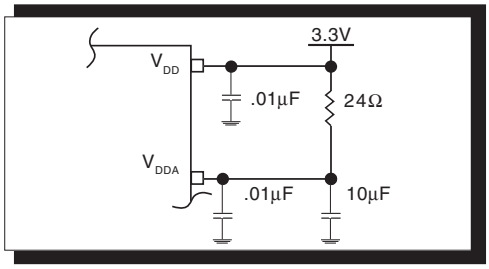



**FIGURE 1. POWER SUPPLY FILTERING**

## WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

*Figure 2* shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = $V_{DD}$/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and $V_{DD}$ = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

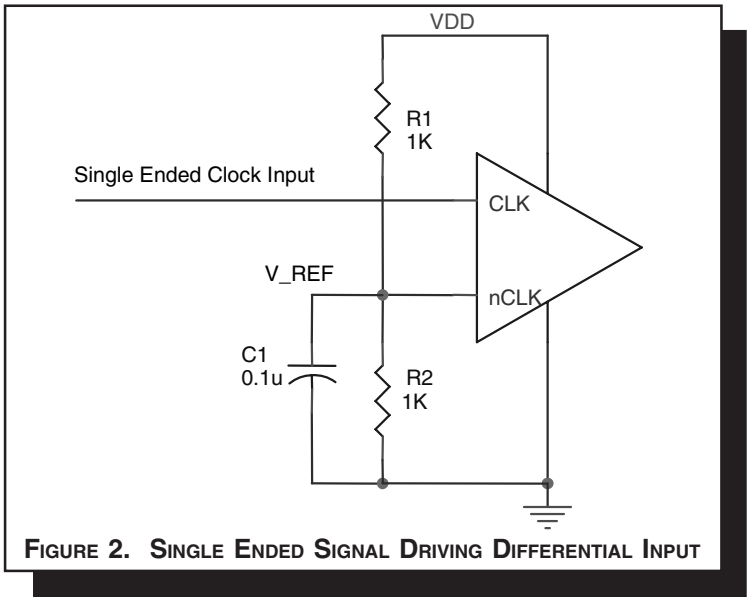



**FIGURE 2. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT**

## DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both $V_{SWING}$ and $V_{OH}$ must meet the $V_{PP}$ and $V_{CMR}$ input requirements. Figures 3A to 3D show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 3A,* the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

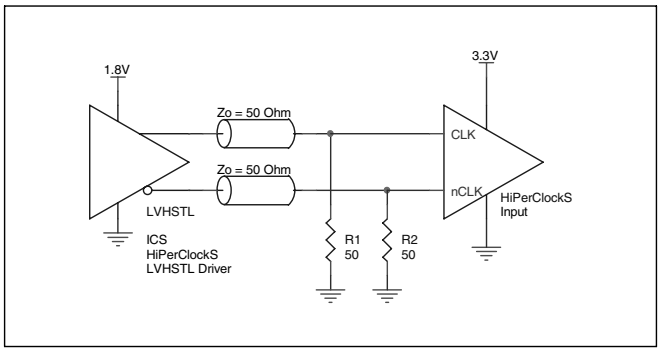



**FIGURE 3A. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY ICS HIPERCLOCKS LVHSTL DRIVER**

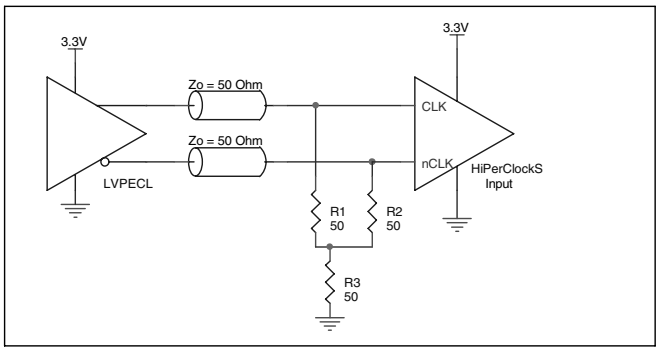



**FIGURE 3B. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER**

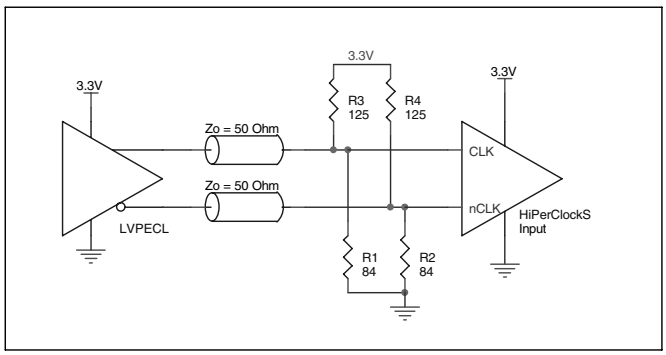



**FIGURE 3C. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER**

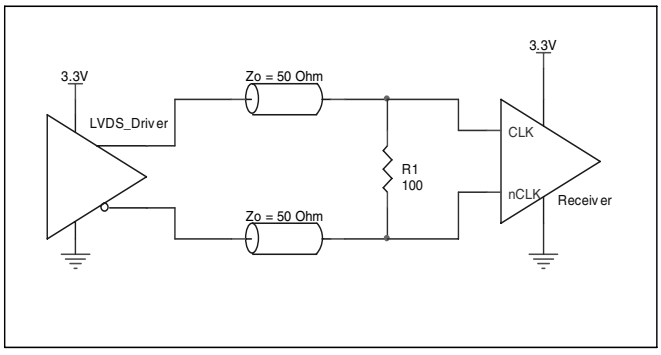



**FIGURE 3D. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVDS DRIVER**

## SCHEMATIC EXAMPLE

The schematic below illustrates two different terminations. Both are reliable and adequate. The PCI Express termination is recommended for all PCI Express application. The optional termination, which has a slightly better signal integrity, is recommended for all other applications.

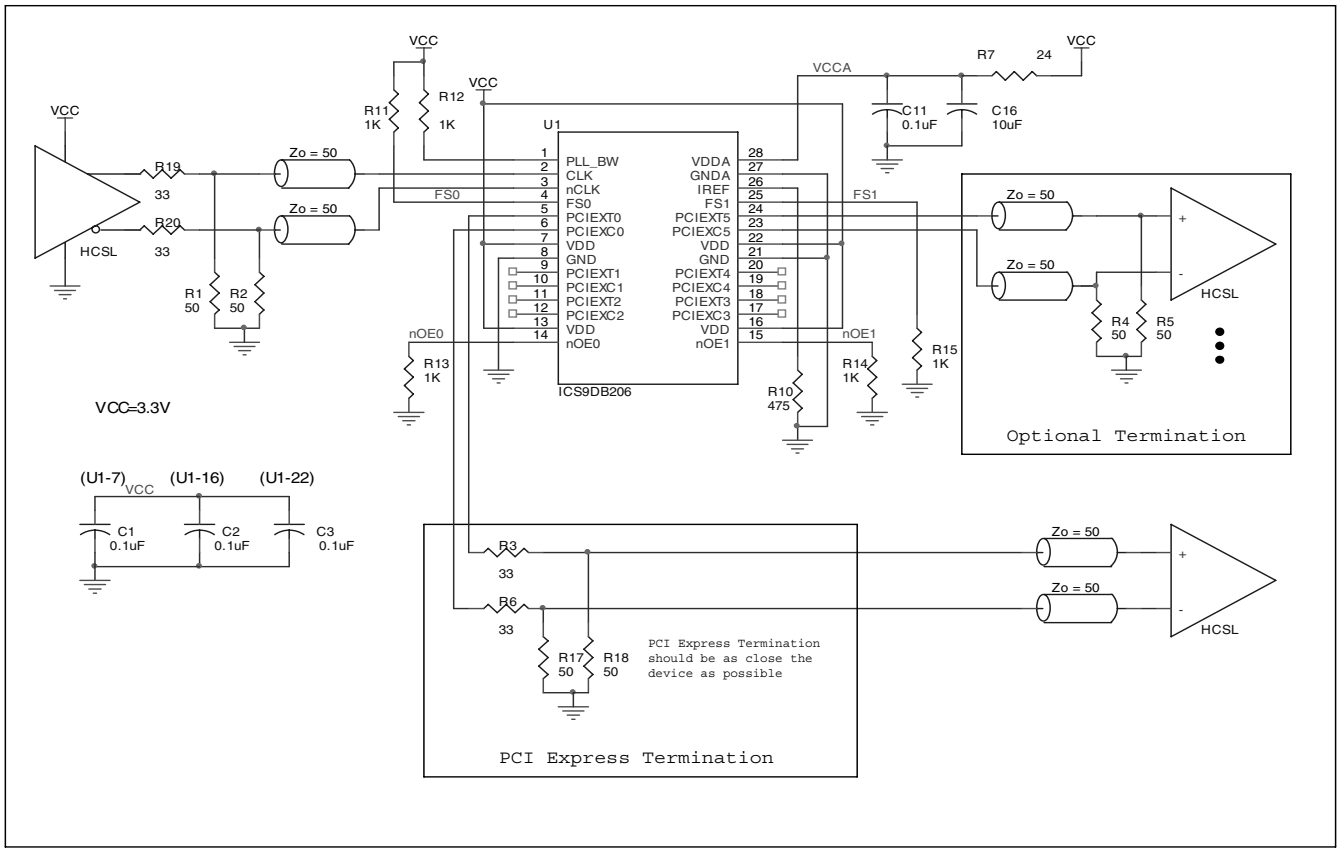



**FIGURE 4. EXAMPLE OF ICS9DB206 SCHEMATIC**

# RELIABILITY INFORMATION

**TABLE 6A. $\theta_{JA}$ VS. AIR FLOW TABLE FOR 28 LEAD TSSOP PACKAGE**

| $\theta_{JA}$ by Velocity (Linear Feet per Minute) | | | |
|---|---|---|---|
| | **0** | **200** | **500** |
| Single-Layer PCB, JEDEC Standard Test Boards | 82.9°C/W | 68.7°C/W | 60.5°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 49.8°C/W | 43.9°C/W | 41.2°C/W |

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

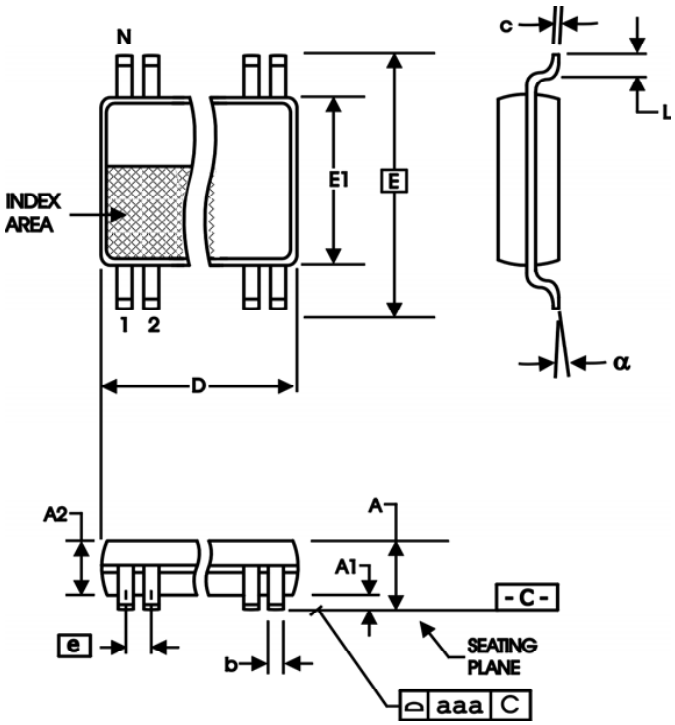
**TABLE 6B. $\theta_{JA}$ VS. AIR FLOW TABLE FOR 28 LEAD SSOP PACKAGE**

| $\theta_{JA}$ by Velocity (Linear Feet per Minute) | | | |
|---|---|---|---|
| | **0** | **200** | **500** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 49°C/W | 36°C/W | 30°C/W |

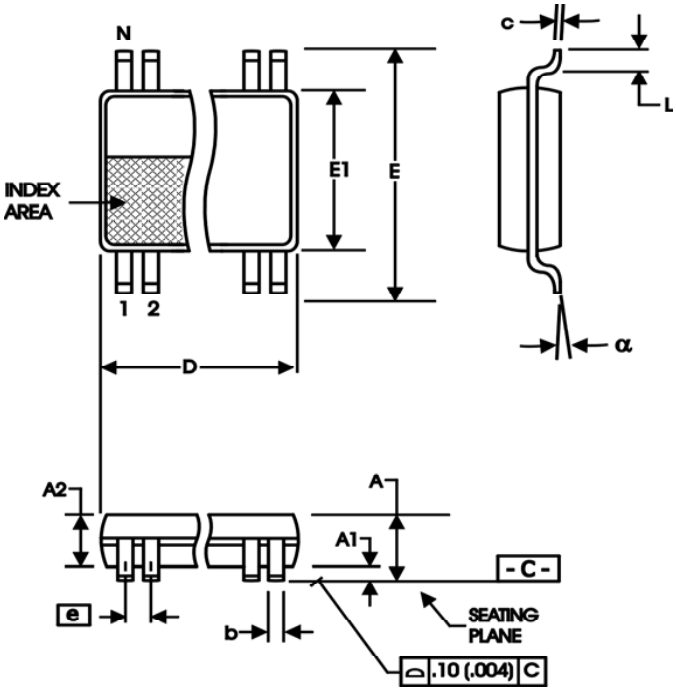
**TRANSISTOR COUNT**

The transistor count for ICS9DB206 is: 2471

## PACKAGE OUTLINE - L SUFFIX FOR 28 LEAD TSSOP




## PACKAGE OUTLINE - F SUFFIX FOR 28 LEAD SSOP




### TABLE 6A. PACKAGE DIMENSIONS

| SYMBOL | Millimeters | |
|---|---|---|
| | Minimum | Maximum |
| N | 28 | |
| A | -- | 1.20 |
| A1 | 0.05 | 0.15 |
| A2 | 0.80 | 1.05 |
| b | 0.19 | 0.30 |
| c | 0.09 | 0.20 |
| D | 9.60 | 9.80 |
| E | 6.40 BASIC | |
| E1 | 4.30 | 4.50 |
| e | 0.65 BASIC | |
| L | 0.45 | 0.75 |
| α | 0° | 8° |
| aaa | -- | 0.10 |

Reference Document: JEDEC Publication 95, MO-153

### TABLE 6B. PACKAGE DIMENSIONS

| SYMBOL | Millimeters | |
|---|---|---|
| | Minimum | Maximum |
| N | 28 | |
| A | | 2.00 |
| A1 | 0.05 | |
| A2 | 1.65 | 1.85 |
| b | 0.22 | 0.38 |
| c | 0.09 | 0.25 |
| D | 9.90 | 10.50 |
| E | 7.40 | 8.20 |
| E1 | 5.00 | 5.60 |
| e | 0.65 BASIC | |
| L | 0.55 | 0.95 |
| α | 0° | 8° |

Reference Document: JEDEC Publication 95, MO-150

**TABLE 7. ORDERING INFORMATION**

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|---|---|---|---|---|
| ICS9DB206CL | ICS9DB206CL | 28 Lead TSSOP | Tube | 0°C to 70°C |
| ICS9DB206CLT | ICS9DB206CL | 28 Lead TSSOP | 1000 Tape & Reel | 0°C to 70°C |
| ICS9DB206CLLF | ICS9DB206CLLF | 28 Lead "Lead-Free" TSSOP | Tube | 0°C to 70°C |
| ICS9DB206CLLFT | ICS9DB206CLLF | 28 Lead "Lead-Free" TSSOP | 1000 Tape & Reel | 0°C to 70°C |
| ICS9DB206CF | ICS9DB206CF | 28 Lead SSOP | Tube | 0°C to 70°C |
| ICS9DB206CFT | ICS9DB206CF | 28 Lead SSOP | 1000 Tape & Reel | 0°C to 70°C |
| ICS9DB206CFLF | ICS9DB206CFLF | 28 Lead "Lead-Free" SSOP | Tube | 0°C to 70°C |
| ICS9DB206CFLFT | ICS9DB206CFLF | 28 Lead "Lead-Free" SSOP | 1000 Tape & Reel | 0°C to 70°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

| REVISION HISTORY SHEET | | | | |
|---|---|---|---|---|
| **Rev** | **Table** | **Page** | **Description of Change** | **Date** |
| A | T7 | 12 | Ordering Information Table - added Lead-Free marking for TSSOP package. | 11/29/04 |
| B | T4D | 4 | HCSL Table -adjusted $V_{OH}$ min from 680mV to 610mV and added $V_{OH}$ max. | 12/21/04 |
| B | T7 | 12 | Ordering Information Table - added Lead-Free marking for SSOP package. | 3/21/05 |