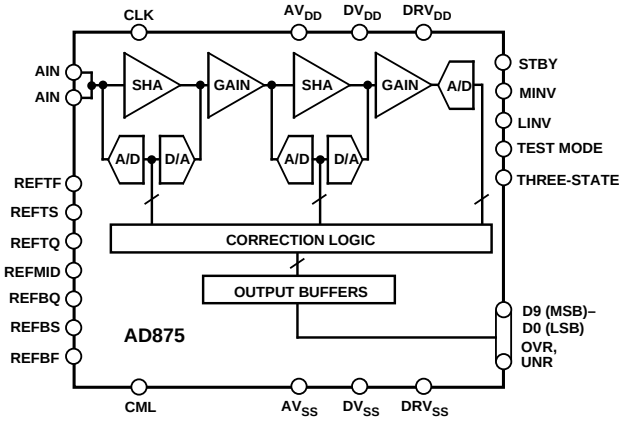
10-Bit, 15 MHz, 185 mW CMOS A/D Converter

AD875

FEATURES
CMOS 10-Bit, 15 MHz A/D Converter
Low Power Dissipation: 185 mW
+5 V Single-Supply Operation
Differential Nonlinearity: 0.4 LSB
Guaranteed No Missing Codes
Power-Down (Standby) Mode: <50 mW
Three-State Outputs
Digital I/Os Compatible with +5 V or +3.3 V Logic
Adjustable Reference Input
Small Size: 48-Pin Thin Quad Flatpack (TQFP)

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD875 is a CMOS, low power 10-bit, 15 MHz analog-to-digital converter (ADC). The AD875 combines high speed 10-bit resolution and performance with low power and single supply operation. By implementing a multistage pipelined architecture with output error correction logic, the AD875 offers accurate performance and guarantees no missing codes over the full operating temperature range. To minimize external voltage drops, the reference ladder top and bottom are provided with force and sense pins.

The AD875's digital I/Os can interface to either +5 V or +3.3 V logic. The AD875 can be placed into a standby mode of operation reducing the power below 50 mW. Digital output data can be placed in a high impedance state and is offered in a variety of formats, including straight binary and twos complement output. The AD875 also provides both underrange and overrange output bits, indicating when the analog input has exceeded the analog input range.

The AD875's speed, resolution and single-supply operation are ideally suited for a variety of applications in imaging, high speed data acquisition and communications. The AD875's low power and single supply operation are required for high speed portable applications. Its speed and resolution are ideally suited for charge coupled device (CCD) input systems such as color scanners, digital copiers, electronic still cameras and camcorders.

The AD875 is packaged in a space saving 48-pin thin quad flatpack (TQFP) and is specified over the commercial (0°C to +70°C) temperature range.

PRODUCT HIGHLIGHTS

Low Power—The AD875 at 185 mW consumes a fraction of the power of presently available 10-bit, video-speed converters. Power-down mode and single-supply operation further enhance its desirability in low power, battery operated applications such as electronic still cameras, camcorders and communication systems.

Superior Differential Nonlinearity Performance—The AD875's typical DNL performance is 0.4 LSB and a maximum of 0.8 LSBs for the 0 to 255 code range (ideal for imaging systems). No missing codes are guaranteed.

Very Small Package—The AD875 is available in a 48-pin surface mount, thin quad flatpack. The TQFP package is ideal for very tight, low headroom designs. The AD875 is available in tape and-reel.

Digital I/O Functionality—The AD875 offers several digital features which allow output data formatting, fixed output test pattern generation to facilitate in-circuit testing, three-state output control and over/underrange indicators.

REV. 0

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AD875–SPECIFICATIONS

DC SPECIFICATIONS (T_{MIN} to T_{MAX} with AV_{DD} = +5.0 V, DV_{DD} = +5.0 V, DRV_{DD} = +3.3 V, V_{REFTF} = +4.0 V, V_{REFBF} = +2.0 V, f_{CLOCK} = 15 MHz, unless otherwise noted)

Parameter	Min	Typ	Max	Units
RESOLUTION	10			Bits
DC ACCURACY				
Integral Nonlinearity (INL)		±1.5	±2.5	LSB
Differential Nonlinearity (DNL)				
Codes 0 to 255		±0.4	±0.8	LSB
Codes 256 to 1023		±0.4	±1	LSB
No Missing Codes		GUARANTEED		
Offset		0.1		%FSR
Gain		0.2		%FSR
ANALOG INPUT				
Input Range	1.8	2	2.2	V p-p
Input Resistance		100		kΩ
Input Current		10		μA
Input Capacitance		5		pF
REFERENCE INPUT				
Reference Top Voltage	3.6	4.0	4.1	V
Reference Bottom Voltage	1.6	2.0	2.1	V
Reference Input Resistance	250	400		Ω
Reference Input Current		5	8	mA
Force-Sense Offset				
Top		25		mV
Bottom		25		mV
POWER SUPPLIES				
Operating Voltages				
AV_{DD}	+4.5		+5.25	Volts
DV_{DD}	+4.5		+5.25	Volts
DRV_{DD}	+3.0		+5.25	Volts
Operating Current				
IAV_{DD}		19	34	mA
IDV_{DD}		17	25	mA
$IDRV_{DD}$[1]		1	5	mA
POWER CONSUMPTION		185	235	mW
TEMPERATURE RANGE				
Operating	0		+70	°C

NOTE
[1]C_L = 20 pF.

Specifications subject to change without notice. See Definition of Specifications for additional information.

DIGITAL SPECIFICATIONS (T_{MIN} to T_{MAX} with AV_{DD} = +5.0 V, DV_{DD} = +5.0 V, DRV_{DD} = +3 3 V, V_{REFTF} = +4.0 V, V_{REFBF} = +2.0 V, f_{CLOCK} = 15 MHz, C_L = 20 pF unless otherwise noted)

Parameter	Symbol	DRV_{DD}	Min	Typ	Max	Units
LOGIC INPUT						
High Level Input Voltage	V_{IH}	3.0	2.4			V
		4.75	3.8			V
		5.25	4.2			V
Low Level Input Voltage	V_{IL}	3.0			0.6	V
		4.75			0.95	V
		5.25			1.05	V
High Level Input Current	I_{IH}	4.75	–10		+10	μA
Low Level Input Current	I_{IL}	4.75	–50		+50	μA
Low Level Input Current (CLK Only)	I_{IL}	4.75	–10		+10	μA
Input Capacitance	C_{IN}			5		pF
LOGIC OUTPUTS						
High Level Output Voltage	V_{OH}					
(I_{OH} = 50 μA)		3.0	2.4			V
		4.75	3.8			V
(I_{OH} = 0.5 mA)		4.75	2.4			V
Low Level Output Voltage	V_{OL}					
(I_{OL} = 50 μA)		3.6			0.7	V
		5.25			1.05	V
(I_{OL} = 0.6 mA)		5.25			0.4	V
Output Capacitance	C_{OUT}			5		pF
Output Leakage Current	I_{OZ}		–10		+10	μA

Specifications subject to change without notice.

TIMING SPECIFICATIONS (T_{MIN} to T_{MAX} with AV_{DD} = +5.0 V, DV_{DD} = +5.0 V, DRV_{DD} = +3.3 V, V_{REFTF} = +4.0 V, V_{REFBF} = +2.0 V, f_{CLOCK} = 15 MHz, C_L = 20 pF unless otherwise noted)

	Symbol	Min	Typ	Max	Units
Maximum Conversion Rate[1]		15			MHz
Clock Period	t_C	66			ns
Clock High	t_{CH}	30	33		ns
Clock Low	t_{CL}	30	33		ns
Output Delay[2]	t_{OD}	12	15		ns
Pipeline Delay (Latency)				3	Clock Cycles
Sampling Delay 1[3]	t_{S1}		2.5		ns
Sampling Delay 2[3]	t_{S2}		2.5		ns
External Settling Requirement[3]	V_{SE}			±16	mV

NOTES
[1]Conversion rate is operational down to 10 kHz without degradation in specified performance.
[2]C_L = 20 pF.
[3]See the section entitled "Driving the Analog Input."

Specifications subject to change without notice.

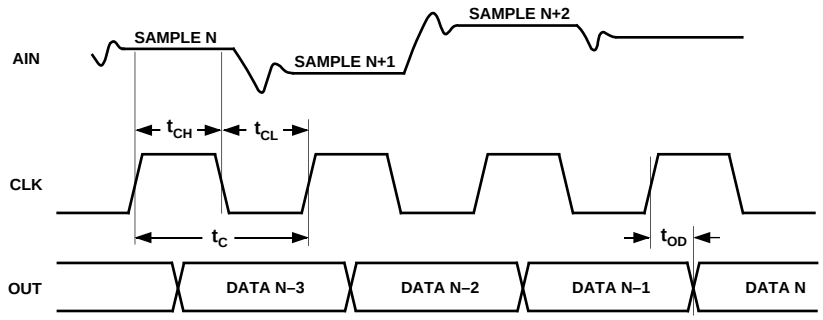
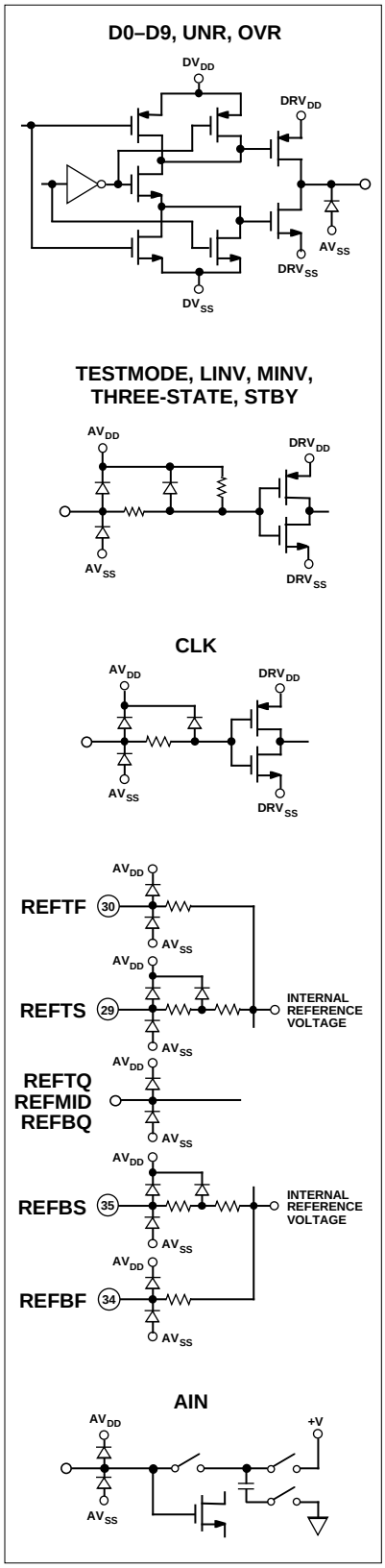


Figure 1. AD875 Timing Diagram

PIN DESCRIPTIONS

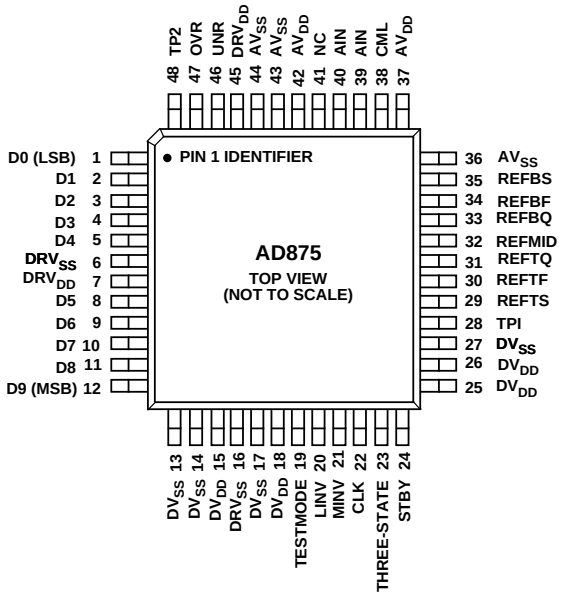
Symbol	Pin No.	Type	Name and Function	
D0 (LSB)	1	DO	Least Significant Bit	
D1–D4	2–5	DO	Data Bits 1 Through 4	
D5–D8	8–11	DO	Data Bits 5 Through 8	
D9 (MSB)	12	DO	Most Significant Bit	
UNR	46	DO	Underrange Output	
OVR	47	DO	Overrange Output	
TESTMODE	19	DI	TESTMODE = LOW 1 0 1 0 . . . Pattern On D0-D9	TESTMODE = HIGH or N/C Normal Operating Mode
LINV	20	DI	Invert the Lower Order Output Bits LINV = LOW No Inversion	LINV = HIGH or N/C Invert Low Order Output Bits (D0–D8)
MINV	21	DI	Invert the Most Significant Bit MINV = LOW No Inversion	MINV = HIGH or N/C Invert MSB (D9)
THREE-STATE	23	DI	THREE-STATE = LOW Normal Operating Mode	THREE-STATE = HIGH or N/C High Impedance Outputs
STBY	24	DI	STBY = LOW Normal Operating Mode	STBY = HIGH or N/C Standby Mode
CLK	22	DI	Clock Input	
CML	38	AO	Bypass Pin for an Internal Bias Point. A 10 µF capacitor in parallel with a 0.1 µF capacitor must be connected to CML. CML is not to be used to drive external circuitry.	
REFTS	29	AI	Reference Top Sense	
REFTF	30	AI	Reference Top Force	
REFTQ	31	AI	Reference Top Quarter Point (Bypass)	
REFMID	32	AI	Reference Midpoint (Bypass)	
REFBQ	33	AI	Reference Bottom Quarter Point (Bypass)	
REFBF	34	AI	Reference Bottom Force	
REFBS	35	AI	Reference Bottom Sense	
AIN	39, 40	AI	Analog Input	
AV_{DD}	37, 42	P	+5 V Analog Supply	
AV_{SS}	36, 43, 44	P	Analog Ground	
DV_{DD}	15, 18, 25, 26	P	+5 V Digital Supply	
DV_{SS}	13, 14, 17, 27	P	Digital Ground	
DRV_{DD}	7, 45	P	+3.3 V/+5 V Digital Supply. Supply for Digital Input and Output Buffers	
DRV_{SS}	6, 16	P	+3.3 V/+5 V Digital Ground. Ground for Digital Input and Output Buffers	
TP1	28	P	Connect to AV_{SS} (Analog Ground)	
TP2	48	P	Connect to DV_{SS} (Digital Ground)	
N/C	41		No Connect	

TYPE: AI = Analog Input; AO = Analog Output; DI = Digital Input;
DO = Digital Output;
P = Power.



Equivalent Circuits

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Package
AD875JST	0°C to +70°C	48-Pin TQFP
AD875JST-Reel	0°C to +70°C	48-Pin TQFP (Tape and Reel 13")

TYPICAL CHARACTERISTIC CURVES

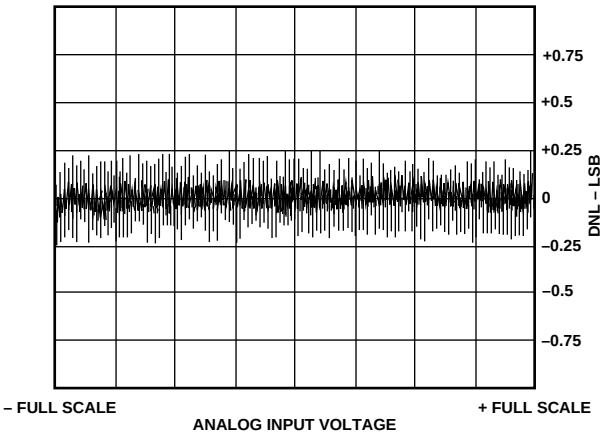


Figure 2. Typical DNL

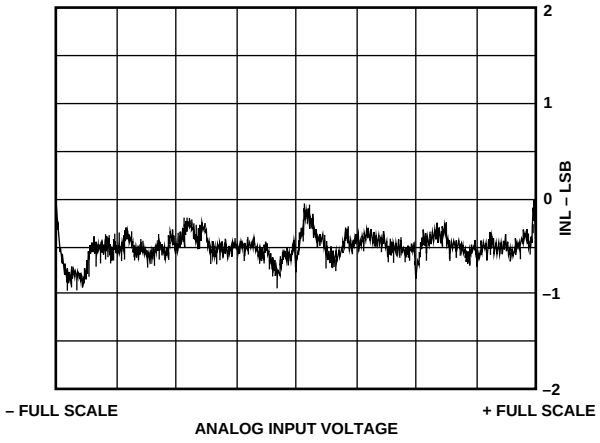


Figure 3. Typical INL

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min	Max	Units
AV_{DD}	AV_{SS}	–0.5	+6.5	Volts
DV_{DD}, DRV_{DD}	DV_{SS}, DRV_{SS}	–0.5	+6.5	Volts
AV_{SS}	DV_{SS}, DRV_{SS}	–0.5	+0.5	Volts
AIN	AV_{SS}	–0.5	+6.5	Volts
REFTS, REFTF, REFBS, REFBF	AV_{SS}	–0.5	+6.5	Volts
Digital Inputs, CLK	DV_{SS}, DRV_{SS}	–0.5	+6.5	Volts
Junction Temperature			+150	°C
Storage Temperature		–65	+150	°C
Lead Temperature (10 sec)			+300	°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD875 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

DEFINITIONS OF SPECIFICATIONS

Integral Nonlinearity (INL)
Integral nonlinearity refers to the deviation of each individual code from a line drawn from "zero" through "full scale." The point used as "zero" occurs 1/2 LSB before the first code transition. "Full scale" is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line.

Differential Nonlinearity (DNL, No Missing Codes)
An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. It is often specified in terms of the resolution for which no missing codes (NMC) are guaranteed.

Offset Error
The first transition should occur at a level 1/2 LSB above "zero." Offset is defined as the deviation of the actual first code transition from that point.

Gain Error
The first code transition should occur for an analog value 1/2 LSB above nominal negative full scale. The last transition should occur for an analog value 1 1/2 LSB below the nominal positive full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between the first and last code transitions.

Pipeline Delay (Latency)
The number of clock cycles between conversion initiation and the associated output data being made available. New output data is provided every clock cycle.

Reference Force/Sense Offset
Resistance between the reference input and comparator input tap points causes offset errors. These errors can be nulled out by using the force-sense connection as shown in the Reference Input section.

THEORY OF OPERATION

The AD875 uses a pipelined multistage architecture to achieve high sample rate with low power. The multistage approach distributes the conversion over several smaller A/D sub-blocks, refining the conversion with progressively higher accuracy as it passes the results from stage to stage. As a consequence of the distributed conversion, the AD875 requires only a small fraction of the 1023 comparators that would be required in a more traditional 10-bit flash type A/D. A sample-and-hold (SHA) function within each of the stages permits the first stage to operate on a new sample of the input while the second and third stages operate on the two preceding samples. This "assembly line" operation on multiple samples, known as pipelining, allows higher throughput at the cost of some delay, referred to as latency. (See the output timing diagram.)

The detailed operation is as follows: the first stage makes a 4-bit estimate of the analog input voltage by means of the first stage A/D sub-block. The first stage estimate is converted to analog form by the first stage D/A and subtracted from the original input signal. The remainder, or residue, is the difference between the first stage estimate and the actual analog input. Next, the residue is amplified and passed to the second stage where another A/D sub-block makes a 4-bit estimate of its value. Again the analog version of the estimate is subtracted from the signal and an even finer residue is generated. Finally, the A/D sub-block in the last stage measures the value of this second stage residue.

The A/D sub-blocks within each stage are actually 4-bit flash converters. Ideally 3 bits in the second and third stages would be sufficient for a 10-bit A/D. The additional bits allow for digital correction of errors in preceding stages, reducing the tolerances on the sub-block components and making a more robust A/D. The reference ladders for all three of these flash sub-blocks are wired in parallel and connected to the reference pins of the AD875.

Inside the AD875 all signals are processed differentially. This not only enhances the internal dynamic range of the components but provides a high level of noise immunity in a digital environment.

APPLYING THE AD875

DRIVING THE ANALOG INPUT

The high input resistance and low input capacitance features of the AD875 simplify the current and settling time demands placed on input drive circuitry. Figure 4 shows the equivalent input circuit of the AD875.

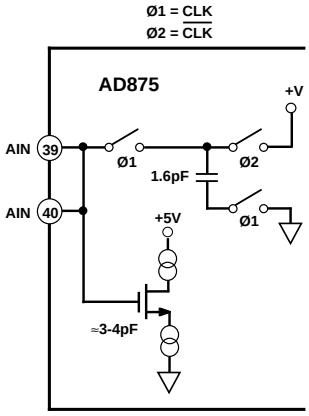


Figure 4. AD875 Equivalent Input Structure

The full-scale input range is set by the voltage span, REFTF-REFBF (see "Driving the Reference" section). The recommended span should nominally be 2 V peak-to-peak. This span must remain bounded by the minimum and maximum input range (specified in the Analog Input section under DC Specifications). Some example input ranges are given in Table I.

Table I. Input Range Examples

–Full Scale = REFBF (V)	+Full Scale = REFTF (V)	Input Span (V)
+1.6	+3.6	+2.0
+2.0	+4.0	+2.0
+2.1	+4.1	+2.0

While the input impedance of the AD875 is quite high, the switched capacitor input structure results in a small dynamic input current. In order to prevent gain variations as a result of the input current, maintaining a source impedance of less than

or equal to 75 Ω is suggested (Figure 5). In general, a low drive impedance is suggested to minimize noise coupled on the AIN inputs.

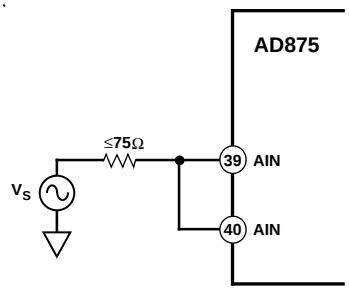


Figure 5. Simple AD875 Drive Requirements

For systems which must level shift a ground-referenced signal in order to comply with the input requirements of the AD875, a circuit like Figure 6 is recommended. The suggested op amp, an AD817 or AD818, is configured in inverting mode, where the ac gain of the input signal is –1. The amount of dc-level shifting is controlled by the dc voltage at the noninverting input of the op amp. The REFBF signal is attenuated by a resistive voltage divider and then multiplied by 2. In the case where REFBF = 1.6 V, the dc output level will be 2.6 V. The AD817 is a low cost, fast settling, single-supply op amp with a 29 MHz unity gain bandwidth. The AD818 is similar to the AD817 but has a 50 MHz unity gain bandwidth.

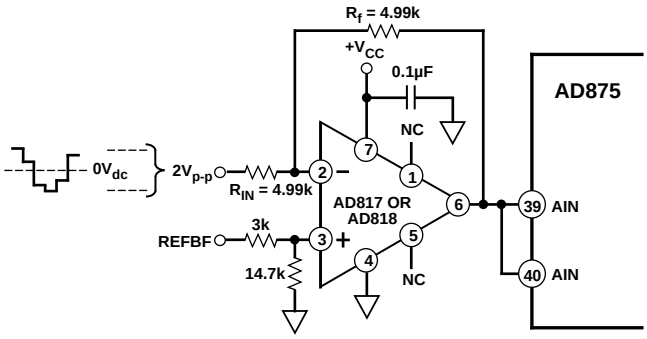


Figure 6. DC Level Shift with Gain of –1×

The AD875 samples the analog input voltage twice: once on the rising edge of the clock (CLK) and once on the falling edge. The first sample, taken on the rising edge, is used to perform a coarse estimate of the input. As indicated in Figure 7, the analog input voltage must be settled within V_{SE} (±16 mV) of its final value at this time and must remain within V_{SE} until the second sample has been taken. The second sample, taken on the falling edge of the clock, will determine the exact value digitized and should be accurate to within 10 bits (0.1%). Note that the actual sample points are delayed by t_{S1} and t_{S2}.

For applications where step input signals are expected (i.e., CCD or multiplexed outputs), the settling time of the input drive circuitry should be examined carefully. In most cases, the settling time requirements placed on the input amplifier are easily met by the AD817 or AD818. For higher speed operation, it may be necessary to use faster op amps such as the AD810 or AD811.

As a result of the AD875's settling requirements, there is a maximum slew rate limitation placed on the analog input signal. For applications using CCDs and other sampled analog systems, the AD875 can be used directly. However, for continuous signal applications, Figure 7 implies a maximum slew rate limitation on the analog input:

$$Slew\ Rate\ of\ Analog\ Input\ (maximum) = \frac{16\ mV}{t_{CH}}\ (V/sec)$$

where t_{CH} is the "high" period of the sample clock in seconds, or one-half the full period when the clock is run with 50% duty cycle. For example, at 15 MHz clock rate, the maximum slew rate is about 0.48 V/μs. This corresponds to a maximum analog input frequency of 76 kHz when a full-scale (2 V peak-to-peak) sine wave is used. For input signals with higher slew rates, a sample-and-hold amplifier must be used for accurate digitization.

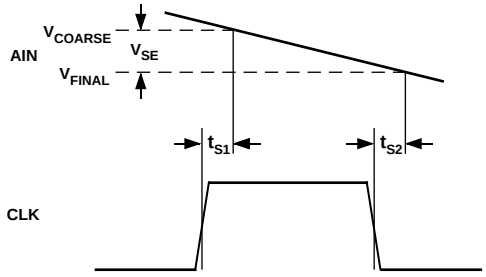


Figure 7. Analog Input Settling Requirement

REFERENCE INPUT

Driving the Reference Terminals

The AD875 requires an external reference on pins REFTF and REFBF. Reference sense pins REFTS and REFBS are also provided for Kelvin connections to minimize voltage drops due to external and internal wiring resistances. A resistor ladder nominally 400 Ω is connected internally between pins REFTF and REFBF.

The voltage drop across the internal resistor ladder determines the input span of the AD875. The driving voltages required at the REFTF and REFBF pins are nominally +4 V and +2 V respectively resulting in a 2 V input span. In order to maintain the requisite 2 V drop across the internal ladder, the external reference must be capable of typically providing 5 mA of dc current.

Transient current flows in and out of the REFTF and REFBF pins. Therefore, a low ac impedance is required at these terminals for proper operation. Bypassing each pin with suitable capacitive decoupling should effectively attenuate any transients. See the AD875 Evaluation Board Schematic for recommended values. Mid (REFMID) and quarter (REFTQ, REFBQ) ladder tap points are also available for additional decoupling if required. It is important to note that these tap points cannot be used to correct integral linearity as is sometimes done in a typical flash converters.

There are several reference configurations suitable for the AD875 depending on the application, desired performance and cost trade-offs. The simplest configuration, shown in Figure 8, utilizes a resistor string to generate the reference voltages from the converter's analog power supply. A 10 μF tantalum capacitor in parallel with a 0.1 μF ceramic capacitor will provide adequate decoupling for both the REFTF and REFBF pins. The 0.1 μF capacitors should be physically located within 1 cm of REFTF and REFBF. A 10 μF capacitor connected between

REFTF and REFBF is also recommended for optimum performance. This reference configuration provides the lowest cost solution but has several disadvantages including poor dc power supply rejection and poor accuracy due to the variability of the internal and external resistor values.

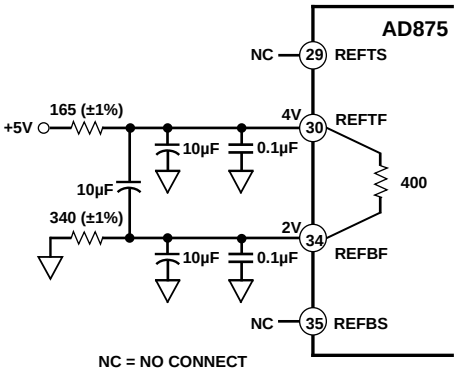


Figure 8. Low Cost Reference Circuit

A higher performance solution employs a voltage regulator to improve dc power supply rejection and absolute accuracy. Figure 9 shows a LM317 adjustable regulator configured to generate a 1.6 V output for REFBF. This output is also used to generate the 3.6 V REFTF signal by multiplying the REFBF signal by 2.25. Note that the AD817 op amp used to multiply REFBF has been compensated to ensure stability while driving the large capacitive load. The accuracy of this solution is limited by the external resistors and the initial accuracy of the reference.

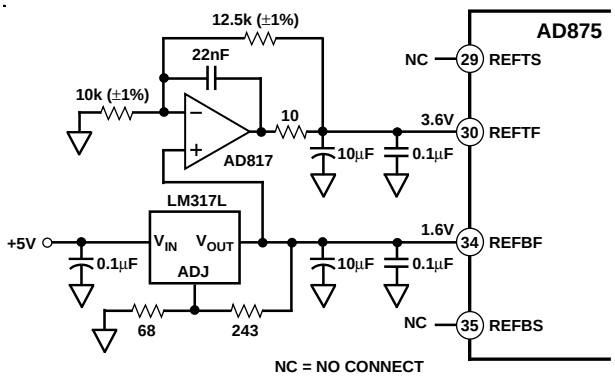


Figure 9. Reference Circuit with Good PSRR

For optimal performance, a force sense or Kelvin configuration can be used as shown in Figure 10. This circuit uses a high-accuracy reference (AD589) and a dual op amp (OP295) to maintain accuracy and minimize voltage drops which are generated in the wire connections to the REFTF and REFBF inputs. The output of the AD589 is increased to 1.6 V and 3.6 V at the outputs of the op amps as required. Both op amps are compensated to maintain stability while driving the decoupling capacitors required at the REFTF and REFBF pins.

These outputs, being connected in a feedback loop, tend to cancel any errors caused by the voltage drops in the wires. Note that if the REFTS and REFBS are not used in a force sense configuration, they should be left unconnected and should not be connected to REFTF and REFBF.

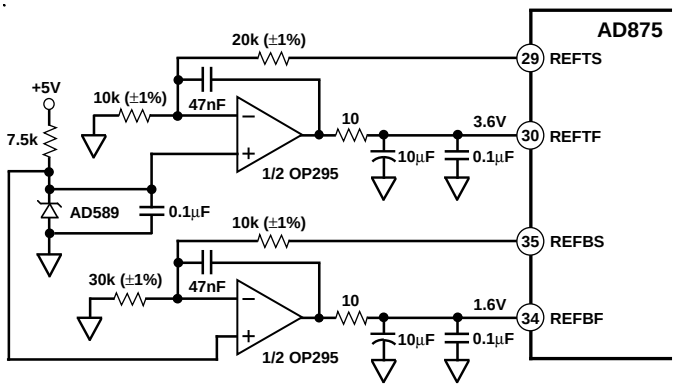


Figure 10. High Performance Reference Circuit Using Kelvin Connections

Like any high resolution converter, the layout and decoupling of the reference is critical. The actual voltage digitized by the AD875 is relative to the reference voltages. In Figure 11, for example, the reference returns and the bypass capacitors are connected to the shield of the incoming analog signal. Disturbances in the ground of the analog input, which will be common-mode to the REFTF, REFBF, and AIN pins because of the common ground, are effectively removed by the AD875's high common-mode rejection.

High frequency noise sources, V_{N1} and $V_{N2,}$ are shunted to ground by decoupling capacitors. Any voltage drops between the analog input ground and the reference bypassing points will be treated as input signals by the converter via the reference inputs. Consequently, the reference decoupling capacitors should be connected to the same analog ground point used to define the analog input voltage. (For further suggestions, see the "Grounding and Layout Rules" section of the data sheet.)

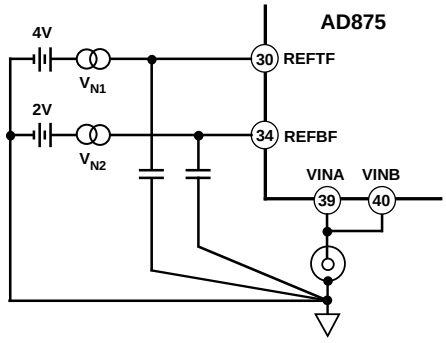


Figure 11. Recommended Bypassing for the Reference Inputs

CLOCK INPUT

The AD875 clock input is buffered internally with an inverter powered from the DRV_{DD} pin. This feature allows the AD875 to accommodate either +5 V or +3.3 V CMOS logic input signal swings with the input threshold for the CLK pin nominally at $DRV_{DD}/2$.

The AD875's pipelined architecture operates on both rising and falling edges of the input clock. To minimize duty cycle variations the recommended logic family to drive the clock input is high speed CMOS (HC/HCT) logic. HCMOS logic provides both symmetrical voltage threshold levels and sufficient rise and fall times to support 15 MHz operation. The AD875's minimum

clock half cycle may necessitate the use of an external divide-by-two circuit as shown in Figure 12.

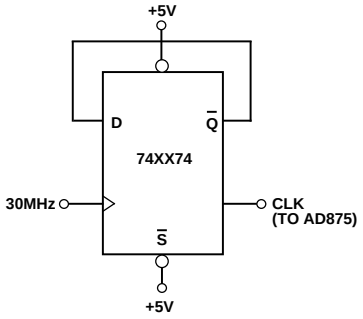


Figure 12. Divide-By-Two Clock Input Circuit

The AD875 is designed to support a conversion rate of 15 MHz; running the part at slightly faster clock rates may be possible, although at reduced performance levels. Conversely, some slight performance improvements might be realized by clocking the AD875 at slower clock rates.

The power dissipated by the correction logic and output buffers is largely proportional to the clock frequency; running at reduced clock rates provides a reduction in power consumption. Figure 13 illustrates this trade-off.

DIGITAL INPUTS AND OUTPUTS

Each of the AD875's digital control inputs, MINV, LINV, TEST MODE, THREE-STATE, and STBY is buffered with an inverter powered from the DRV_{DD} supply pins. With DRV_{DD} set to +5 V all digital inputs readily interface with 5 V CMOS logic.

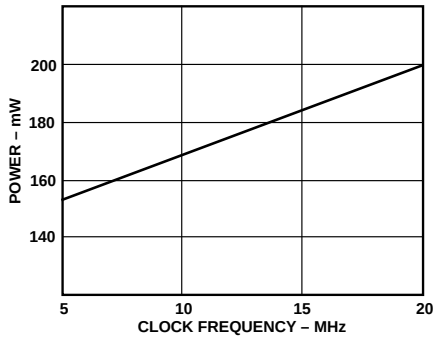


Figure 13. Typical Power Dissipation vs. Clock Frequency

For interfacing with lower voltage CMOS logic, DRV_{DD} can be set to 3.3 V effectively lowering the nominal input threshold of all digital inputs to 3.3 V/2 = 1.65 V.

The AD875 provides several convenient digital input pins for controlling the converter output format. By utilizing digital input pins MINV and LINV, three digital output formats are possible: binary, twos complement, and ones complement.

Another element of digital functionality is provided with the TEST MODE pin. To facilitate in-circuit testing of the digital portion of your application, a fixed digital pattern controlled by a digital input is available. For TEST MODE = LOW, an alternating 1010101010 pattern is established. This pattern is further manipulated when used in conjunction with the LINV and MINV pins (see Output Data Format, Table II below).

Table II. Output Data Format

Approx AIN (V)	MINV	LINV	Test Mode	Three State	OVR	(MSB) D9	D8	D7	D6	D5	D4	D3	D2	D1	(LSB) D0	UNR
>4	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	0
4	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	0
3	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0
2	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
<2	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1
X	0	0	0	0	?	1	0	1	0	1	0	1	0	1	0	?
>4	1	0	1	0	1	0	1	1	1	1	1	1	1	1	1	0
4	1	0	1	0	0	0	1	1	1	1	1	1	1	1	1	0
3	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
2	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0
<2	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	1
X	1	0	0	0	?	0	0	1	0	1	0	1	0	1	0	?
>4	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0
4	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0
3	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1	0
2	0	1	1	0	0	0	1	1	1	1	1	1	1	1	1	0
<2	0	1	1	0	0	0	1	1	1	1	1	1	1	1	1	1
X	0	1	0	0	?	1	1	0	1	0	1	0	1	0	1	?
>4	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0
4	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
3	1	1	1	0	0	0	1	1	1	1	1	1	1	1	1	0
2	1	1	1	0	0	1	1	1	1	1	1	1	1	1	1	0
<2	1	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1
X	1	1	0	0	?	0	1	0	1	0	1	0	1	0	1	?
>4	X	X	X	0	1	?	?	?	?	?	?	?	?	?	?	0
2<AIN<4	X	X	X	0	0	?	?	?	?	?	?	?	?	?	?	0
<2	X	X	X	0	0	?	?	?	?	?	?	?	?	?	?	1
X	X	X	X	1	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

Z – High Impedance; X – Don't Care; ? – Determined By AIN.

Also, a sleep mode feature is provided such that for STBY = HIGH and the clock disabled, the static power of the AD875 will drop below 50 mW. The AD875 reaches rated accuracy 4 clock cycles after STBY is brought LOW and the clock is started.

DIGITAL OUTPUTS

Each of the on-chip buffers for the AD875 output bits (D0–D9, OVR, UNR) is powered from the DRV_{DD} supply pins, separate from AV_{DD} or DV_{DD}. The output drivers are sized to handle a variety of logic families while minimizing the amount of glitch energy generated. In all cases, a fan-out of one is recommended to keep the capacitive load on the output data bits below the specified 20 pF level.

For DRV_{DD} = 5 V, the AD875 output signal swing is compatible with both high speed CMOS and TTL logic families. For TTL, the AD875 on-chip, output drivers were designed to support several of the high speed TTL families (F, AS, S). For applications where the clock rate is below 15 MHz, other TTL families may be appropriate. For interfacing with lower voltage CMOS logic, the AD875 sustains 15 MHz operation with DRV_{DD} = 3.3 V. In all cases, check your logic family data sheets for compatibility with the AD875 Digital Specification table.

THREE-STATE OUTPUTS

The digital outputs of the AD875 can be placed in a high impedance state by setting the THREE-STATE pin to HIGH. This feature is provided to facilitate in-circuit testing or evaluation. Note that this function is not intended for enabling/disabling the ADC outputs from a bus at 15 MHz. Also, to avoid corruption of the sampled analog signal during conversion (three clock cycles), it is highly recommended that the AD875 outputs be enabled on the bus prior to the first sampling. For the purpose of budgetary timing, the maximum access and float delay times (t_{DD}, t_{HL} shown in Figure 14) for the AD875 are 150 ns.

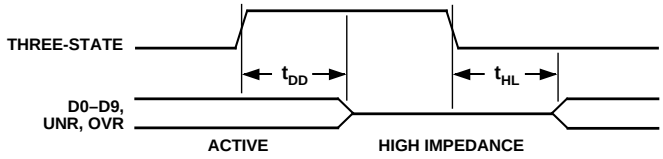


Figure 14. High Impedance Output Timing Diagram

OUT OF RANGE

As Table II indicates, an Underrange (UNR) or Overrange (OVR) condition exists when the analog input voltage is beyond the input range (nominally +2 V to +4 V) of the converter. UNR (Pin 46) is set LOW when the analog input voltage is within the analog input range. UNR is set HIGH (after accounting for pipeline latency) and will remain HIGH when the analog input voltage is less than the input range by 1/2 LSB from the center of the negative full-scale output code. OVR (Pin 47) is set LOW when the analog input voltage is within the analog input range. OVR is set HIGH (after accounting for pipeline latency) and will remain HIGH when the analog input voltage is greater than the input range by 1/2 LSB from the center of the positive full-scale output code.

GROUNDING AND LAYOUT RULES

As is the case for any high performance device, proper grounding and layout techniques are essential in achieving optimal performance. The analog and digital grounds on the AD875 have been separated to optimize the management of return currents in a system. It is recommended that a 4-layer printed circuit board (PCB) which employs a ground plane and power planes be used with the AD875. The use of ground and power planes offers distinct advantages:

1. The minimization of the loop area encompassed by a signal and its return path.
2. The minimization of the impedance associated with ground and power paths.
3. The inherent distributed capacitor formed by the power plane, PCB insulation, and ground plane.

These characteristics result in both a reduction of electromagnetic interference (EMI) and an overall improvement in performance.

It is important to design a layout which prevents noise from coupling onto the input signal. Digital signals should not be run in parallel with the input signal traces and should be routed away from the input circuitry.

Separate analog and digital grounds should be joined together directly under the AD875. A solid ground plane under the AD875 is also acceptable if care is taken in the management of the power and ground return currents. A general "rule-of-thumb" for mixed signal layouts dictates that the return currents from digital circuitry should not pass through critical analog circuitry.

POWER SUPPLY DECOUPLING

The analog and digital supplies of the AD875 have been separated to prevent the typically large transients associated with digital circuitry from coupling into the analog supply (AV_{DD}).

The digital supplies have also been separated into DRV_{DD} and DV_{DD}. The DRV_{DD} pins provide power for the digital I/Os of the AD875 and are likely to contain high energy transients. Each power supply pin should be decoupled with a 0.1 μF capacitor located as close to the pin as possible. For optimal performance, surface-mount capacitors are recommended. The inductance associated with the leads of through-hole ceramic capacitors typically render them ineffective at higher frequencies. A *complete* system will also incorporate tantalum capacitors in the 10 μF–100 μF range to decouple low frequency noise and ferrite beads to limit high frequency noise.

APPLICATIONS

IMAGING SYSTEM OVERVIEW

While the specifics of a particular imaging system will vary, most architectures will employ some or all of the building blocks shown in Figure 15. The image sensor, often a charged-coupled device (CCD), transforms light to electrical output. The resultant pixel stream is conditioned by a clamp/sample-hold circuit which is sometimes referred to as a correlated double sampler (CDS). A gain block sets signal levels which maximize the utilization of the dynamic range of the A/D converter. DC restoration is often used to remove any static dc errors which may accumulate over time and temperature. The digitized signal is then processed by the application specific digital signal processor.

For optimum performance the CDS is tailored to the sensor output characteristics. When used in conjunction with a CCD, the CDS acts to remove low frequency signal variations, kT/C noise, and other noise components, all of which are artifacts generated by the CCD. The output signal from the CCD is characterized by a series of pixels, each containing both a reset level and the actual video data. Aside from the various noise components, the video data is essentially a stream of stepped dc signals. This pixel stream from the CCD is then ac-coupled through a capacitor to a switch (contained within the CDS block).

This switch, in turn, is connected to a clamp reference voltage. The switch is closed during the reset portion of each pixel. As a result, the difference between the reset level of each pixel and the clamp reference voltage is stored on the coupling capacitor. When the switch is opened, the dc voltage stored on the coupling capacitor sets the dc level for the pixel stream. The video portion of each pixel is then sampled and held using traditional sample/hold (SHA) architectures. Since the CCD noise sources are correlated between the reset and video portions of the pixel stream, and the output of the SHA represents the difference between these two levels, the noise is effectively eliminated.

The output of the CDS will generally require some form of gain control in order to maximize the full-scale input range of the A/D converter. In some applications, a fixed gain may be adequate while in many applications such as camcorders, variable gain control is used to automatically account for variations in scene brightness. Gain control can be achieved using analog or digital techniques and often times must be able to respond at a rate equivalent to the pixel rate. Gilbert multiplier cells and multiplying D/As are two common circuits used for the gain block.

The dc restore block acts to set the final dc level of the signal before digitization by the A/D converter. A fixed voltage level (equivalent to the black level or negative full scale) generated by the CCD is sampled by the dc restoration circuit usually at the beginning or end of a "scan line." Any difference between the sampled black level and the desired negative full scale is removed either by a servo loop or corrected digitally. To maximize the use of the A/D's input range, the error must be removed prior to the A/D. This is generally accomplished by a high dc-gain feedback path which servos any error detected at the output. The dc restoration effectively removes dc level shifts which may occur as a result of long-term parameter shifts such as component drift and temperature variations.

The main criterion for choosing the A/D converter is generally based on resolution and speed. Resolution affects the signals-to-noise ratio of the system, dictates the maximum digital dynamic range of the image, and is a consideration for round-off errors produced in the digital signal processing. The speed of the A/D converter is related to the number of pixel elements and the pixel output rate of the particular image sensor. Multichannel systems may multiplex more than one pixel stream into a single A/D, thus requiring faster conversion rates. Similarly, area CCDs (CCDs which capture video information in two dimensions) operate at higher rates than linear (one dimensional) CCDs.

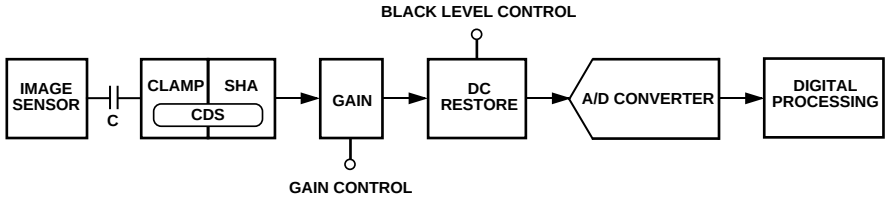


Figure 15. Typical Imaging System Block Diagram

MULTICHANNEL IMAGE ACQUISITION SYSTEM

The AD875's fast conversion rate combined with the AD783 sample/hold amplifiers (SHAs) and the AD9300 high speed multiplexer can be used to construct an analog front-end capable of acquiring and digitizing three or more analog signals at a rate of 1 MSPS. Figure 16 shows a typical circuit which employs three AD783s capable of acquiring a 2 V p-p step input to 10-bit accuracy in less than 350 ns.

Referring to the timing diagram in Figure 17, the three analog inputs are simultaneously sampled on the falling edge of S/H. After allowing the SHAs to settle (250 ns), the R channel is digitized at the conversion rate of 12 MHz (83.3 ns). Next, the MUX is switched to the G channel, allowed to settle (83.3 ns), and digitized. The B channel is digitized similarly. While the B channel is converted, the R channel data becomes available at the output of the AD875 (due to the pipelined latency). The rising edges of the signals RDAV, GDAV, and BDAV are the signals which indicate when valid data is available at the output of the A/D converter.

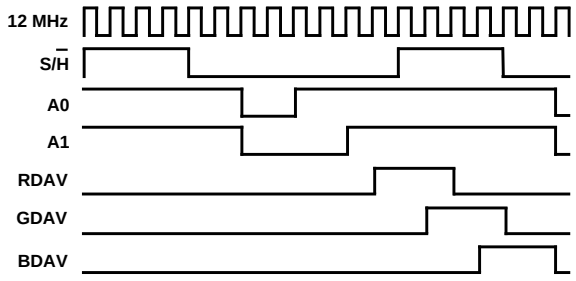


Figure 17. Timing Diagram for Figure 16

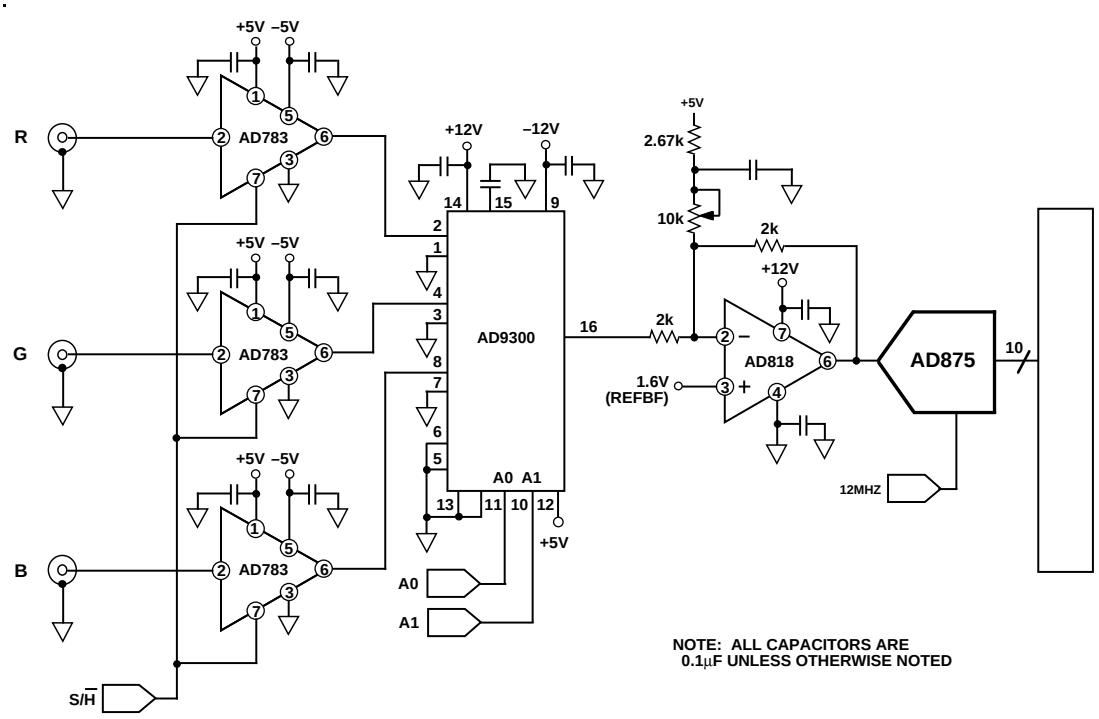


Figure 16. Multichannel Image Acquisition System

HIGH SPEED SAMPLE-AND-HOLD AMPLIFIER (SHA)

A sample-hold amplifier is often needed as part of a correlated double sampler or when high bandwidth inputs such as video signals are to be converted by the AD875. For fast, precise sampling required for video signals, an integrated solution such as the AD9101 track-and-hold amplifier is suggested for optimum performance. However, the requirements of many 10-bit imaging systems can be achieved using a SHA architecture similar to the one shown in Figure 18. This discrete SHA can accurately acquire a 1 V input step within 1 mV accuracy in less than 200 ns. Hold-mode settling within 1 mV is typically less than 50 ns. The resultant throughput rate is 3.3 MSPS.

CIRCUIT DESCRIPTION

The discrete SHA shown in Figure 13 is a closed-loop, noninverting architecture that accepts 1 V p-p inputs. The overall gain of the SHA is +2 in order to accommodate the 2 V input span of the AD875. The AD847, with 0.1% settling time of 65 ns, is the suggested input buffer to the SHA. The circuit also employs an SD5001 that contains four ultrahigh speed DMOS switches (Q1–Q4). The low cost, fast settling time and high CMRR of the AD817 op amp are critical features necessary for optimal performance and economy.

In sample mode, Q1 and Q3 of the SD5001 are closed (Q2 and Q4 are open). C28 is charged to the input voltage level at a rate primarily determined by the time constant, R9 × C28, and the gain (2×). Simultaneously, C29 is connected to ground through a 250 Ω resistor. If C28 is equal to C29, charge injection from Q1 will be approximately equal to charge injection form Q3 based on the symmetry of the circuit and the inherent matching of the switch capacitance. The resultant pedestal errors appear as a common-mode signal to the AD817 and are approximately canceled from the differential architecture.

In hold mode, Q2 and Q4 are closed (Q1 and Q3 are open) to reduce feedthrough. The AD817 buffers the voltage held on C28 and settles within the requisite 1 mV within 50 ns. The output of the AD817 must then be level-shifted in order to interface with the AD875 input span requirements. Throughput rates greater than 3.3 MSPS using this architecture are limited by the R_{ON} of the SD5001. Faster sample rates require open-loop architectures or diode-bridge switching in order to reduce the on-resistance.

TIMING DESCRIPTION

Figure 19 shows the timing requirements for the discrete SHA. The complementary S/$\overline{H}$ inputs are HCMOS-compatible although larger gate voltages will improve performance slightly by lowering the on resistances of the DMOS switches. The conversion is started as soon as the output of the SHA has settled within 16 mV of its final value.

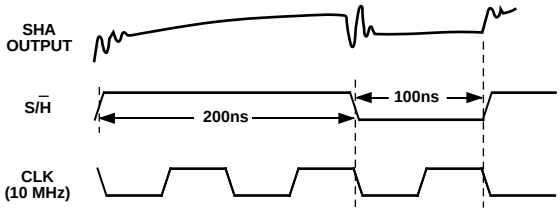


Figure 19. Timing Diagram for Discrete SHA

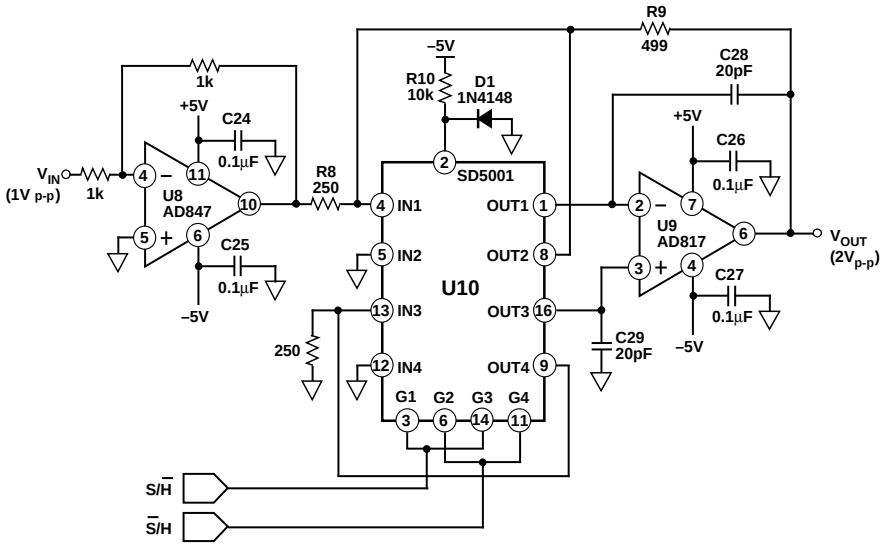


Figure 18. High Speed Discrete SHA

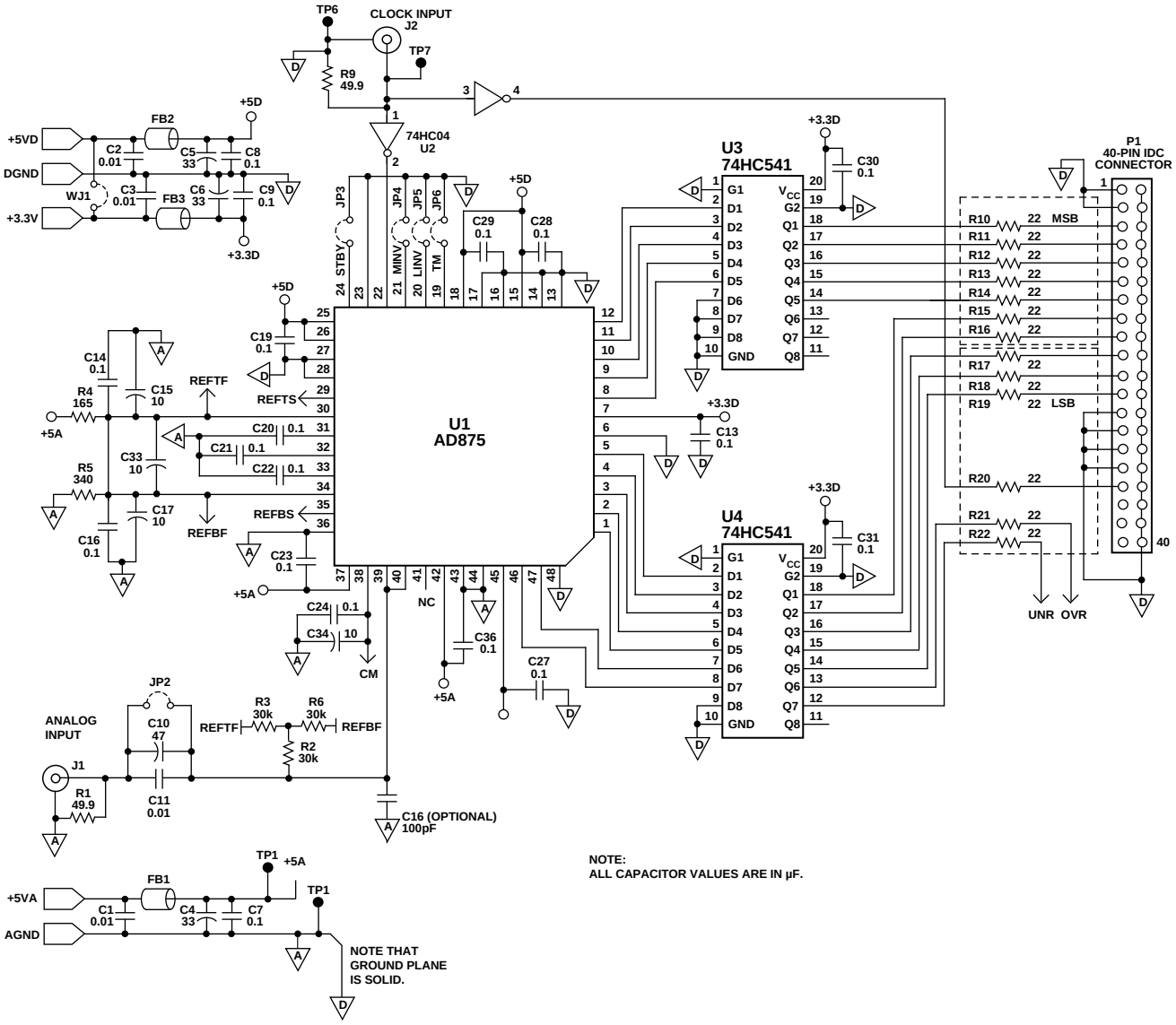


Figure 20. AD875 Evaluation Board Schematic

Table III. Components List

Reference Designator	Description	Quantity
U1	AD875	1
U2	74HC04	1
U3, U4	74HC541	2
R1, R9	Resistor, 51 Ω	2
R2, R3, R6	Resistor, 30 kΩ	3
R4	Resistor, 165 Ω	1
R5	Resistor, 340 Ω	1
R10–R22	Resistor, 22 Ω Resistor Network	1
C10	Capacitor, Electrolytic, 47 µF	1
C11	Capacitor, NPO Ceramic, 0.01 µF	1
C15, C17, C33	Capacitor, Electrolytic, 10 µF	3
C13, C14, C16, C19, C23, C24, C31 C27, C28, C30, C31, C35, C36	Capacitor, X7R Ceramic, 0.1 µF	12
P1	40-Pin IDC Connector	1
J1, J2	BNC Jack	2

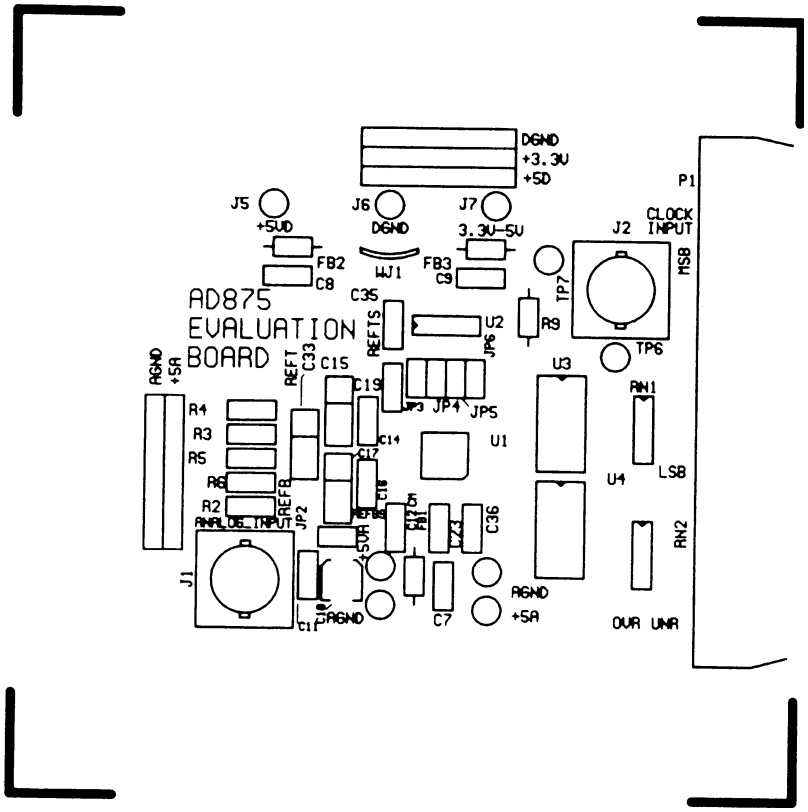


Figure 21. Silkscreen Layer, Component Side PCB Layout

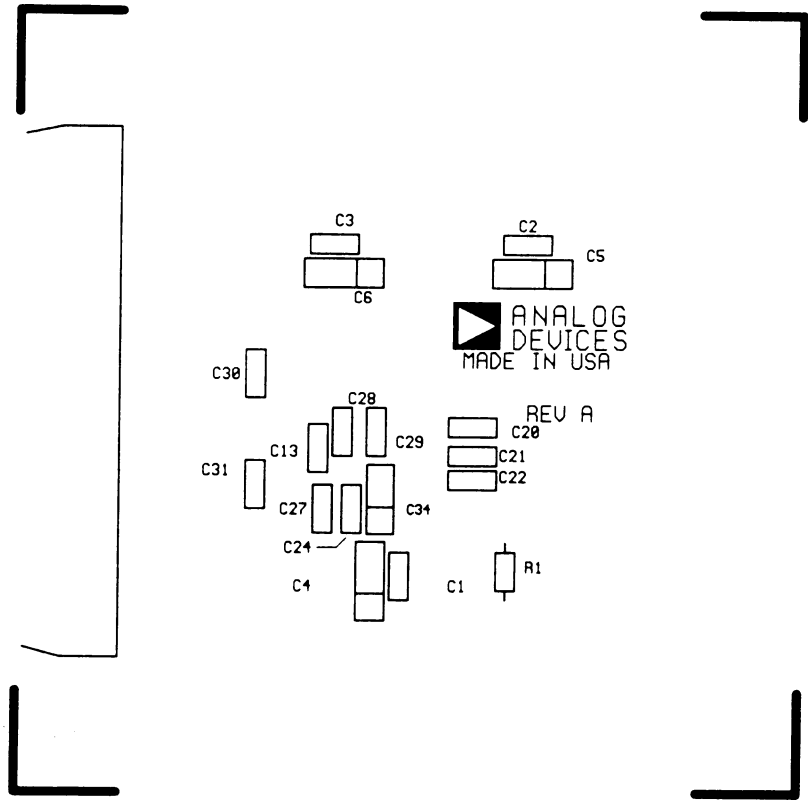


Figure 22. Silkscreen Layer, Circuit Side PCB Layout

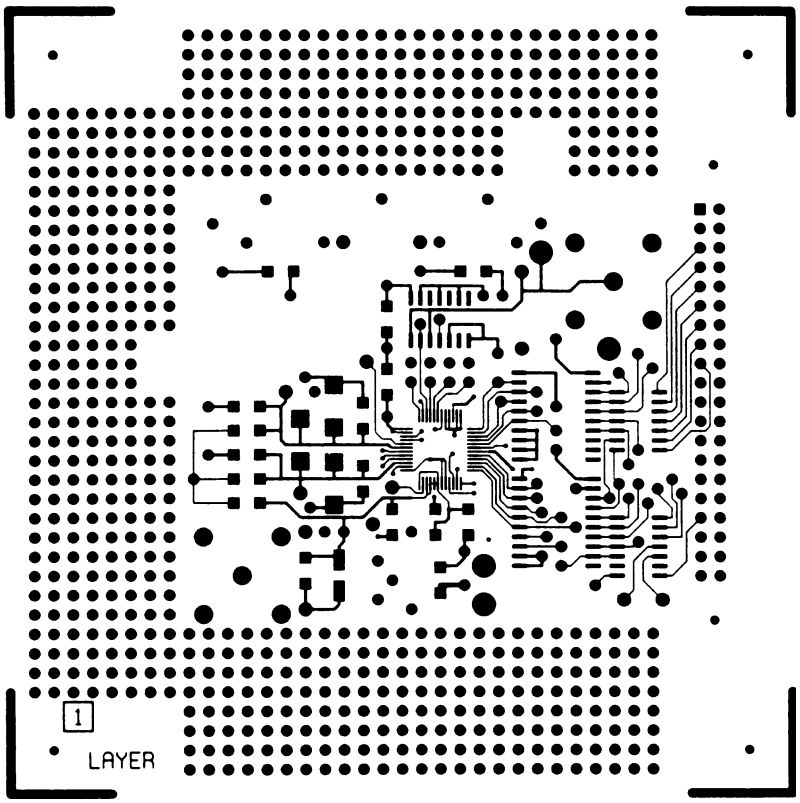


Figure 23. Component Side PCB Layout

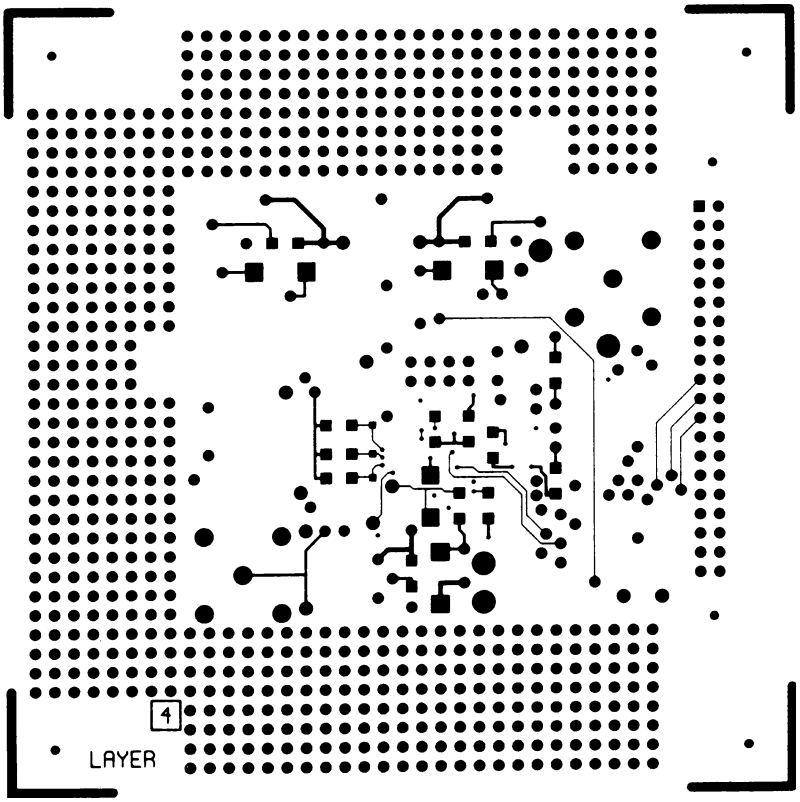


Figure 24. Circuit Side PCB Layout

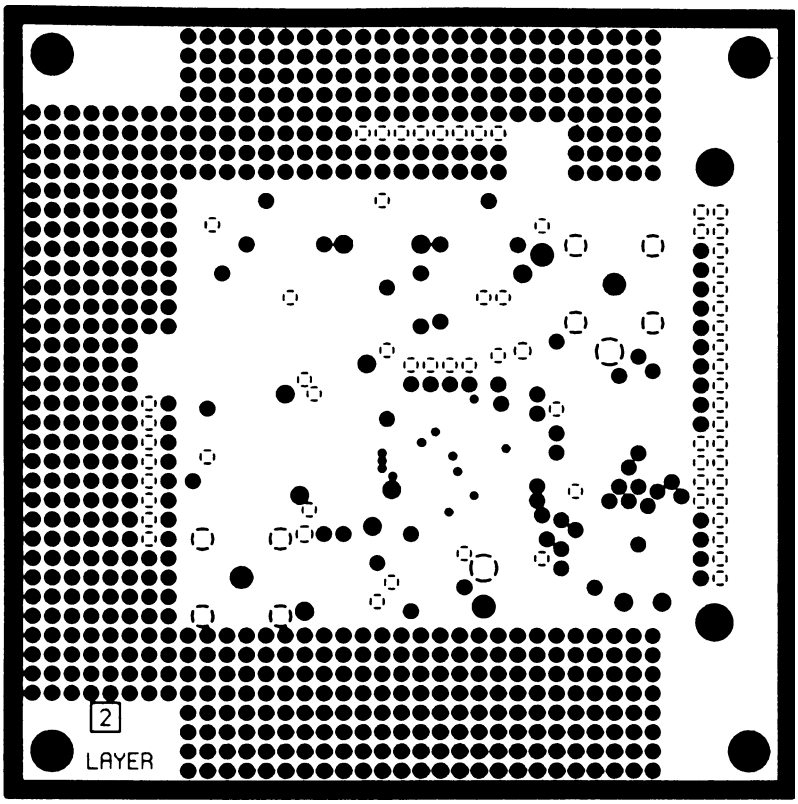


Figure 25. Ground Layer PCB Layout

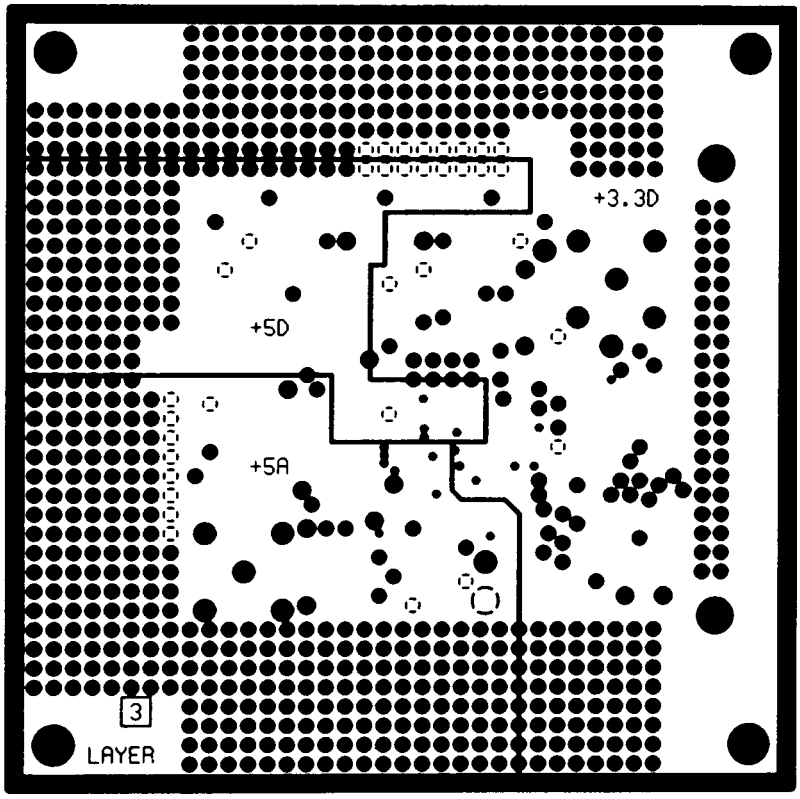
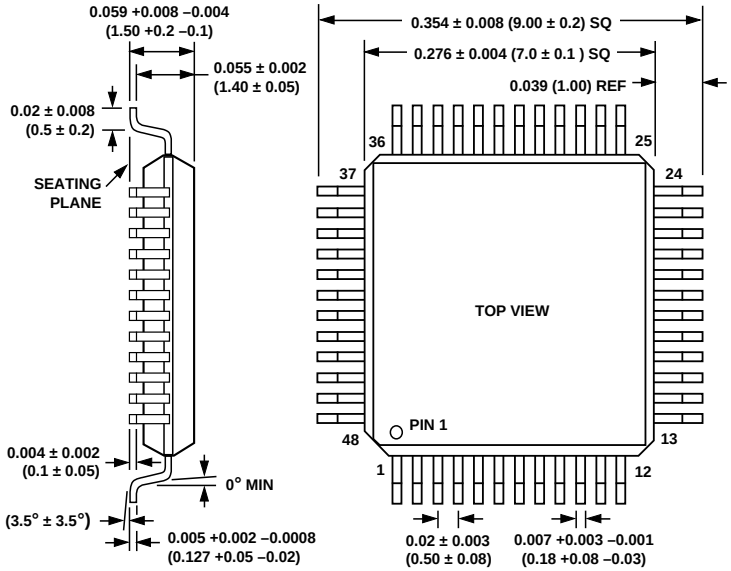


Figure 26. Power Layer PCB Layout

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

TQFP



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