

TOSHIBA BIPOLAR DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

**ULN2003AP, ULN2003AFW, ULN2004AP, ULN2004AFW**

**7CH DARLINGTON SINK DRIVER**

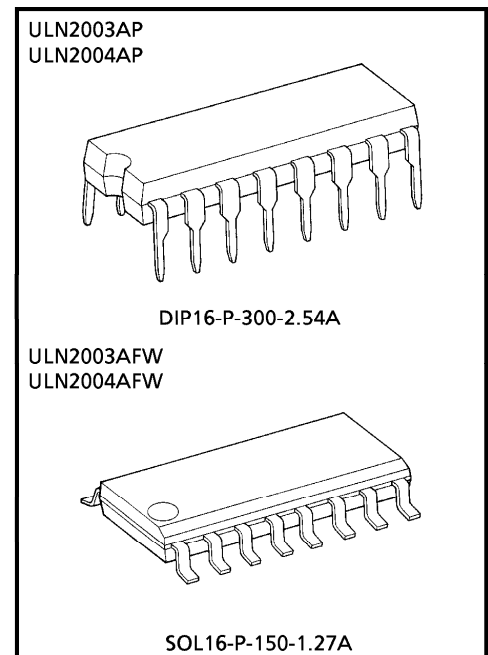
The ULN2003AP / AFW Series are high-voltage, high-current darlington drivers comprised of seven NPN darlington pairs.

All units feature integral clamp diodes for switching inductive loads.

Applications include relay, hammer, lamp and display (LED) drivers.

**FEATURES**

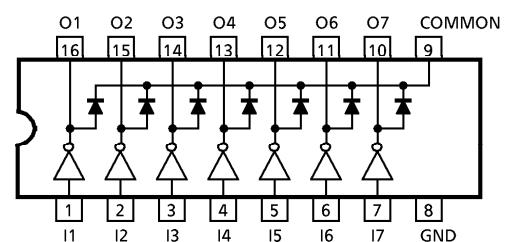
- Output current (single output) 500 mA MAX.
- High sustaining voltage output  
50 V MIN. (ULN2003AP / AFW Series)
- Output clamp diodes
- Inputs compatible with various types of logic
- Package Type-AP : DIP-16pin
- Package Type-AFW : SOL-16pin



**Weight**  
 DIP16-P-300-2.54A : 1.11 g (Typ.)  
 SOL16-P-150-1.27A : 0.15 g (Typ.)

TYPE	INPUT BASE RESISTOR	DESIGNATION
ULN2003AP / AFW	2.7 kΩ	TTL, 5 V CMOS
ULN2004AP / AFW	10.5 kΩ	6~15 V PMOS, CMOS

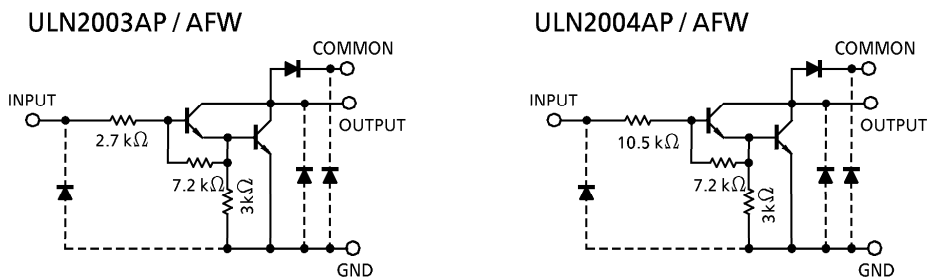
**PIN CONNECTION (TOP VIEW)**



980910EBA1

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**SCHEMATICS (EACH DRIVER)**



(Note) : The input and output parasitic diodes cannot be used as clamp diodes.

**MAXIMUM RATINGS (Ta = 25°C)**

CHARACTERISTIC	SYMBOL	RATING	UNIT
Output Sustaining Voltage	$V_{CE(SUS)}$	-0.5~50	V
Output Current	$I_{OUT}$	500	mA / ch
Input Voltage	$V_{IN}$	-0.5~30	V
Clamp Diode Reverse Voltage	$V_R$	50	V
Clamp Diode Forward Current	$I_F$	500	mA
Power Dissipation	AP	1.47	W
	AFW	0.54 / 0.625 (Note)	
Operating Temperature	$T_{opr}$	-40~85	°C
Storage Temperature	$T_{stg}$	-55~150	°C

(Note) : On glass epoxy PCB (30 × 30 × 1.6 mm Cu 50%)

**RECOMMENDED OPERATING CONDITIONS (Ta = -40~85°C)**

CHARACTERISTIC		SYMBOL	CONDITION		MIN.	TYP.	MAX.	UNIT
Output Sustaining Voltage		V <sub>CE (SUS)</sub>			0	—	50	V
Output Current	AP	I <sub>OUT</sub>	T <sub>pw</sub> = 25 ms 7 Circuits Ta = 85°C Tj = 120°C	Duty = 10%	0	—	370	mA / ch
	AFW			Duty = 50%	0	—	130	
				Duty = 10%	0	—	233	
				Duty = 50%	0	—	70	
Input Voltage		V <sub>IN</sub>			0	—	24	V
Input Voltage (Output On)	ULN2003A	V <sub>IN (ON)</sub>	I <sub>OUT</sub> = 400 mA h <sub>FE</sub> = 800		2.8	—	24	V
	ULN2004A				6.2	—	24	
Input Voltage (Output Off)	ULN2003A	V <sub>IN (OFF)</sub>			0	—	0.7	V
	ULN2004A				0	—	1.0	
Clamp Diode Reverse Voltage		V <sub>R</sub>			—	—	50	V
Clamp Diode Forward Current		I <sub>F</sub>			—	—	350	mA
Power Dissipation	AP	P <sub>D</sub>	Ta = 85°C		—	—	0.76	W
	AFW		(Note) Ta = 85°C		—	—	0.325	

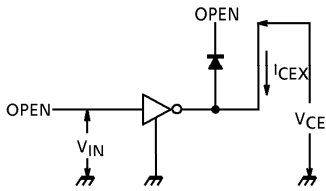
(Note) : On glass epoxy PCB (30 × 30 × 1.6 mm Cu 50%)

**ELECTRICAL CHARACTERISTICS** (Ta = 25°C unless otherwise noted)

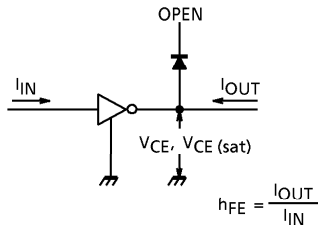
CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Output Leakage Current	I <sub>CEX</sub>	1	V <sub>CE</sub> = 50 V, Ta = 25°C	—	—	50	μA	
			V <sub>CE</sub> = 50 V, Ta = 85°C	—	—	100		
Collector-Emitter Saturation Voltage	V <sub>CE (sat)</sub>	2	I <sub>OUT</sub> = 350 mA, I <sub>IN</sub> = 500 μA	—	1.3	1.6	V	
			I <sub>OUT</sub> = 200 mA, I <sub>IN</sub> = 350 μA	—	1.1	1.3		
			I <sub>OUT</sub> = 100 mA, I <sub>IN</sub> = 250 μA	—	0.9	1.1		
DC Current Transfer Ratio	h <sub>FE</sub>	2	V <sub>CE</sub> = 2 V, I <sub>OUT</sub> = 350 mA	1000	—	—		
Input Current (Output On)	ULN2003A	3	V <sub>IN</sub> = 2.4 V, I <sub>OUT</sub> = 350 mA	—	0.4	0.7	mA	
	ULN2004A							V <sub>IN</sub> = 9.5 V, I <sub>OUT</sub> = 350 mA
Input Current (Output Off)	I <sub>IN (OFF)</sub>	4	I <sub>OUT</sub> = 500 μA, Ta = 85°C	50	65	—	μA	
Input Voltage (Output On)	ULN2003A	5	V <sub>CE</sub> = 2 V h <sub>FE</sub> = 800	I <sub>OUT</sub> = 350 mA	—	—	2.6	V
				I <sub>OUT</sub> = 200 mA	—	—	2.0	
	ULN2004A			I <sub>OUT</sub> = 350 mA	—	—	4.7	
				I <sub>OUT</sub> = 200 mA	—	—	4.4	
Clamp Diode Reverse Current	I <sub>R</sub>	6	V <sub>R</sub> = 50 V, Ta = 25°C	—	—	50	μA	
			V <sub>R</sub> = 50 V, Ta = 85°C	—	—	100		
Clamp Diode Forward Voltage	V <sub>F</sub>	7	I <sub>F</sub> = 350 mA	—	—	2.0	V	
Input Capacitance	C <sub>IN</sub>	—		—	15	—	pF	
Turn-On Delay	t <sub>ON</sub>	8	V <sub>OUT</sub> = 50 V, R <sub>L</sub> = 125 Ω C <sub>L</sub> = 15 pF	—	0.1	—	μs	
Turn-Off Delay	t <sub>OFF</sub>	8	V <sub>OUT</sub> = 50 V, R <sub>L</sub> = 125 Ω C <sub>L</sub> = 15 pF	—	0.2	—		

**TEST CIRCUIT**

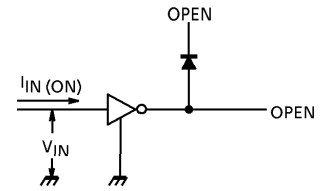
1.  $I_{CEX}$



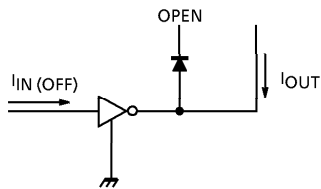
2.  $V_{CE} (sat), h_{FE}$



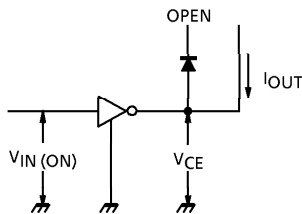
3.  $I_{IN} (ON)$



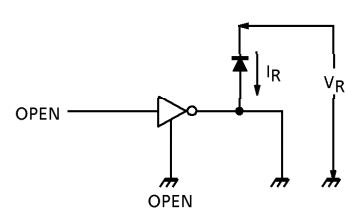
4.  $I_{IN} (OFF)$



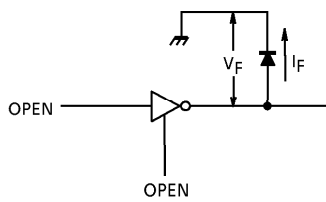
5.  $V_{IN} (ON)$



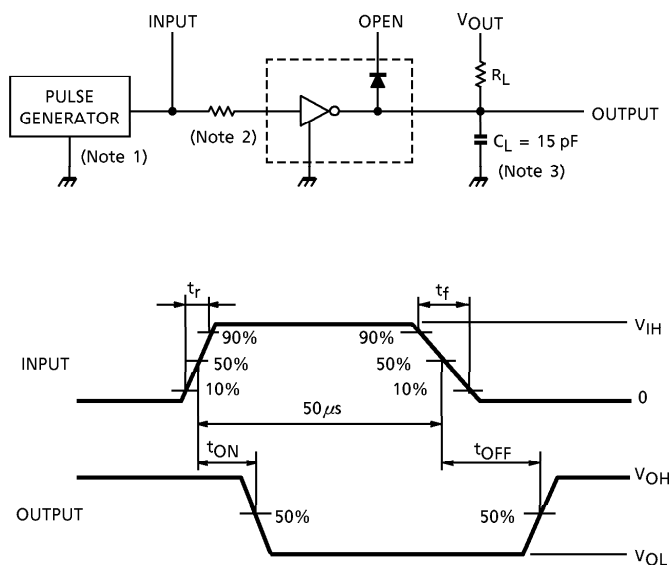
6.  $I_R$



7.  $V_F$



8.  $t_{ON}$ ,  $t_{OFF}$



- (Note 1) : Pulse width 50  $\mu$ s, duty cycle 10%  
Output impedance 50  $\Omega$ ,  $t_r \leq 5$  ns,  $t_f \leq 10$  ns
- (Note 2) : See below

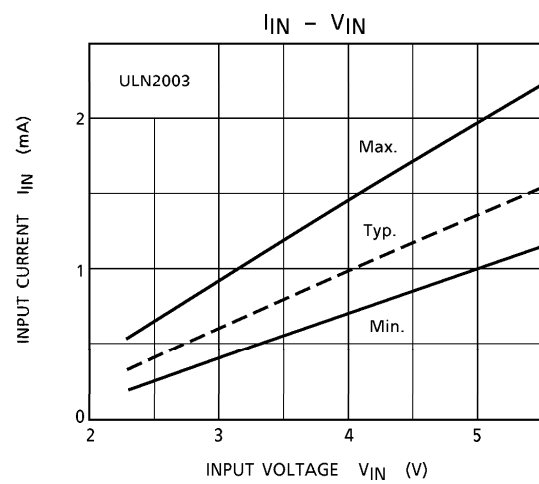
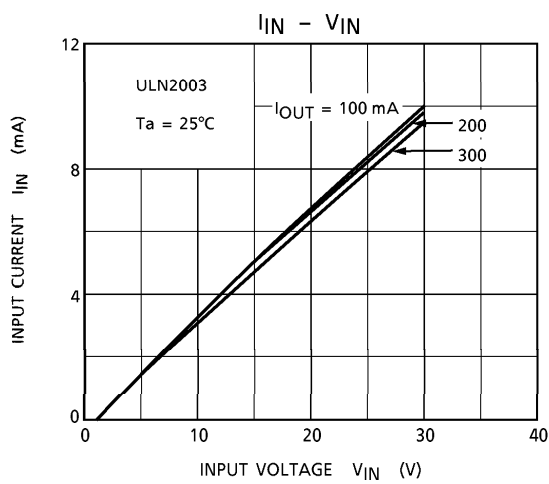
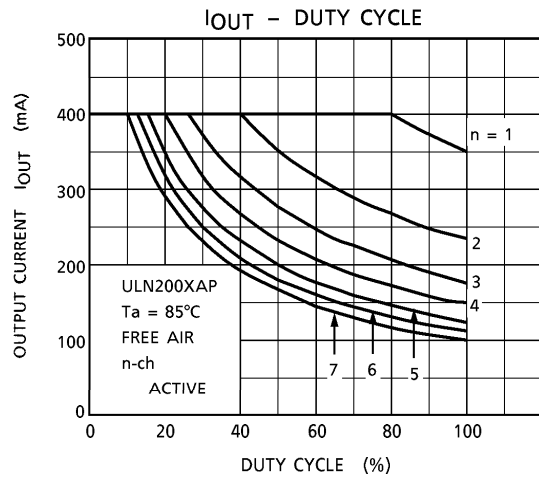
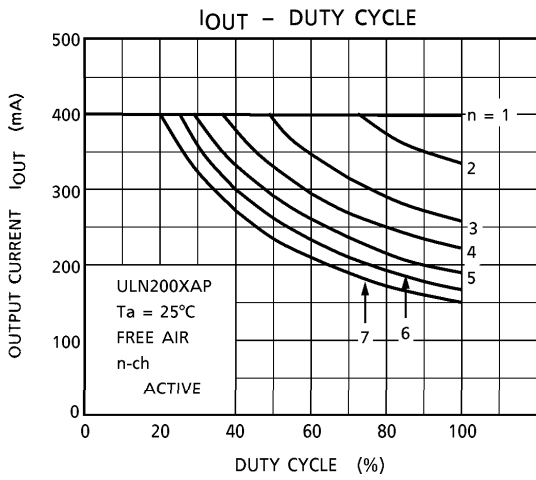
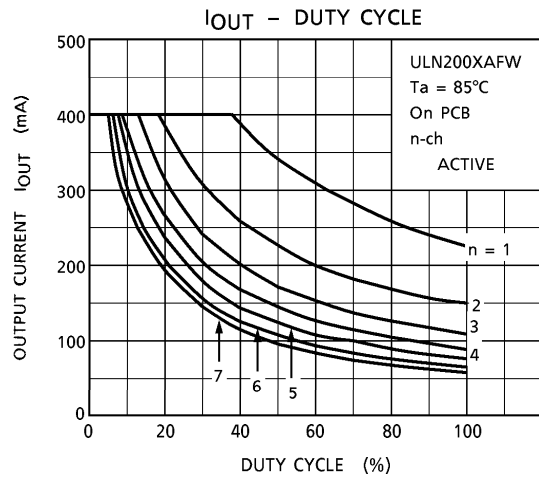
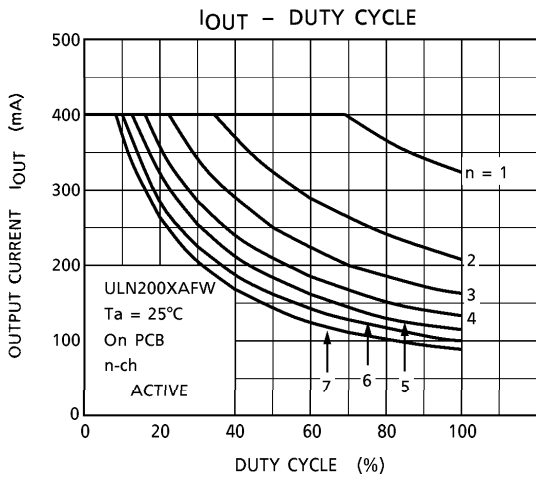
INPUT CONDITION

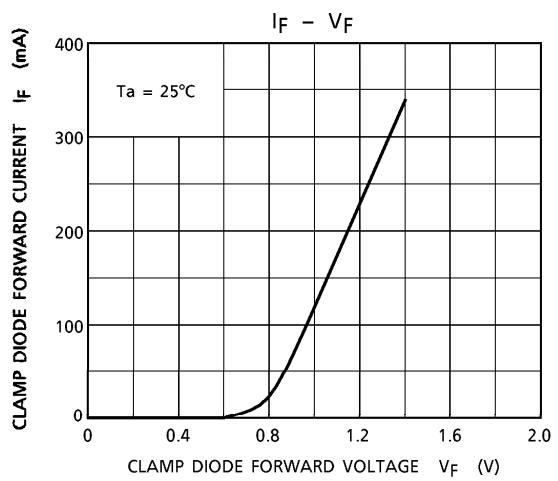
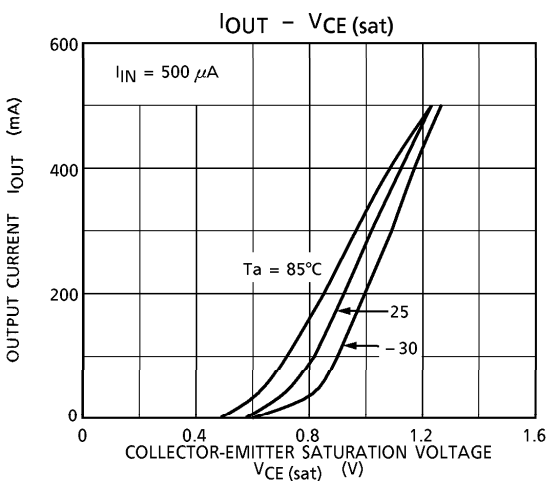
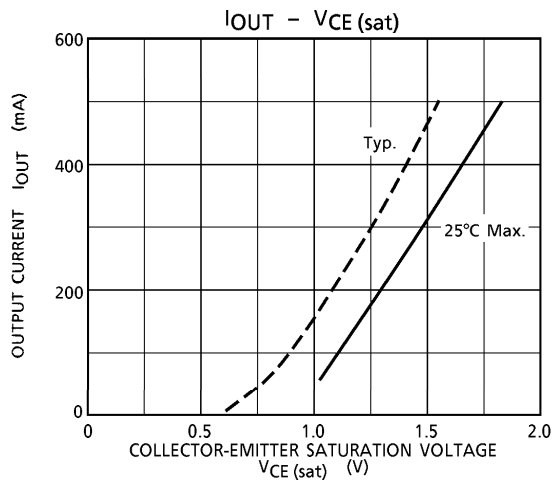
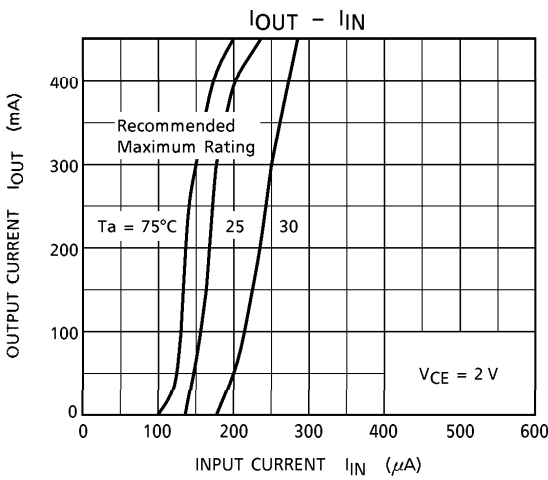
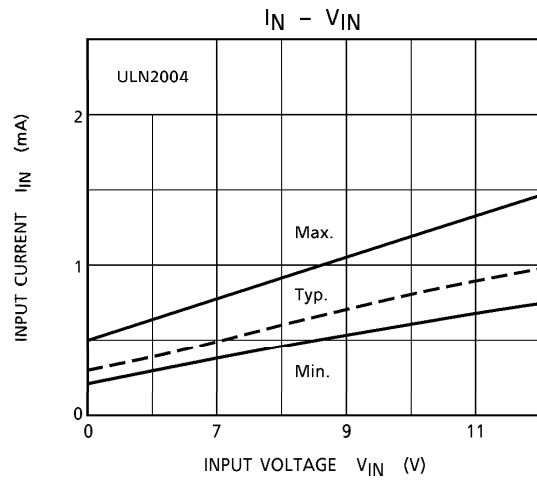
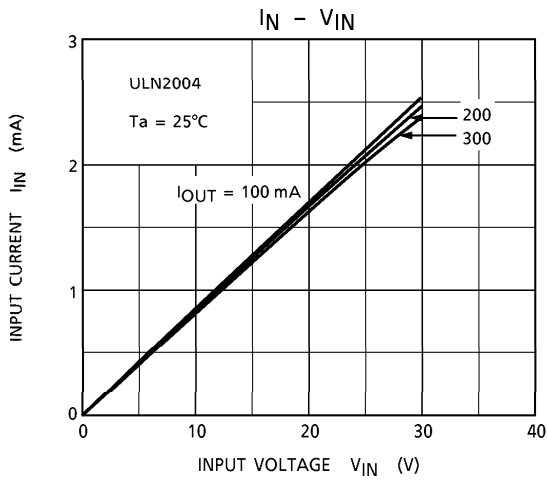
TYPE NUMBER	R1	$V_{IH}$
ULN2003AP / AFW	0	3 V
ULN2004AP / AFW	0	8 V

- (Note 3) :  $C_L$  includes probe and jig capacitance.

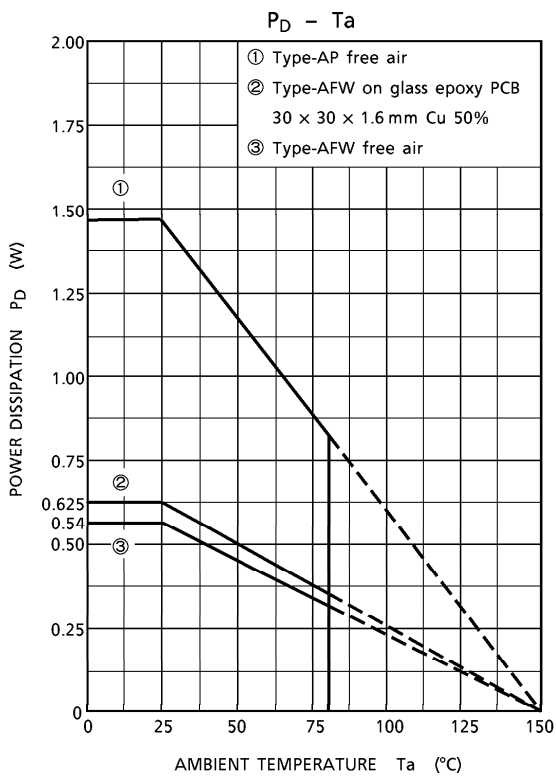
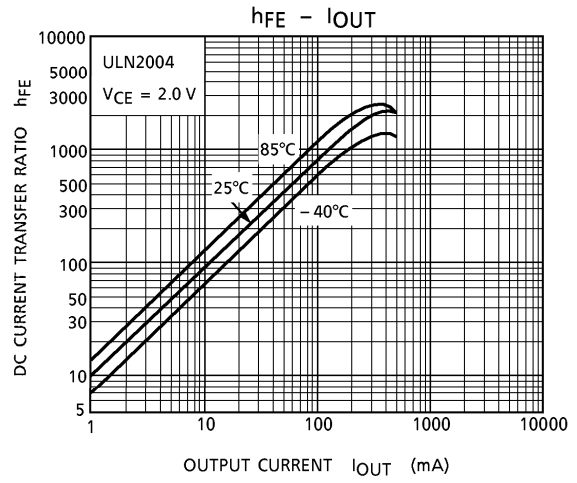
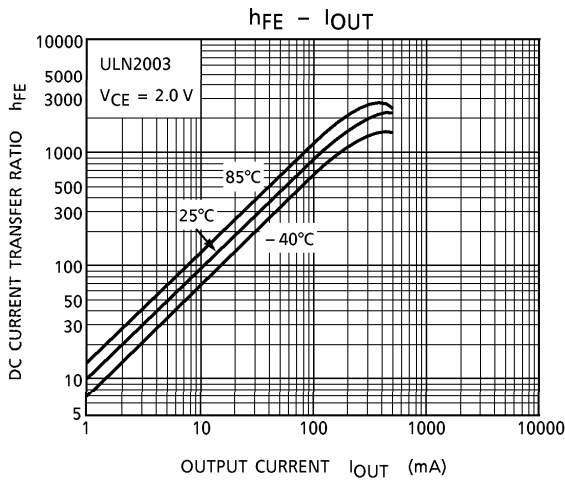
PRECAUTIONS for USING

Utmost care is necessary in the design of the output line, COMMON and GND line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.

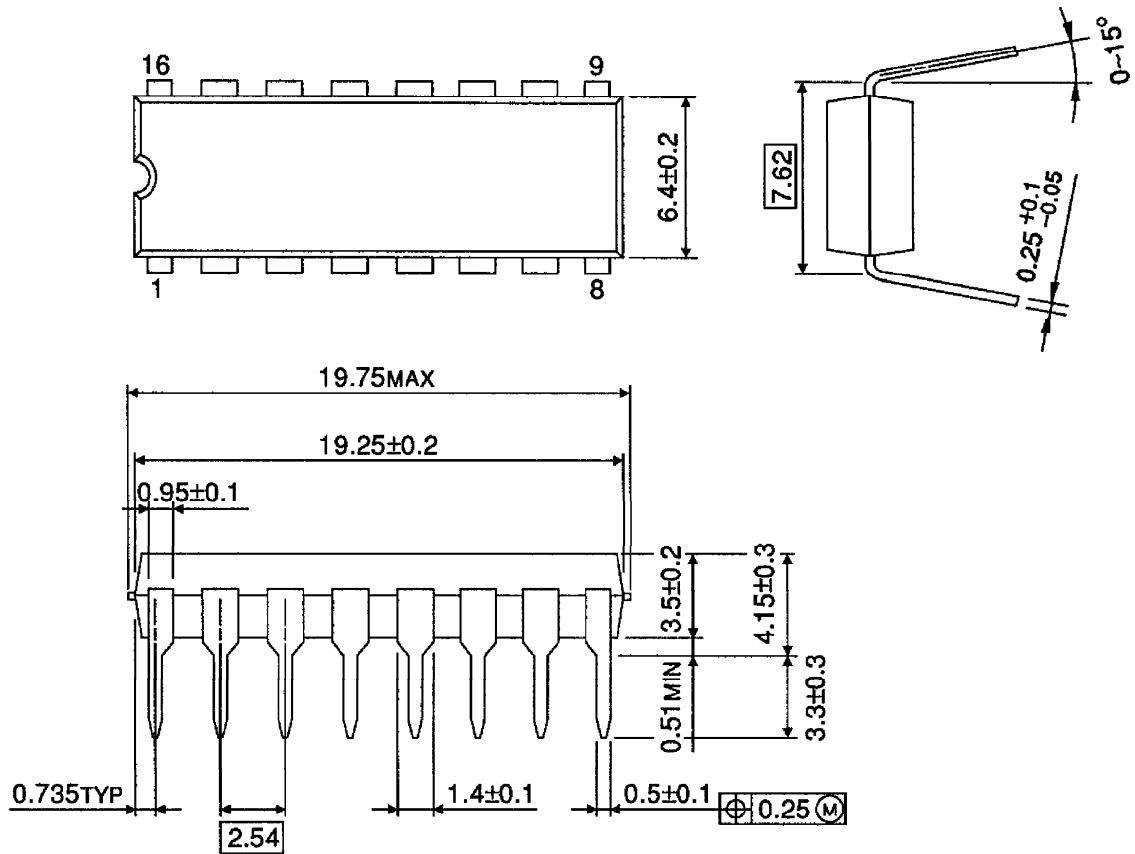








**OUTLINE DRAWING**  
DIP16-P-300-2.54A



Weight : 1.11 g (Typ.)

