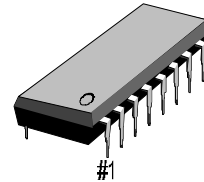


## OVERVIEW

The S5D2508A01 is used to display some characters or symbols on a screen of monitor. Basically, the operation is to control the internal memory on chip and generate the R,G,B signals for some characters or symbols. The R,G,B signals are synchronized with the horizontal sync. Then the R,G,B signals are mixed with the main video signal in the Video Amp IC.

The font data for characters or symbols are stored in the internal ROM. This stored data are accessed and controlled by the control data from a micro controller. The control data are transmitted through the I<sup>2</sup>C bus. All timing control signals including the system clock are synchronized with the horizontal sync. Therefore there is a PLL circuitry on chip.

16-DIP-300



## FEATURES

- 256 ROM fonts (Each font consists of 12 x 18 dots.)
- Full Screen Memory Architecture
- Wide range PLL available (15 kHz — 120 kHz)
- Programmable vertical height of character
- Programmable vertical and horizontal positioning
- Character color selection up to 16 different colors
- Programmable background color (Up to 16 colors)
- Character blinking, bordering and shadowing
- Color blinking
- Character scrolling
- Fade-in and fade-out
- Box drawing
- Character sizing up to four times
- 96 MHz pixel frequency from on-chip PLL
- IIC Protocol Data Transmission (Slave Address : BAH)

## ORDERING INFORMATION

Device	Package	Operating Temperature
S5D2508A01-D0B0	16-DIP-300	0°C — 70°C

BLOCK DIAGRAM

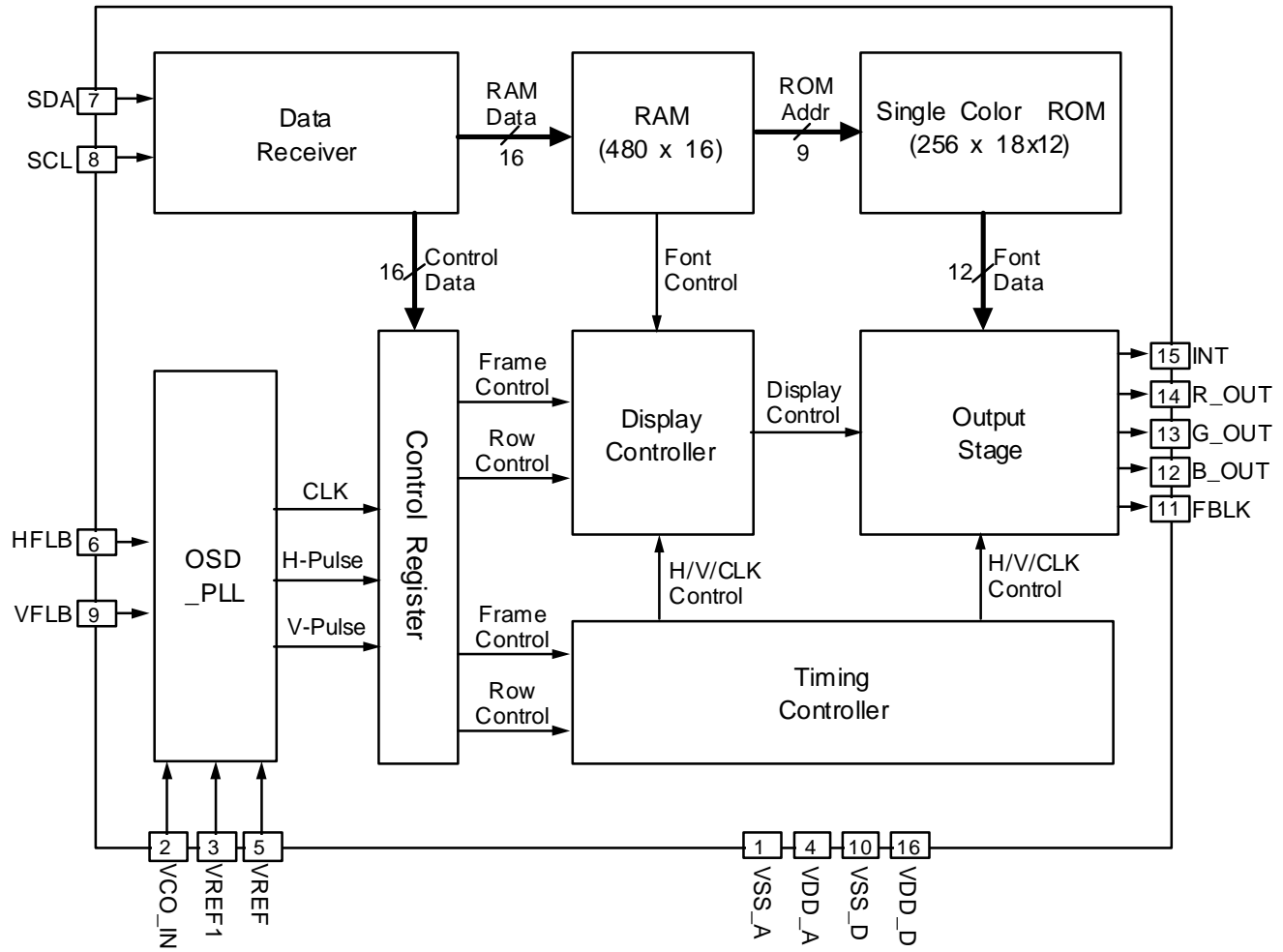


Figure 1. Functional Block Diagram

## PIN CONFIGURATIONS

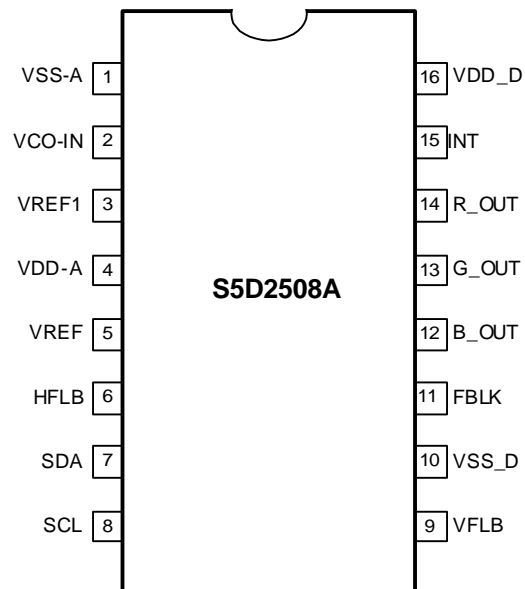


Figure 2. Pin Configurations

## PIN DESCRIPTIONS

Table 1. Pin Descriptions

Pin No.	Signal	Active	I/O	Description
1	VSS_A	-	-	Ground (Analog Part)
2	VCO_IN	-	Input	This voltage is generated at the external loop filter and goes into the input stage of the VCO.
3	VREF1	-	Input	1.26 V DC Voltage from the Bandgap Reference. Connected to ground through a resistor to make internal reference current (Typical 36 K $\Omega$ for 27 $\mu$ A)
4	VDD_A	-	-	+5 V Supply Voltage for Analog Part
5	VREF	-	Input	Bandgap Reference Voltage (Typical 1.26 V)
6	HFLB	Low	Input	Horizontal Flyback Signal
7	SDA	-	In/Out	Serial Data (I <sup>2</sup> C)
8	SCL	-	In/Out	Serial Clock (I <sup>2</sup> C)
9	VFLB	Low	Input	Vertical Flyback Signal
10	VSS_D	-	-	Ground for Digital Part
11	FBLK	-	Output	Fast Blank Signal
12	B_OUT	-	Output	Video Signal Output (B)
13	G_OUT	-	Output	Video Signal Output (G)
14	R_OUT	-	Output	Video Signal Output (R)
15	INT	-	Output	Intensity Signal Output
16	VDD_D	-	-	+5 V SUpply Voltage for Dogital Part

**ABSOLUTE MAXIMUM RATINGS**

Parameters	Symbol	Value			Unit
		Min.	Typ.	Max.	
Maximum Supply Voltage	VDD	-	-	7.0	V
Input Voltage	V <sub>I</sub>	-	-	7.0	V
Operating Temperature Range	T <sub>OPR</sub>	-20	-	70	°C
Storage Temperature Range	T <sub>STG</sub>	-40		125	°C
Power Dissipation	P <sub>D</sub>	-	-	1200	mW

**NOTE:** PKG Thermal Resistance : 64.2 °C/W

**ELECTRICAL CHARACTERISTICS****DC Electrical Characteristics**

(T<sub>a</sub> = 25 °C, VDD = 5 V)

**Table 2. DC Electrical Characteristics**

Parameters (Conditions)	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	VDD	4.75	5.00	5.25	V
Supply Current (No load on any output)	I <sub>DD</sub>	-	-	25	mA
Input Voltage	V <sub>IH</sub>	0.8VDD	-	-	V
	V <sub>IL</sub>	-	-	VSS + 0.4	V
Output Voltage (I <sub>out</sub> = 1mA)	V <sub>OH</sub>	0.8VDD	-	-	V
	V <sub>OL</sub>	-	-	VSS + 0.4	V
Input Leakage Current	I <sub>IL</sub>	-10	-	10	μA
VCO Input Voltage	V <sub>VCO</sub>		2.5		V

## OPERATION TIMINGS

Table 3. Operation Timings

Parameters (Conditions)	Symbol	Min.	Typ.	Max.	Unit
<b>Output Signal - R/G/B_OUT, INT, FBLK</b> ( $T_a = 25^\circ\text{C}$ , $V_{DDA} = V_{DD} = 5\text{ V}$ , $C_{LOAD} = 30\text{pF}$ )					
Rise Time	$t_R$	-	-	6	nsec
Fall Time	$t_F$	-	-	6	nsec
<b>Input Signal - HFLB, VFLB</b>					
Horizontal Flyback Signal Frequency	$f_{HFLB}$	-	-	120	kHz
Vertical Flyback Signal Frequency	$f_{VFLB}$	-	-	200	Hz
<b>I<sup>2</sup>C Interface - SDA, SCL</b> (Refer to Figure 3)					
SCL Clock Frequency	$f_{SCL}$	-	-	300	kHz
Hold Time for start condition	$t_{hs}$	500	-	-	ns
Set Up Time for stop condition	$t_{sus}$	500	-	-	ns
Low Duration of clock	$t_{low}$	400	-	-	ns
High Duration of clock	$t_{high}$	400	-	-	ns
Hold Time for data	$t_{hd}$	0	-	-	ns
Set Up Time for data	$t_{sud}$	500	-	-	ns
Time between 2 access	$t_{ss}$	500	-	-	ns
Fall Time of SDA	$t_{fSDA}$	-	-	20	ns
Rise Time of both SCL and SDA	$t_{rSDA}$	-	-	-	ns

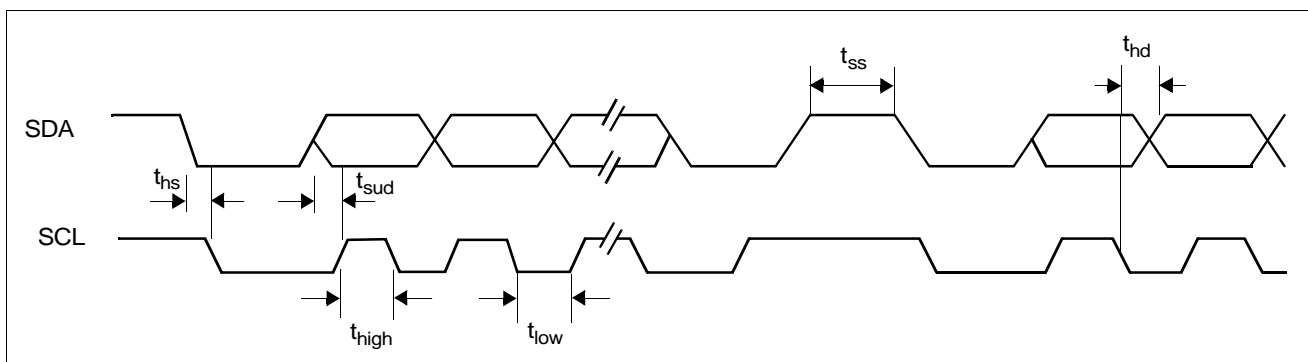


Figure 3. I<sup>2</sup>C Bus Timing Diagram

**FUNCTIONAL DESCRIPTIONS**

**Data Transmission to the S5D2508A01**

According to the I<sup>2</sup>C protocol, the S5D2508A01 receives the data from a micro controller. The SDA line and the SCL line are shown in Figure 4. As shown in Figure 4, after the starting pulse, the slave address with R/W\* bit and an acknowledge are transmitted in sequence, an internal register address of the S5D2508A01 is followed. The first 8-bit byte is the upper 8bits of the register address. The lower 8bits of the register address are followed after the second acknowledge. There is a data transmission format and are two address bit patterns in the S5D2508A01 as following.

The slave address of the S5D2508A01 is BAH(in hexadecimal).

**Data Transmission Format**

Row Address -> Column Address -> Data Byte N -> Data Byte N+1 -> Data Byte N+2 -> ....

**Address Bit Pattern for Display Registers Data**

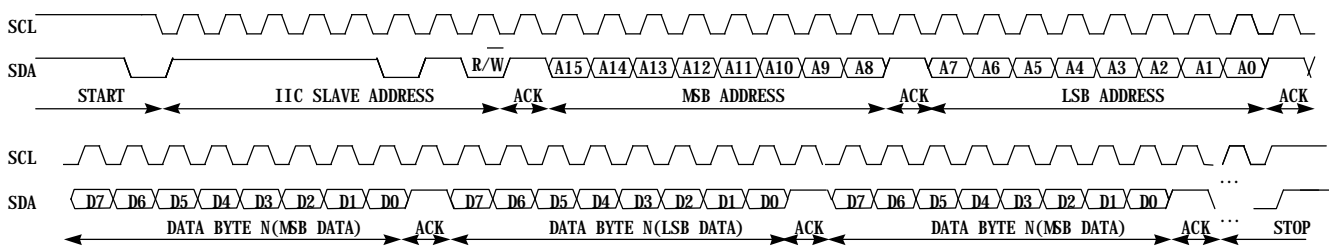
(a) Row Address Bit Pattern                      R3 - R0: Valid Data for Row Address

A15	A14	A13	A12	A11	A10	A9	A8
X	X	X	X	R3	R2	R1	R0

(b) Column Address Bit Pattern                      C4 - C0: Valid Data for Column Address

A7	A6	A5	A4	A3	A2	A1	A0
X	X	X	C4	C3	C2	C1	C0

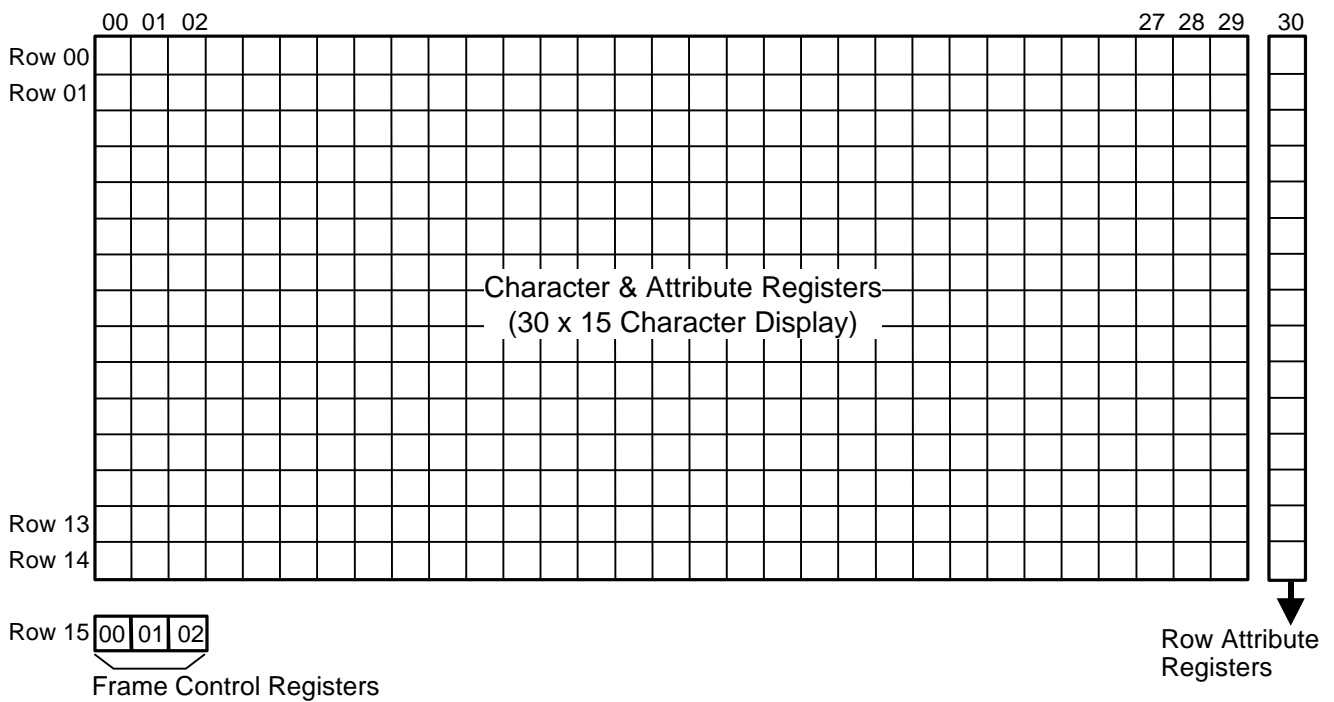
After addressing, data bytes are followed as the above data transmission format. The Figure 4 describes the data transmission with the I<sup>2</sup>C bus protocol.



**Figure 4. SDA line and SCL line (Write Operation)**

**Memory Map**

The display RAM is addressed with the row and column number in sequence. The display RAM consists of four register groups: Character & Attribute Registers, Row Attribute Registers and Frame Control Registers-. As the display area in a monitor screen is 30 columns by 15 rows, the related Character & Attribute Registers are also 30 columns by 15 rows. Each register contains a character address and an attribute corresponding to display location on a monitor screen. And one register is composed of 16 bits. The lower 8 bits select characters out of 256 ROM fonts. The upper 7 bits are assigned to give a character attribute to a selected font. Row Attribute Registers occupy the 31th column of Display RAM and provide the row attribute of a blank mode, raster color, raster color intensity, character color intensity, horizontal character size, vertical character size. Frame Control Registers are located at the 16th row. The content of each register is described in Figure 5 and following register set.

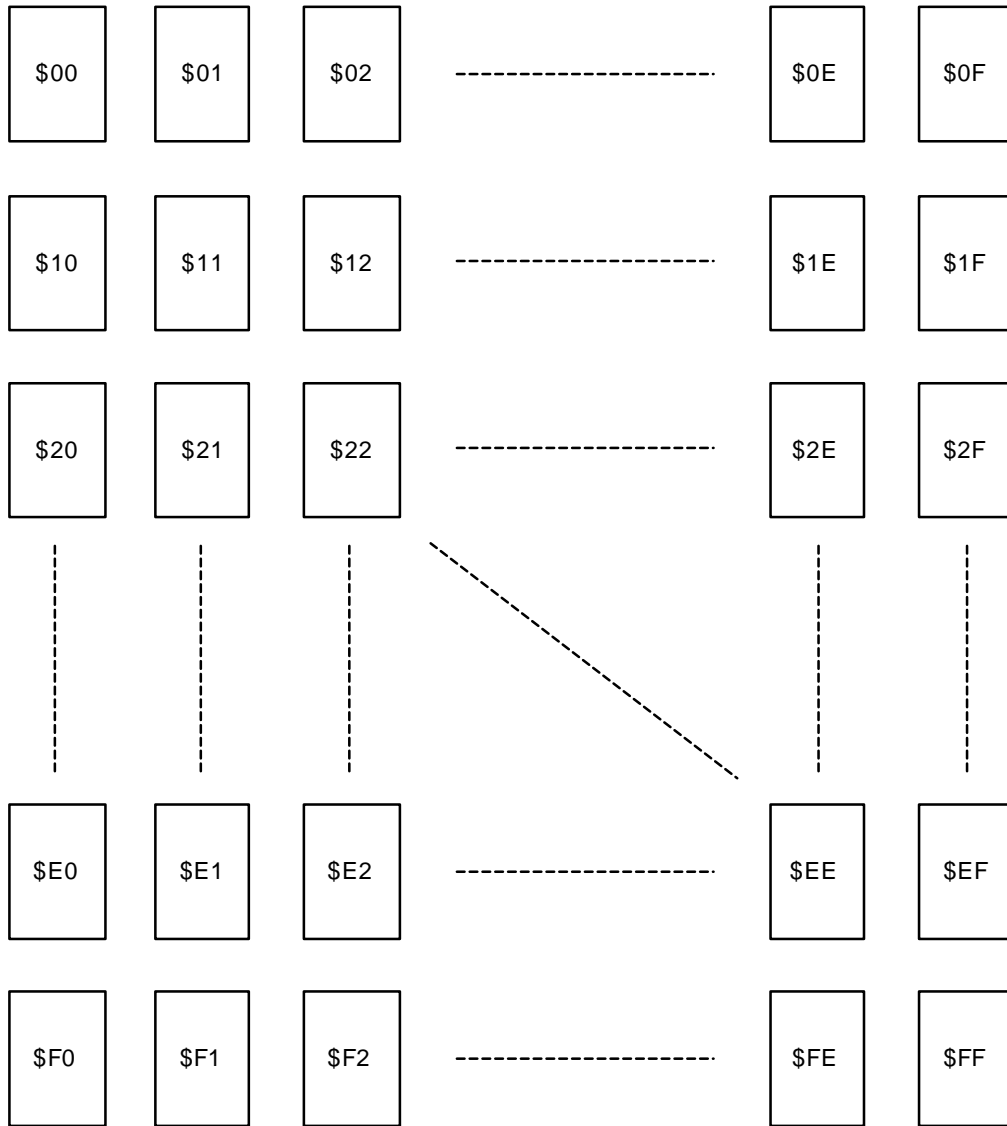


**Figure 5. Memory Map of Display Registers**



**ROM Fonts**

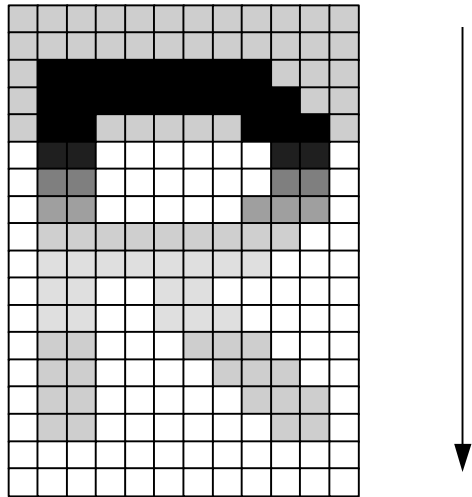
S5D2508A01 is able to supply 256 single-color ROM fonts for describing an OSD icon. So a multi-language OSD icon can be generated. The standard font \$00 is reserved for blank data.



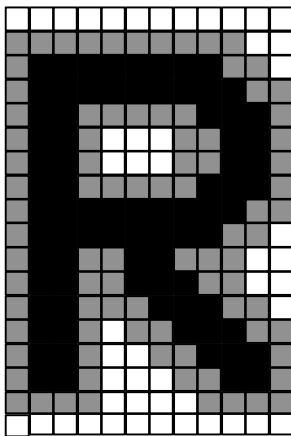
**Figure 6. Array of ROM Fonts**

### Scroll

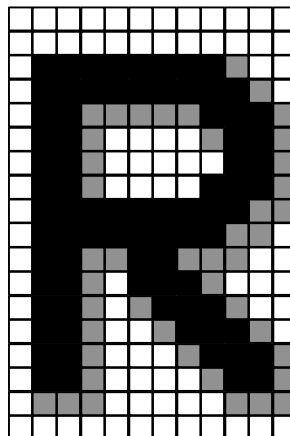
The scrolling function is to display or erase a character slowly from the top line to the bottom. The scrolling time is controlled by 'ScrT' bit of the frame control registers. If 'ScrT' bit is high, then the time is 0.5 sec. Otherwise, 1 sec.



### Character Bordering & Shadowing



Bordering



Shadowing

## Character Height Control

Two examples of the height-controlled character are shown in the following figure. The height control is performed by repeating some lines. The repeating line-number comes from the equation below.

$$\begin{aligned} &[\# \text{ of the repeating lines} = 2 + N \times M] , \\ &\text{where } N = 1,2,3,\dots \text{ and } M = \text{round}\{14 \div (\text{CH}[5:0] - 18)\}. \end{aligned}$$

If the M value is less than or equal to 1, all the lines of the standard font are repeated once or more. This is described as following.

(i) If CH[5:0] is greater than 32, and less than or equal to 46 ( $32 < \text{CH}[5:0] \leq 46$ ), then all lines are repeated once or twice. The lines repeated twice are selected by the following equation.

$$\begin{aligned} &[\# \text{ of the repeating lines} = 2 + N \times M] , \\ &\text{where } N = 1,2,3,\dots \text{ and } M = \text{round}\{14 \div (\text{CH}[5:0] - 32)\}. \end{aligned}$$

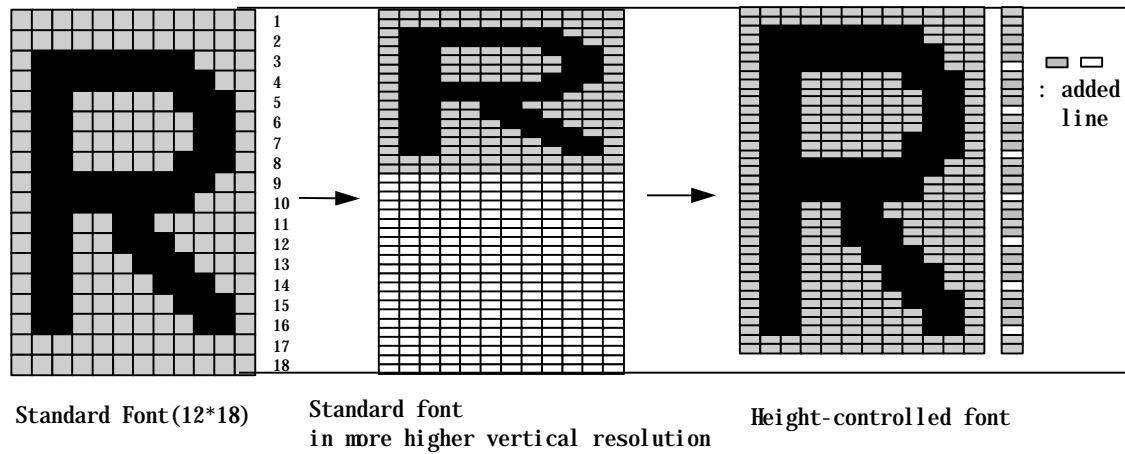
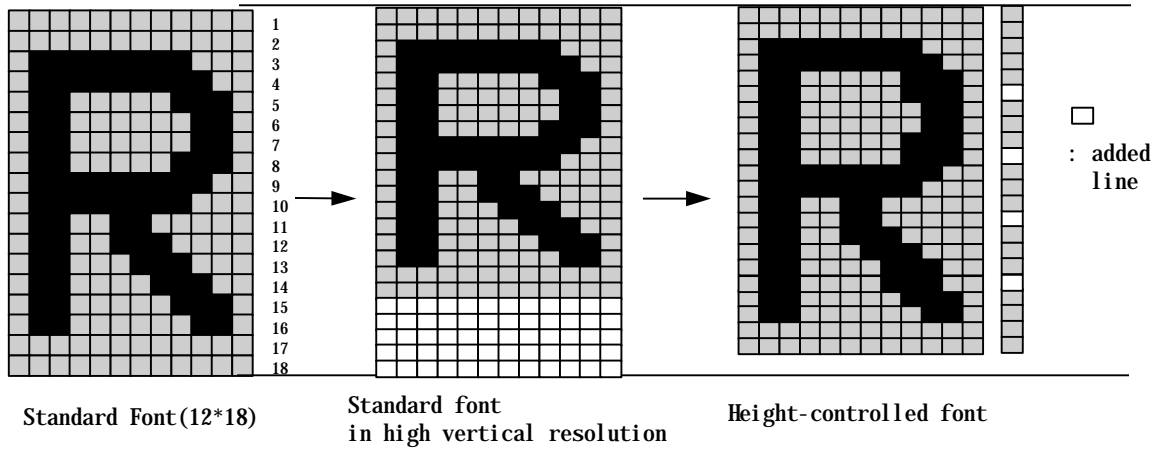
(ii) If CH[5:0] is greater than 46, and less than or equal to 60 ( $46 < \text{CH}[5:0] \leq 60$ ), then all lines are repeated twice or three times. The lines repeated three times are selected by the following equation.

$$\begin{aligned} &[\# \text{ of the repeating lines} = 2 + N \times M] , \\ &\text{where } N = 1,2,3,\dots \text{ and } M = \text{round}\{14 \div (\text{CH}[5:0] - 46)\}. \end{aligned}$$

iii) If CH[5:0] is greater than 60, and less than or equal to 64 ( $60 < \text{CH}[5:0] \leq 64$ ), then all lines are repeated three or four times. The lines repeated four times are selected by the following equation.

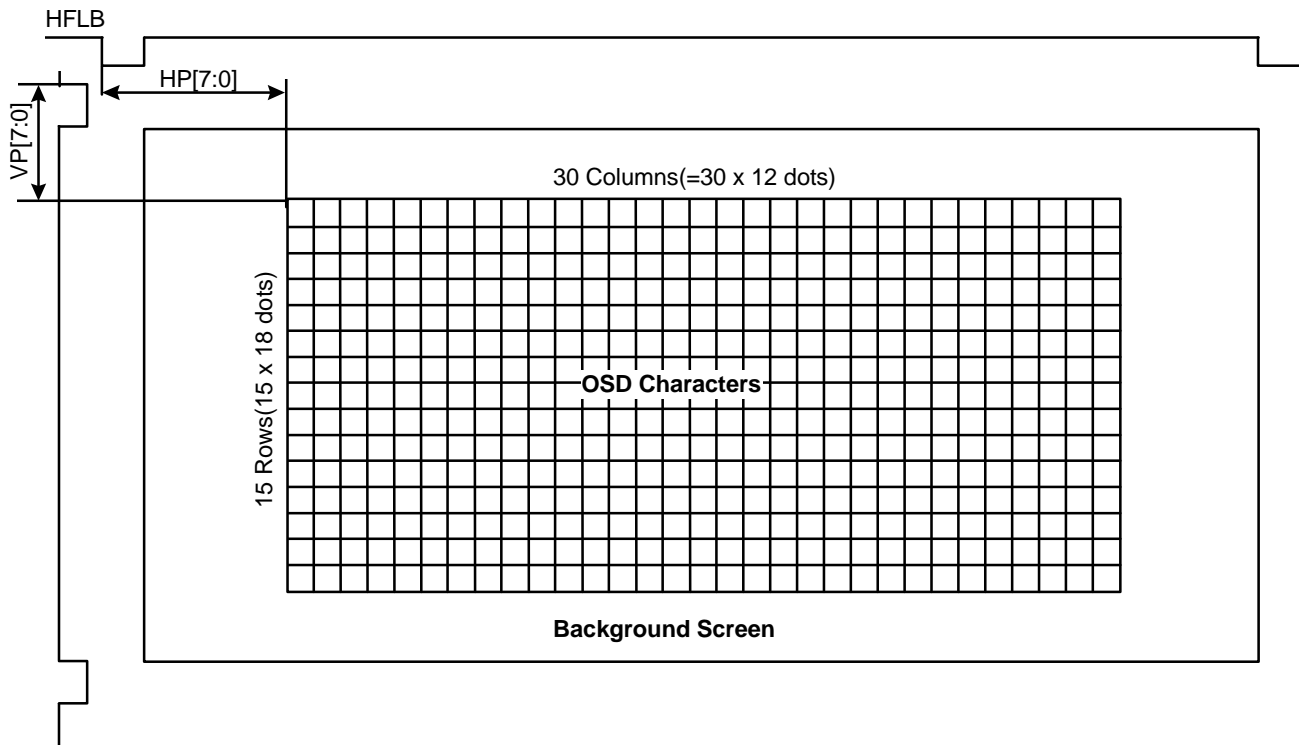
$$\begin{aligned} &[\# \text{ of the repeating lines} = 2 + N \times M] , \\ &\text{where } N = 1,2,3,\dots \text{ and } M = \text{round}\{14 \div (\text{CH}[5:0] - 60)\}. \end{aligned}$$

The repeating line-number is limited to 16.



## FRAME CONTROL &amp; TIMING

Figure 7 shows the composition of display frame with the OSD characters.



**Figure 7. Frame Composition with the OSD Characters**

User can determine the dot frequency by the equation of H freq. x the number of horizontal resolution. And the number of horizontal resolution is determined by the bit9 - 8 (dot 1, dot 0) of the frame Control registers-1. If dot 0 = '0', dot 1 = '0', then the dot frequency is calculated by the equation of H freq.  $\times$  320. If the H freq. = 15 kHz, then the dot frequency is  $15 \text{ kHz} \times 320 = 4.8 \text{ MHz}$ . If dot 0 = '1', dot 1 = '1' and the horizontal frequency is 120 kHz, then the dot frequency is  $120 \text{ kHz} \times 800 = 96 \text{ MHz}$ . 96 MHz is the maximum clock frequency in this processor.

## REGISTER DESCRIPTION

**Character & Attribute Register : Row00~14, Column00~29**

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
BINV	BOX1	BOX0	B	G	R	Blink	-	C7	C6	C5	C4	C3	C2	C1	C0
← Character Attribute →								← Character Code (256 Fonts) →							

**Row Attribute Register : Row00~14, Column30**

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
-	BREN	INTE	CBli	BOXE	BORD	SHA	RB	RG	RR	RINT	CINT	HZ1	HZ0	VZ1	VZ0
								← Raster Color →		← Intensity →		← Character Size →			

**Frame Control Register 0 : Row15, Column00**

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
-	Fde	FdeT	VPOL	HPOL	-	-	-	-	Erase	EN	ScrI	ScrT	Bli1	Bli0	BliT

**Frame Control Register 1 : Row15, Column01**

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
CP1	CP0	Fpll	HF2	HF1	HF0	dot1	dot0	DPLL	FBLK	CH5	CH4	CH3	CH2	CH1	CH0
← PLL Control →									← Character Height Control →						

**Frame Control Register 2 : Row15, Column02**

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0
← Horizontal Start Position →								← Vertical Start Position →							

Table 4. Register Description













Registers	Bits	Description																																			
Character & Attribute Register (Row 00— 14, Column 00~29)	C7— C0 (Bit 7— 0)	Character Code Address of 256 ROM Fonts.																																			
	Blink/FINT (Bit 9)	<p>Character Blinking/Font Intensity Enable. If INTE'bit is low, this bit control blinking effect. The blinking period is set by the 'BliT' bit and the duty is selected by the 'Bli0' and ' Bli1' bits. If INTE'bit is high, this bit control the font intensity combined with INTE,' RINT'and CINT'as following table.</p> <table border="1"> <thead> <tr> <th>INTE</th> <th>Blink/FINT</th> <th>RINT</th> <th>CINT</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>-</td> <td>-</td> <td>Normal</td> </tr> <tr> <td>0</td> <td>1</td> <td>-</td> <td>-</td> <td>Blink</td> </tr> <tr> <td>1</td> <td>0</td> <td>-</td> <td>-</td> <td>Normal(No Intensity)</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>1</td> <td>Character Intensity</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>0</td> <td>Raster Intensity</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>Character &amp; Raster Intensity</td> </tr> </tbody> </table>	INTE	Blink/FINT	RINT	CINT	Function	0	0	-	-	Normal	0	1	-	-	Blink	1	0	-	-	Normal(No Intensity)	1	1	0	1	Character Intensity	1	1	1	0	Raster Intensity	1	1	1	1	Character & Raster Intensity
	INTE	Blink/FINT	RINT	CINT	Function																																
	0	0	-	-	Normal																																
0	1	-	-	Blink																																	
1	0	-	-	Normal(No Intensity)																																	
1	1	0	1	Character Intensity																																	
1	1	1	0	Raster Intensity																																	
1	1	1	1	Character & Raster Intensity																																	
B,G,R (Bit C— A)	Character color is determined by these bits. 8 colors can be selected and the color intensity of a character is given by 'CINT' bit of Row Attribute Registers. So user can select up to 16 colors.																																				
BOX 1, BOX0 (Bit E, D)	<p>Character Box Drawing. The combinations of this two bits generate four different box drawing modes as following. The following example is the case that box dawning is activated with the font 'A'</p> <table border="1"> <tr> <td></td> <td>BOX0</td> <td>0</td> <td>1</td> </tr> <tr> <td>BOX1</td> <td>0</td> <td>BOX OFF</td> <td></td> </tr> <tr> <td>1</td> <td></td> <td></td> <td></td> </tr> </table> <p>* Bit F— D(RB/RG/RR) is also used for raster color by setting the 'BOXE' bit low. if the 'BOXE' bit is low,Raster color of a font is determined by this bits . Priority of raster color selected here is higher than that of row attribute.</p>		BOX0	0	1	BOX1	0	BOX OFF		1																											
	BOX0	0	1																																		
BOX1	0	BOX OFF																																			
1																																					

Table 4. Register Description (Continued)

Registers	Bits	Description															
	BINV (Bit F)	Box Inversion. The box drawing activated by the bit E and D is changed to white box from black and conversely.															
Row Attribute Register (Row 00 ~ 14, Column 30)	VZ1,VZ0 (Bit 1, 0)	Vertical Character Size Control. Vertical character size is determined by the combinations of this two bits as following table. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>VZ1</th> <th>VZ0</th> <th>Vertical Character Size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1X</td> </tr> <tr> <td>0</td> <td>1</td> <td>2X</td> </tr> <tr> <td>1</td> <td>0</td> <td>3X</td> </tr> <tr> <td>1</td> <td>1</td> <td>4X</td> </tr> </tbody> </table>	VZ1	VZ0	Vertical Character Size	0	0	1X	0	1	2X	1	0	3X	1	1	4X
	VZ1	VZ0	Vertical Character Size														
	0	0	1X														
	0	1	2X														
	1	0	3X														
	1	1	4X														
	HZ1,HZ0 (Bit 3, 2)	Horizontal Character Size Control. The horizontal character size is determined by the combinations of this two bits as following table. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>HZ1</th> <th>HZ0</th> <th>Horizontal Character Size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1X</td> </tr> <tr> <td>0</td> <td>1</td> <td>2X</td> </tr> <tr> <td>1</td> <td>0</td> <td>3X</td> </tr> <tr> <td>1</td> <td>1</td> <td>4X</td> </tr> </tbody> </table>	HZ1	HZ0	Horizontal Character Size	0	0	1X	0	1	2X	1	0	3X	1	1	4X
	HZ1	HZ0	Horizontal Character Size														
0	0	1X															
0	1	2X															
1	0	3X															
1	1	4X															
CINT (Bit 4)	Character Color Intensity. If INTE'bit and this bit is set, the color intensity of characters setting FINT'bit in the same row is high.																
RINT (Bit 5)	Raster Color Intensity. If INTE'bit and this bit is set, the color intensity of rasters setting FINT'bit in the same row is high.																
RB, RG, RR (Bit 8— 6)	Raster Color is determined by these bits. 8 colors can be selected and the color intensity of a character is given by RINT'bit of Row Attribute Registers. So it can be selected up to 16 colors.																
SHA	Character Shadowing. Set this bit to activate characters shadowing.																
BORD	Character Bordering. Set this bit to activate characters shadowing.																



Table 4. Register Description (Continued)

Registers	Bits	Description
	BOXE (Bit B)	BOX Enable. If this bit is set, Bit F-D in the Character & Attribute Registers are used for the box-drawing function. Otherwise, those are used for raster color of a font. Even though the raster color attribute is given by Bit 8-6 in the row attribute registers, the priority of Bit F-D in the character & attribute registers is higher.
	CBli (Bit C)	Color Blink Enable. If this bit is high, color blinking effect is activated. The effect is to repeat color inversion between character and raster. Color blinking time and the duty is controlled by Bil T, Bil 1 and Bli 0.
	INTE (Bit D)	Intensity Enable. If this bit is set, the function of RINT and CINT bit are enabled and the bit 9 of Character & Attribute Register control the font intensity effect. Otherwise, all intensity functions are disabled and the bit 9 of Character & Attribute Register control the blinking effect.
	BREN (Bit E)	Back Raster Blank Enable. If this bit is high and the raster color is black, the raster is transparent
	Bit F	Reserved

Table 4. Register Description (Continued)

Registers	Bits	Description															
Frame Control Register 0 (Row 15, Column 00)	Bli T (Bit 0)	Blink Time Control. If this bit is high, the blink time is 0.5 sec. Otherwise, 1 sec.															
	Bli 1, Bli 0 (Bit 2, 1)	Blinking Duty Control. The blinking duty is controlled by the combination of this two bits as following. <table border="1" data-bbox="619 573 1265 813"> <thead> <tr> <th>Bli 1</th> <th>Bli 0</th> <th>Blinking Duty</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Blink Off</td> </tr> <tr> <td>0</td> <td>1</td> <td>Duty 25%</td> </tr> <tr> <td>1</td> <td>0</td> <td>Duty 50%</td> </tr> <tr> <td>1</td> <td>1</td> <td>Duty 75%</td> </tr> </tbody> </table>	Bli 1	Bli 0	Blinking Duty	0	0	Blink Off	0	1	Duty 25%	1	0	Duty 50%	1	1	Duty 75%
	Bli 1	Bli 0	Blinking Duty														
	0	0	Blink Off														
	0	1	Duty 25%														
	1	0	Duty 50%														
	1	1	Duty 75%														
	ScrT (Bit 3)	Scroll Time Control. If this bit is high, the scroll time is 0.5 sec. Otherwise, 1 sec.															
	Scrl (Bit 4)	Scroll Enable. The scroll display is activated by setting this bit high.															
	EN (Bit 5)	OSD Enable. If this bit is high, OSD is enable. Otherwise, disable.															
	Erase (Bit 6)	RAM Erasing. RAM data are erased by setting this bit.															
Bit A — 7	Reserved.																
HPOL (Bit B)	Polarity of Horizontal Fly Back Signal. Positive 1, Negative 0																
VPOL (Bit C)	Polarity of Vertical Fly Back Signal. Positive 1, Negative 0																
FdeT (Bit D)	Fade-in and fade-out Time Control. If this bit is high, the time is 0.5 sec. Otherwise, 1 sec.																
Fde (Bit E)	Fade-in and fade-out Enable. The fade-in and fade-out effect is activated by setting this bit high.																
Bit F	Reserved.																

Table 4. Register Description (Continued)

Registers	Bits	Description																																			
Frame Control Register 1 (Row 15, Column 01)	CH5— CH0 (Bit 5— 0)	Character Height Control. The vertical character size is determined by the bit 'VZ1' and VZ0'. According to the value made by this six bits, the character height is determined. If the value is 32, the number of vertical pixel of character font is 32. Eventually, the character height is expanded from 18 to 63. The binary vlaue must be greater than 18.																																			
	FBLK (Bit 6)	It determines the configuration of FBLK output pin. When it is clear, FBLK pin outputs high during displaying characters or rasters. Otherwise,FBLK pin outputs high only during displaying characters.																																			
	DPLL (Bit 7)	It determines the PLL scheme. If this bit is low, then the PLL mode is differential mode. Otherwise, single mode.																																			
	dot 1,dot 0 (Bit 9,8)	This two bits determine the number of dots per horizontal line. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>dot 1</th> <th>dot 0</th> <th>No. of Dots</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>320 dots/line</td> </tr> <tr> <td>0</td> <td>1</td> <td>480 dots/line</td> </tr> <tr> <td>1</td> <td>0</td> <td>640 dots/line</td> </tr> <tr> <td>1</td> <td>1</td> <td>800 dots/line</td> </tr> </tbody> </table>	dot 1	dot 0	No. of Dots	0	0	320 dots/line	0	1	480 dots/line	1	0	640 dots/line	1	1	800 dots/line																				
	dot 1	dot 0	No. of Dots																																		
	0	0	320 dots/line																																		
	0	1	480 dots/line																																		
1	0	640 dots/line																																			
1	1	800 dots/line																																			
HF2— HF0 (Bit C— A)	The horizontal frequency information is transferred by this three bits. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>HF2</th> <th>HF1</th> <th>HF0</th> <th>Hf Information</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>15 KHz &lt; Hf &lt; 20 KHz</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>20 KHz ≤ Hf &lt;35 KHz</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>35 KHz ≤ Hf &lt; 50 KHz</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>50 KHz ≤ Hf &lt; 65 KHz</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>65 KHz ≤ Hf &lt;80 KHz</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>80 KHz ≤ Hf &lt; 95 KHz</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>95 KHz ≤ Hf &lt; 110 KHz</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>110 KHz ≤ Hf &lt; 120 KHz</td> </tr> </tbody> </table>	HF2	HF1	HF0	Hf Information	0	0	0	15 KHz < Hf < 20 KHz	0	0	1	20 KHz ≤ Hf <35 KHz	0	1	0	35 KHz ≤ Hf < 50 KHz	0	1	1	50 KHz ≤ Hf < 65 KHz	1	0	0	65 KHz ≤ Hf <80 KHz	1	0	1	80 KHz ≤ Hf < 95 KHz	1	1	0	95 KHz ≤ Hf < 110 KHz	1	1	1	110 KHz ≤ Hf < 120 KHz
HF2	HF1	HF0	Hf Information																																		
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1	1	0	95 KHz ≤ Hf < 110 KHz																																		
1	1	1	110 KHz ≤ Hf < 120 KHz																																		
FPLL (Bit D)	If this bit is high, the VCO block of OSD_PLL operates on full range (4MHz - 96 MHz).																																				
CP 1,CP 0 (Bit F,E)	This bit controls charge pump output current. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>CP 1</th> <th>CP 0</th> <th>Charge Pump Current</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0.5mA</td> </tr> <tr> <td>0</td> <td>1</td> <td>0.75mA</td> </tr> <tr> <td>1</td> <td>0</td> <td>1.0mA</td> </tr> <tr> <td>1</td> <td>1</td> <td>1.25mA</td> </tr> </tbody> </table>	CP 1	CP 0	Charge Pump Current	0	0	0.5mA	0	1	0.75mA	1	0	1.0mA	1	1	1.25mA																					
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Table 4. Register Description (Continued)

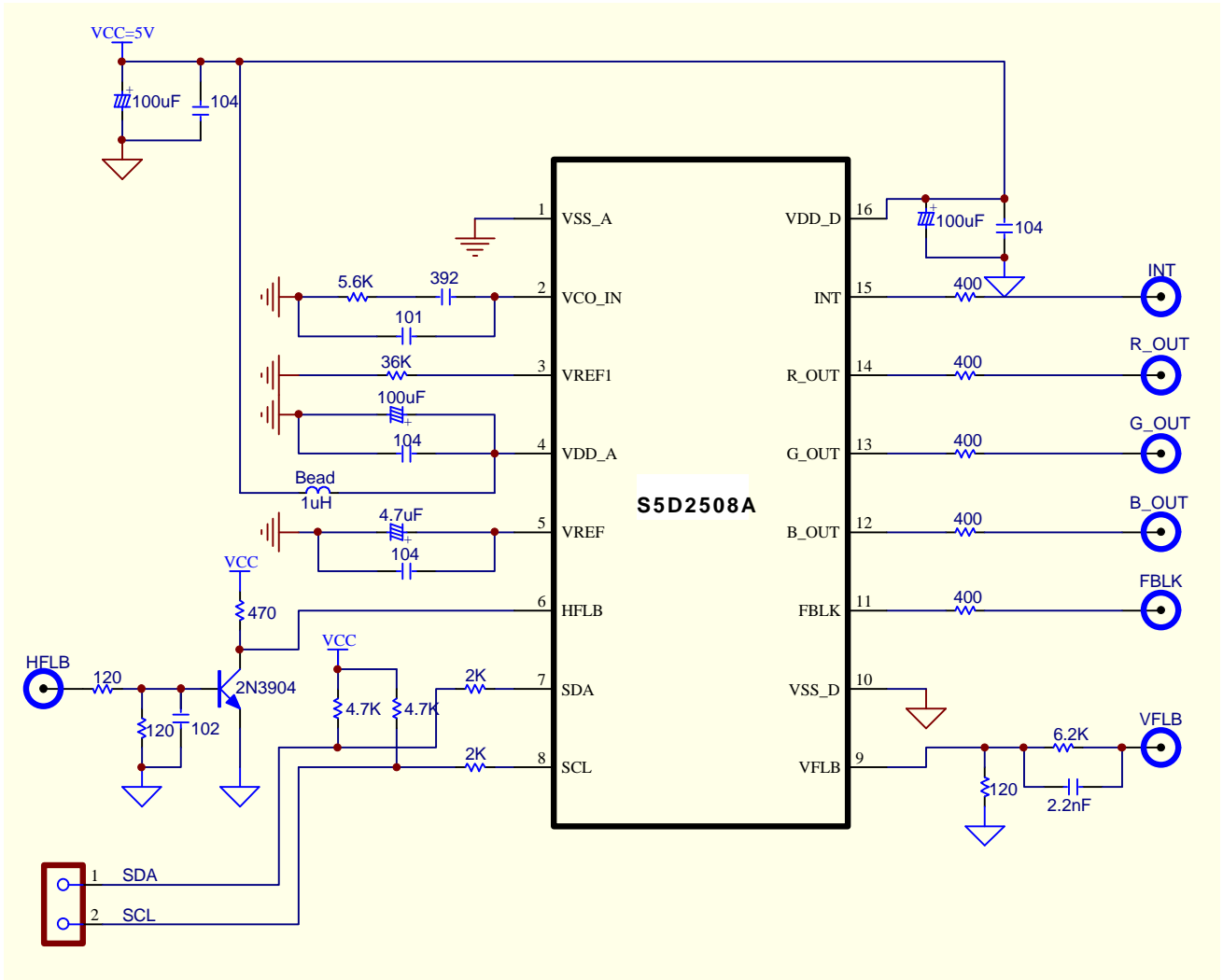
Registers	Bits	Description
Frame Control Register 2 (Row 15, Column 02)	VP7— VP0 (Bit 7— 0)	Vertical Start Position Control. It means the top margin height from the V-sync reference edge. ( = VP[7:0] × 4 )
	HP7— HP0 (Bit F— 8)	Horizontal Start Position Control. It means the horizontal display delay from the H-sync reference edge to the 1'st pixel position of characters. ( = HP[7:0] × 6 )

STANDARD ROM FONTS

000	001	002	003	004	005	006	007	008	009	00A	00B	00C	00D	00E	00F
010	011	012	013	014	015	016	017	018	019	01A	01B	01C	01D	01E	01F
020	021	022	023	024	025	026	027	028	029	02A	02B	02C	02D	02E	02F
	0	1	2	3	4	5	6	7	8	9	:				
030	031	032	033	034	035	036	037	038	039	03A	03B	03C	03D	03E	03F
	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
040	041	042	043	044	045	046	047	048	049	04A	04B	04C	04D	04E	04F
P	Q	R	S	T	U	V	W	X	Y	Z					
050	051	052	053	054	055	056	057	058	059	05A	05B	05C	05D	05E	05F
	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
060	061	062	063	064	065	066	067	068	069	06A	06B	06C	06D	06E	06F
p	q	r	s	t	u	v	w	x	y	z					
070	071	072	073	074	075	076	077	078	079	07A	07B	07C	07D	07E	07F

Ä	Ë	Ï	Ö	Ü	Â	Ê	Î	Ô	Û	Á	É	Í	Ó	Ú	Ç
080	081	082	083	084	085	086	087	088	089	08A	08B	08C	08D	08E	08F
ä	ë	ï	ö	ü	â	ê	î	ô	û	á	é	í	ó	ú	ç
090	091	092	093	094	095	096	097	098	099	09A	09B	09C	09D	09E	09F
À	È	Ì	Ò	Ù	Ã	Õ	Ñ	Ã	Š	Ž	Ÿ	ß			
0AA	0AB	0AC	0AD	0AE	0AF										
à	è	ì	ò	ù	ã	õ	ñ	ã	š	ž	ÿ	œ			
0B0	0B1	0B2	0B3	0B4	0B5	0B6	0B7	0B8	0B9	0BA	0BB	0BC	0BD	0BE	0BF
Ⓜ	Ⓝ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ
0C0	0C1	0C2	0C3	0C4	0C5	0C6	0C7	0C8	0C9	0CA	0CB	0CC	0CD	0CE	0CF
Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ
0D0	0D1	0D2	0D3	0D4	0D5	0D6	0D7	0D8	0D9	0DA	0DB	0DC	0DD	0DE	0DF
Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ
0E0	0E1	0E2	0E3	0E4	0E5	0E6	0E7	0E8	0E9	0EA	0EB	0EC	0ED	0EE	0EF
Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ
0F0	0F1	0F2	0F3	0F4	0F5	0F6	0F7	0F8	0F9	0FA	0FB	0FC	0FD	0FE	0FF

APPLICATION CIRCUIT



NOTES