

## On-Screen-Display for LCD Monitor

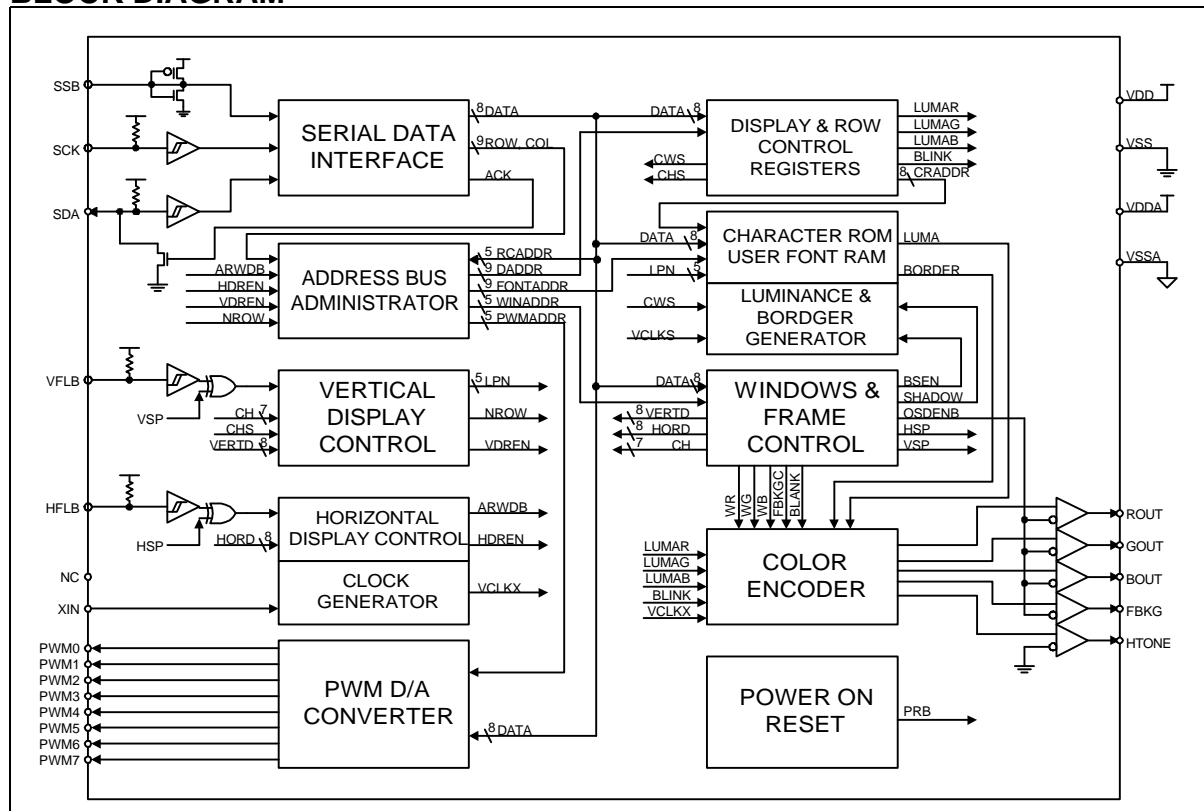
### FEATURES

- Horizontal sync input may be up to 120 KHz.
- Acceptable wide-range pixel clock up to 96MHz from XIN pin.
- Full-screen display consists of 15 (rows) by 30 (columns) characters.
- 12 x 18 dot matrix per character.
- Total of 256 characters and graphic fonts including 248 mask ROM fonts and 8 programmable RAM fonts.
- 8 color selection maximum per display character.
- Double character height and/or width control.
- Programmable positioning for display screen center.
- Bordering, shadowing and blinking effect.
- Programmable vertical character height (18 to 71 lines) control.
- Row to row spacing register to manipulate the constant display height.
- 4 programmable background windows with multi-level operation.
- Software clears for display frame.
- Half tone and fast blanking output.
- 8-channel/8-bit PWM D/A converter output.
- Compatible with SPI bus or I<sup>2</sup>C interface with address 7AH (slave address is mask option).
- 16 or 24-pin PDIP/SOP package.

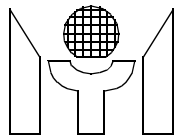
### GENERAL DESCRIPTION

MTV118 is designed for LCD monitor applications to display the built-in characters or fonts onto an LCD monitor screen. The display operates by transferring data and control information from the micro controller to the RAM through a serial data interface. It can execute full screen displays automatically and specific functions such as character bordering, shadowing, blinking, double height and width, font by font color control, frame positioning, frame size control by character height and windowing effect. Moreover, MTV118 also provides 8 PWM DAC channels with 8-bit resolution and a PWM clock output for external digital-to-analog control.

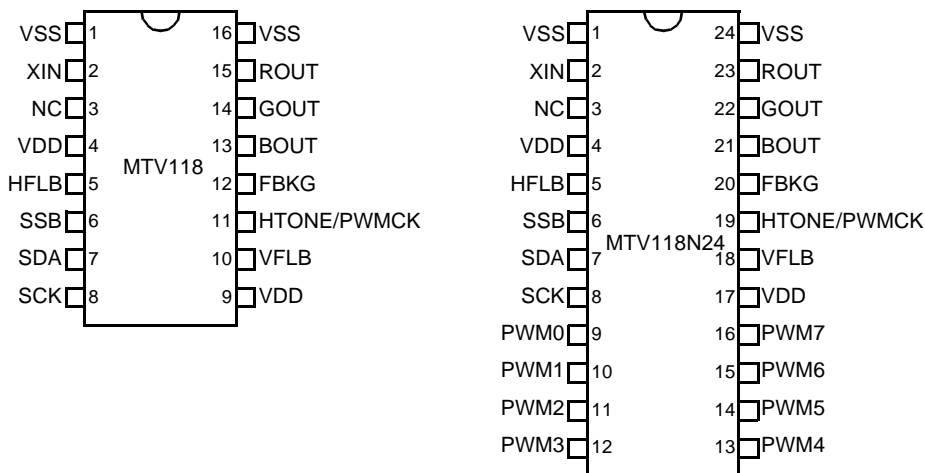
### BLOCK DIAGRAM



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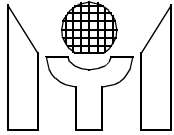


## 1.0 PIN CONNECTION



## 2.0 PIN DESCRIPTIONS

Name	I/O	Pin #		Descriptions
		N16	N24	
VSS	-	1	1	<b>Ground.</b> This ground pin is used for internal circuitry.
XIN	I	2	2	<b>Pixel Clock Input.</b> This is a clock input pin. MTV118 is driven by an external pixel clock source for all the logics inside. The frequency of XIN must be the integral time of pin HFLB.
NC	I	3	3	<b>No connection.</b>
VDD	-	4	4	<b>Power supply.</b> Positive 5 V DC supply for internal circuitry. A 0.1uF decoupling capacitor should be connected across VDD and VSS.
HFLB	I	5	5	<b>Horizontal Input.</b> This pin is used to input the horizontal synchronizing signal. It is a leading edge trigger and has an internal pull-up resistor.
SSB	I	6	6	<b>Serial Interface Enabler.</b> It is used to enable the serial data and is also used to select the operation of I <sup>2</sup> C or SPI bus. If this pin is left floating, I <sup>2</sup> C bus is enabled, otherwise the SPI bus is enabled.
SDA	I	7	7	<b>Serial Data Input.</b> The external data transfers through this pin to internal display registers and control registers. It has an internal pull-up resistor.
SCK	I	8	8	<b>Serial Clock Input.</b> The clock-input pin is used to synchronize the data transfer. It has an internal pull-up resistor.
PWM0	O	-	9	<b>Open-Drain PWM D/A Converter 0.</b> The output pulse width is programmable by the register of row 15, column 19.
PWM1	O	-	10	<b>Open-Drain PWM D/A Converter 1.</b> The output pulse width is programmable by the register of row 15, column 20.
PWM2	O	-	11	<b>Open-Drain PWM D/A Converter 2.</b> The output pulse width is programmable by the register of row 15, column 21.



Name	I/O	Pin #		Descriptions
		N16	N24	
PWM3	O	-	12	<b>Open-Drain PWM D/A Converter 3.</b> The output pulse width is programmable by the register of row 15, column 22.
PWM4	O	-	13	<b>Open-Drain PWM D/A Converter 4.</b> The output pulse width is programmable by the register of row 15, column 23.
PWM5	O	-	14	<b>Open-Drain PWM D/A Converter 5.</b> The output pulse width is programmable by the register of row 15, column 24.
PWM6	O	-	15	<b>Open-Drain PWM D/A Converter 6.</b> The output pulse width is programmable by the register of row 15, column 25.
PWM7	O	-	16	<b>Open-Drain PWM D/A Converter 7.</b> The output pulse width is programmable by the register of row 15, column 26.
VDD	-	9	17	<b>Power Supply.</b> Positive 5 V DC supply for internal circuitry and a 0.1uF decoupling capacitor should be connected across VDD and VSS.
VFLB	I	10	18	<b>Vertical Input.</b> This pin is used to input the vertical synchronizing signal. It is triggered by lead and has an internal pull-up resistor.
HTONE / PWMCK	O	11	19	<b>Half Tone Output / PWM Clock Output.</b> This is a multiplexed pin selected by the PWMCK bit. This pin can be a PWM clock or used to attenuate R, G, B gain of VGA for the transparent windowing effect.
FBKG	O	12	20	<b>Fast Blanking Output.</b> It is used to cut off external R, G, B signals of VGA while this chip is displaying characters or windows.
BOUT	O	13	21	<b>Blue Color Output.</b> This is a blue color video signal output.
GOUT	O	14	22	<b>Green Color Output.</b> This is a green color video signal output.
ROUT	O	15	23	<b>Red Color Output.</b> This is a red color video signal output.
VSS	-	16	24	<b>Ground.</b> This ground pin is used for internal circuitry.

### 3.0 FUNCTIONAL DESCRIPTIONS

#### 3.1 Serial Data Interface

The serial data interface receives data transmitted from an external controller. There are 2 types of bus which can be accessed through the serial data interface: SPI bus and I<sup>2</sup>C bus.

##### 3.1.1 SPI Bus

When the SSB pin is pulled to a HIGH or LOW level, the SPI bus operation is selected. A valid transmission should start from pulling SSB to LOW level, enabling the MTV118 receiving mode and retaining the LOW level until the last cycle for a complete data packet transfer. The protocol is shown in Figure 1 on page 4.

There are 3 transmission formats as shown below:

Format (a) R - C - D → R - C - D → R - C - D

Format (b) R - C - D → C - D → C - D → C - D

Format (c) R - C - D → D → D → D → D → D

R=row address, C=column address, D=display data

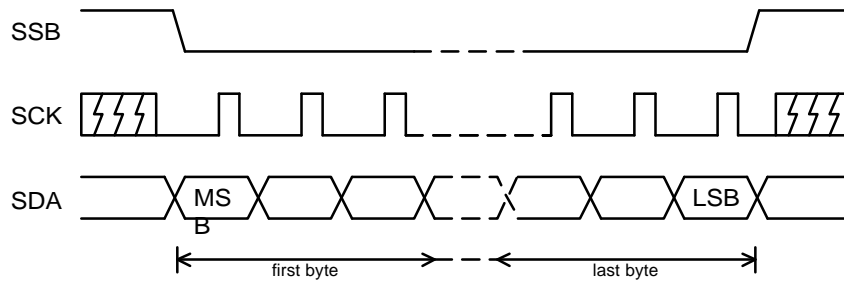
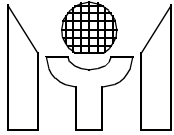


FIGURE 1. Data Transmission Protocol (SPI)

3.1.2 I<sup>2</sup>C Bus

I<sup>2</sup>C bus operation is only selected when the SSB pin is left floating. A valid transmission should begin from writing the slave address 7AH, which is mask option, to MTV118. The protocol is shown in Figure 2 on page 4..

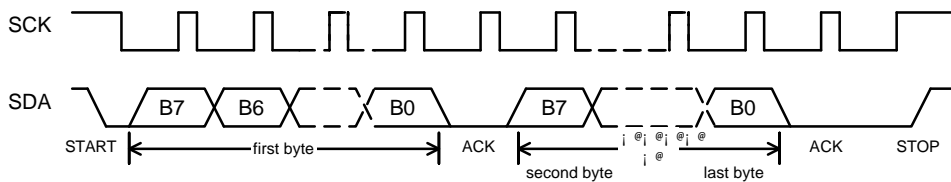


FIGURE 2. Data Transmission Protocol (I<sup>2</sup>C)

There are 3 transmission formats as shown below:

Format (a) S - R - C - D → R - C - D → R - C - D

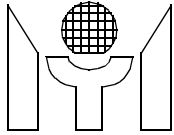
Format (b) S - R - C - D → C - D → C - D → C - D

Format (c) S - R - C - D → D → D → D → D → D

S=slave address, R=row address, C=column address, D=display data

Each arbitrary length of data packet consists of 3 portions: row address (R), column address (C) and display data (D). Format (a) is suitable for updating small amounts of data which will be allocated with different row and column addresses. Format (b) is recommended for updating data that has the same row address but a different column address. Massive data updating or full screen data changes should be done in format (c) to increase transmission efficiency. The row and column addresses will be incremented automatically when format (c) is applied. Furthermore, the undefined locations in display or font RAM should be filled with dummy data.

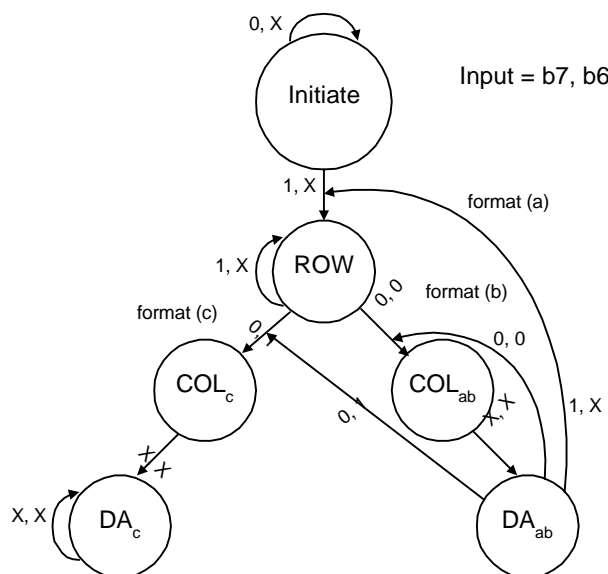
There are 3 types of data which should be accessed through the serial data interface: address bytes of display registers, attribute bytes of display registers and user font RAM data. The protocol is the same for all except bits 5 and 6 of the row addresses. The MSB(b7) is used to distinguish row and column addresses when transferring data from an external controller. Bit 6 of the row address is used to distinguish display registers and user font RAM data and bit6 of the column address is used to differentiate the column address for formats (a), (b) and (c), respectively. Bit 5 of the row address for display registers is used to distinguish the address byte when it is set to "0" and the attribute byte when it is set to "1". The configuration of transmission formats is shown in Table 1 on page 5.



**TABLE 1. Configuration of Transmission Formats**

	Address	b7	b6	b5	b4	b3	b2	b1	b0	Format
<b>Address Bytes of Display Reg.</b>	Row	1	0	0	x	R3	R2	R1	R0	a,b,c
	Column <sub>ab</sub>	0	0	x	C4	C3	C2	C1	C0	a,b
	Column <sub>c</sub>	0	1	x	C4	C3	C2	C1	C0	c
<b>Attribute Bytes of Display Reg.</b>	Row	1	0	1	x	R3	R2	R1	R0	a,b,c
	Column <sub>ab</sub>	0	0	x	C4	C3	C2	C1	C0	a,b
	Column <sub>c</sub>	0	1	x	C4	C3	C2	C1	C0	c
<b>User Fonts RAM</b>	Row	1	1	x	x	x	R2	R1	R0	a,b,c
	Column <sub>ab</sub>	0	0	C5	C4	C3	C2	C1	C0	a,b
	Column <sub>c</sub>	0	1	C5	C4	C3	C2	C1	C0	c

The data transmission is permitted to change from format (a) to format (b) and (c), or from format (b) to format (a), but not from format (c) back to format (a) and (b). The alternation between transmission formats is configured as the state diagram shown in Figure 3 on page 5.



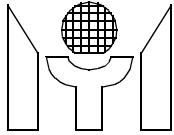
**FIGURE 3. Transmission State Diagram**

**3.2 Address Bus Administrator**

The administrator manages bus address arbitration of internal registers or user font RAM during external data write-in. The external data write through serial data interface to registers must be synchronized by internal display timing. In addition, the administrator also provides automatic incrementation to the address bus when external writing occurs using format (c).

**3.3 Vertical Display Control**

The vertical display control can generate different vertical display sizes for most display standards in current monitors. The vertical display size is calculated with the information of a double character height bit(CH5) and a vertical display height control register(CH6-CH0).The algorithms of a repeating character line display are shown in Tables 2 and 3. The programmable vertical size range is 270 lines to maximum 2130 lines.



The vertical display center for a full-screen display may be figured out according to the information of the vertical starting position register (VERTD) and VFLB input. The vertical delay starting from the leading edge of VFLB is calculated using the following equation:

$$\text{Vertical delay time} = (\text{VERTD} * 4 + 1) * H$$

Where H = 1 horizontal line display time

**TABLE 2. Repeat Line Weight of Character**

CH6-CH0	Repeat Line Weight
CH6,CH5=11	+18*3
CH6,CH5=10	+18*2
CH6,CH5=0x	+18
CH4=1	+16
CH3=1	+8
CH2=1	+4
CH1=1	+2
CH0=1	+1

**TABLE 3. Repeat Line Number of Character**

Repeater Line Weight	Repeat Line #																	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
+1	-	-	-	-	-	-	-	-	v	-	-	-	-	-	-	-	-	-
+2	-	-	-	-	v	-	-	-	-	-	-	-	v	-	-	-	-	-
+4	-	-	v	-	-	-	v	-	-	-	v	-	-	-	v	-	-	-
+8	-	v	-	v	-	v	-	v	-	v	-	v	-	v	-	v	-	-
+16	-	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	-
+17	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	-
+18	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v

Note: "v" means the nth line in the character would be repeated once, while "-" means the nth line in the character would not be repeated.

### 3.4 Horizontal Display Control

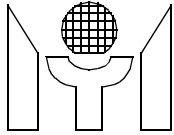
The horizontal display control is used to generate control timing for a horizontal display based on double character width bit (CWS), horizontal positioning register (HORD) and HFLB input. A horizontal display line includes 360 dots for 30 display characters and the remaining dots for a blank region. The horizontal delay starting from the HFLB leading edge is calculated using the following equation:

$$\text{Horizontal delay time} = (\text{HORD} * 6 + 49) * P$$

Where P = 1 XIN pixel display time

### 3.5 Display & Row Control Registers

The internal RAM contains display and row control registers. The display registers have 450 locations which are allocated between row 0/column 0 and row 14/column 29 as shown in Figure 4. Each display register has its corresponding character address on the address byte, and 1 blink bit and its corresponding color bits on attribute bytes. The row control register is allocated at column 30 for row 0 to row 14; it is used to set character size for each respective row. If the double width character (CWS) is cho-



sen, only even column characters may be displayed on-screen and the odd column characters will be hidden.

ROW #	COLUMN #					
	0	1	28	29	30	31
0	DISPLAY REGISTERS				ROW CTRL REG	RESERVED
1						
13						
14						

ROW 15	COLUMN#											
	0	2	3	5	6	8	9	11	12	18	19	26
	WINDOW1		WINDOW2		WINDOW3		WINDOW4		FRAME CTRL REG		PWM D/A CTRL REG	

**FIGURE 4. Memory map**

**3.5.1 Register Descriptions**

1. (i) Display Register, (Row 0 - 14, Column 0 - 29)

ADDRESS BYTE

b7	b6	b5	b4	b3	b2	b1	b0
CRADDR							
MSB				LSB			

CRADDR - Defines ROM character and user-programmable fonts address.

(a) 0 ~ 247 ⇒ 248 built-in characters and graphic symbols

(b) 248 ~ 255 ⇒ 8 user-programmable fonts

ATTRIBUTE BYTE

b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	BLINK	R1	G1	B1

BLINK - Enables blinking effect when this bit is set to " 1 ". The blinking is alternated per 32 vertical frames.

R1, G1, B1 - These bits are used to specify its relative address character color 1.

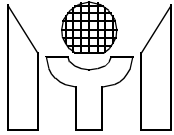
2. Row Control Registers, (Row 0 - 14)

COLN 30	b7	b6	b5	b4	b3	b2	b1	b0
	-	-	-	R2	G2	B2	CHS	CWS

R2, G2, B2 - These bits are used to specify its relative row character color 2. While the corresponding CCS bit is set to 1, color 2 should be chosen.

CHS - Defines double height character to the respective row.

CWS - Defines double width character to the respective row.

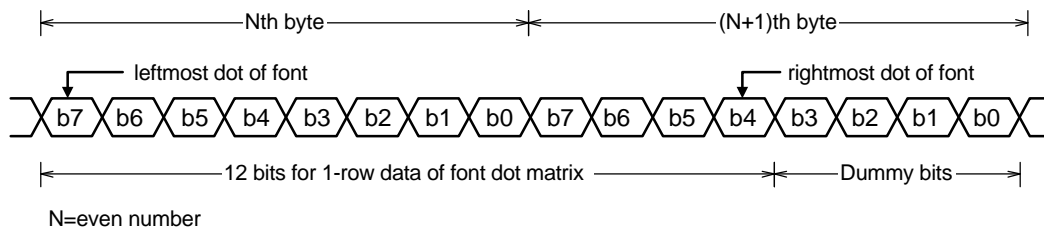


### 3.6 User Font RAM

The user font RAM has 288 locations which are allocated between row 0/column 0 and row 7/column 35 to specify 8 user-programmable fonts, as shown in Figure 5. Each programmable font consists of a 12x18 dot matrix. Each row of dot matrix consists of 2 bytes of data which include 4 dummy bits as shown in figure 6. That is, the dot matrix data of each font is stored in 36-byte registers. For example, font 0 is stored in row 0 from column 0 to column 35 and font 1 is stored in row 1 from column 0 to column 35, etc.

ROW #	COLUMN #					
	0	1	34	35	36	63
0	USER FONT RAM				RESERVED	
1						
6						
7						

**FIGURE 5. User Font RAM Memory Map**



**FIGURE 6. Data Format of Font Dot Matrix**

### 3.7 Character ROM

The character ROM contains 248 built-in characters and symbols from addresses 0 to 247. Each character and symbol consists of a 12x18 dot matrix. The detail pattern structures for each character and symbol are shown in 10.0“CHARACTER AND SYMBOL PATTERN” on page 15.

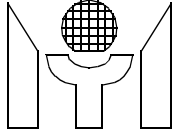
### 3.8 Luminance & Border Generator

There are 2 shift registers included in the design which can shift out of luminance and border dots to the color encoder. The bordering and shadowing feature is configured in this block. For bordering effect, the character will be enveloped with blackedge on 4 sides. For shadowing effect, the character is enveloped with blackedge on right and bottom sides only.

### 3.9 Window and Frame Control

The display frame position is completely controlled by the contents of VERTD and HORD. The window size and position control are specified in columns 0 to 11 on row 15 of the memory map, as shown in Figure 4. Window 1 has the highest priority and window 4 has the least, when 2 windows are overlapping. More detailed information is described as follows:





## 1. Window control registers:

### ROW 15

Column	b7	b6	b5	b4	b3	b2	b1	b0
0,3,6,OR 9	ROW START ADDR				ROW END ADDR			
	MSB				LSB			

Column	b7	b6	b5	b4	b3	b2	b1	b0
1,4,7,OR 10	COL START ADDR				WEN	CCS	-	
	MSB				LSB			

Column	b7	b6	b5	b4	b3	b2	b1	b0
2,5,8,OR 11	COL END ADDR				R	G	B	
	MSB				LSB			

START(END) ADDR - These addresses are used to specify the window size. It should be noted that when the start address is greater than the end address, the window will be disabled.

WEN - Enables the window display.

CCS - When a window is overlapping with the character, character color 2 should be chosen while this bit is set to 1. Color 1 is selected otherwise.

R, G, B - Specifies the color of the relative background window.

## 2. Frame control registers:

### ROW 15

Column 12	b7	b6	b5	b4	b3	b2	b1	b0
	VERTD							
	MSB							
	LSB							

VERTD - Specifies the starting position for vertical display. The total steps are 256, and the increment of each step is 4 horizontal display lines. The initial value is 4 after power-up.

Column 13	b7	b6	b5	b4	b3	b2	b1	b0
	HORD							
	MSB							
	LSB							

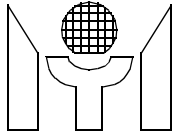
HORD - Defines the starting position for horizontal display. The total steps are 256 and the increment of each step is 6 dots. The initial value is 15 after power-up.

Column 14	b7	b6	b5	b4	b3	b2	b1	b0
	-	CH6	CH5	CH4	CH3	CH2	CH1	CH0

CH6-CH0 - Defines the character vertical height, which is programmable from 18 to 71 lines. The character vertical height is at least 18 lines if the contents of CH6-CH0 are less than 18. For example, when the content is " 2 ", the character vertical height is regarded as equal to 20 lines. If the contents of CH4-CH0 are greater than or equal to 18, it will be regarded as equal to 17. See Tables 2 and 3 for a detailed description of this operation.

Column 15	b7	b6	b5	b4	b3	b2	b1	b0
	Reserved							

This byte is reserved for internal testing.



Column 16	b7	b6	B5	b4	b3	b2	b1	b0
	-	-	-	RSPACE				MSB

RSPACE - Defines the row to row spacing in each unit of the horizontal line. That is, extra RSPACE horizontal lines will be appended below each display row, and the maximum space is 31 lines. The initial value is "0" after power-up.

Column 17	b7	b6	b5	b4	b3	b2	b1	b0
	OSDEN	BSEN	SHADOW	TRIC	BLANK	WENCLR	RAMCLR	FBKGC

OSDEN - Activates the OSD operation when this bit is set to "1". The initial value is "0" after power-up.

BSEN - Enables the bordering and shadowing effect.

SHADOW - Activates the shadowing effect if this bit is set, otherwise the bordering is chosen.

TRIC - Defines the driving state of output pins ROUT, GOUT, BOUT and FBKG when OSD is disabled. That is, while OSD is disabled, these 4 pins will drive LOW if this bit is set to "1", otherwise these pins are in high-impedance state. The initial value is "0" after power-up.

BLANK - Forces the FBKG pin output to HIGH while this bit is set to "1".

WENCLR - Clears all WEN bits of window control registers when this bit is set to "1". The initial value is "0" after power-up.

RAMCLR - Clears all ADDRESS bytes of display registers when this bit is set to "1". The initial value is "0" after power-up.

FBKGC - Defines the output configuration for FBKG pin. When it is set to "0", the FBKG outputs during the display of characters or windows, otherwise, it outputs only during the display of characters.

Column 18	B7	b6	b5	b4	b3	b2	b1	b0
	TEST	FBKGP	PWMCK	DWE	HSP	VSP	PWM1	PWM0

**TEST - = 0 ⇒ Normal mode.**  
**= 1 ⇒ Test mode, not allowed in applications.**

FBKGP - Selects the polarity of the output pin FBKG.  
 = 1 ⇒ Positive polarity FBKG output is selected.  
 = 0 ⇒ Negative polarity FBKG output is selected.  
 The initial value is "1" after power-up.

PWMCK - Selects the output options to the HTONE/PWMCK pin.  
 = 0 ⇒ HTONE option is selected.  
 = 1 ⇒ PWMCK option is selected with 50/50 duty cycle and is synchronous with the input HFLB. The frequency is selected by PWM1, PWM0 as shown in table 4.  
 The initial value is "0" after power-up.

DWE - Enables double width. When the bit is set to "1", the display of the OSD menu can change to half resolution for double character width, and then the number of pixels of each line should be even.

HSP - = 1 ⇒ Accepts positive polarity Hsync input.

= 0 ⇒ Accepts negative polarity Hsync input.

VSP - = 1 ⇒ Accepts positive polarity Vsync input.  
 = 0 ⇒ Accepts negative polarity Vsync input.

PWM1, PWM0 - Selects the PWMCK output frequency.  
 = (0, 0) ⇒ XIN frequency /8  
 = (0, 1) ⇒ XIN frequency /4  
 = (1, 0) ⇒ XIN frequency /2  
 = (1, 1) ⇒ XIN frequency /1  
 The initial value is 0, 0 after power-up.

**Notes :** When XIN is not present, don't write data in any address. If data is written in any address, a malfunction may occur.

**TABLE 4.** PWMCK Frequency and PWMDA Sampling Rate

(PWM1, PWM0)	PWMCK Freq.	PWMDA sampling rate
( 0, 0 )	XIN frequency /8	XIN frequency /(8 * 256)
( 0, 1 )	XIN frequency /4	XIN frequency /(4 * 256)
( 1, 0 )	XIN frequency /2	XIN frequency /(2 * 256)
( 1, 1 )	XIN frequency /1	XIN frequency /(1 * 256)

### 3.10 PWM D/A Converter

There are 8 open-drain PWM D/A outputs (PWM0 to PWM7). The PWM D/A converter output pulse width is programmable by writing data to columns 19-26 registers of row 15 with 8-bit resolution to control the pulse width duration from 0/256 to 255/256. The sampling rate is selected by PWM1, PWM0 as shown in table 4. In applications, all open-drain output pins should be pulled up by external resistors to supply voltage (5V to 9V) for the desired output range.

ROW 15

	b7	b6	b5	b4	b3	b2	b1	b0
Column 19	PWMDA0							
Column 26	PWMDA7							
	MSB							LSB

PWMDA0 - PWMDA7 - Defines the output pulse width of pins PWM0 to PWM7.

### 3.11 Color Encoder

The decoder generates the video output to ROUT, GOUT and BOUT by integrating window color, border blackedge, luminance output and color selection output (R, G, B) to form the desired video outputs.

## 4.0 ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage(VDD,VDDA)	-0.3 to +7 V
Ground Voltage	-0.3 to VDD+0.3 V
Storage Temperature	-65 to +150 °C
Ambient Operating Temperature	0 to +70 °C

## 5.0 OPERATING CONDITIONS

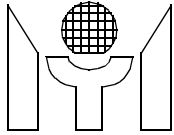
DC Supply Voltage(VDD,VDDA)	+4.75 to +5.25 V
Operating Temperature	0 to +70 °C

## 6.0 ELECTRICAL CHARACTERISTICS (Under Operating Conditions)

Symbol	Parameter	Conditions(Notes)	Min.	Max.	Unit
V <sub>IH</sub>	Input High Voltage	-	0.7 * VDD	VDD+0.3	V
V <sub>IL</sub>	Input Low Voltage	-	VSS-0.3	0.3 * VDD (0.2*VDD for SSB pin )	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> ≥ -24 mA	VDD-0.8	-	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> ≤ 24 mA	-	0.5	V
V <sub>ODH</sub>	Open Drain Output High Voltage	- (For all OD pins, pulled up by external 5 to 9V power supply)	5	9	V
V <sub>ODL</sub>	Open Drain Output Low Voltage	5 mA ≥ I <sub>DOL</sub> ( For all OD pins )	-	0.5	V
I <sub>SB</sub>	Standby Current	V <sub>in</sub> = VDD, I <sub>load</sub> = 0uA	-	12	mA
I <sub>CC</sub>	Operating Current	Pixel rate=96MHz I <sub>load</sub> = 0uA	-	20	mA

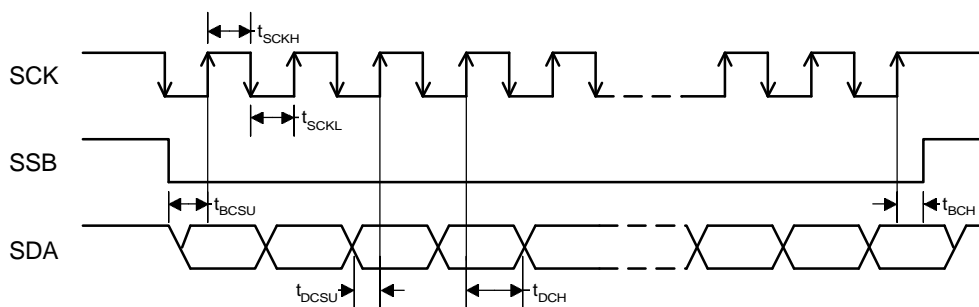
## 7.0 SWITCHING CHARACTERISTIC (Under Operating Conditions)

Symbol	Parameter	Min.	Typ.	Max.	Unit
f <sub>HFLB</sub>	HFLB input frequency	15	-	120	KHz
T <sub>r</sub>	Output rise time	-	-	5	ns
T <sub>f</sub>	Output fall time	-	-	5	ns
t <sub>BCSU</sub>	SSB to SCK set-up time	200	-	-	ns
t <sub>BCH</sub>	SSB to SCK hold time	100	-	-	ns
t <sub>DCSU</sub>	SDA to SCK set-up time	200	-	-	ns
t <sub>DCH</sub>	SDA to SCK hold time	100	-	-	ns
t <sub>SCKH</sub>	SCK HIGH time	500	-	-	ns
t <sub>SCKL</sub>	SCK LOW time	500	-	-	ns
t <sub>SU:STA</sub>	START condition set-up time	500	-	-	ns
t <sub>HD:STA</sub>	START condition hold time	500	-	-	ns
t <sub>SU:STO</sub>	STOP condition set-up time	500	-	-	ns

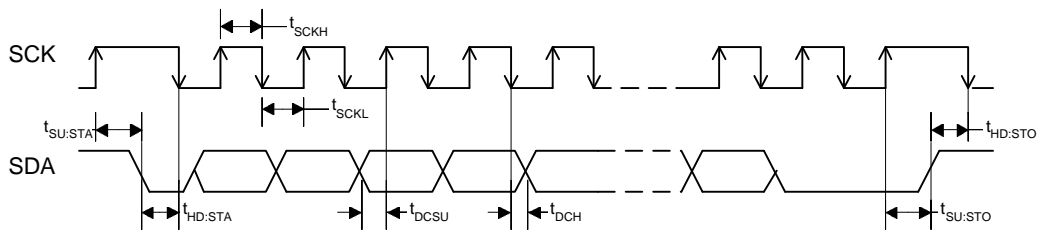


Symbol	Parameter	Min.	Typ.	Max.	Unit
$t_{HD:STO}$	STOP condition hold time	500	-	-	ns
$t_{SETUP}$	HFLB delay to rising edge of pixel clock	2		6	ns
$t_{HOLD}$	minimum pulse width of HFLB	25			ns
$t_{pd}$	propagation delay of output to pixel clock			10	ns
PIXin	pixel clock input	6		96	MHz

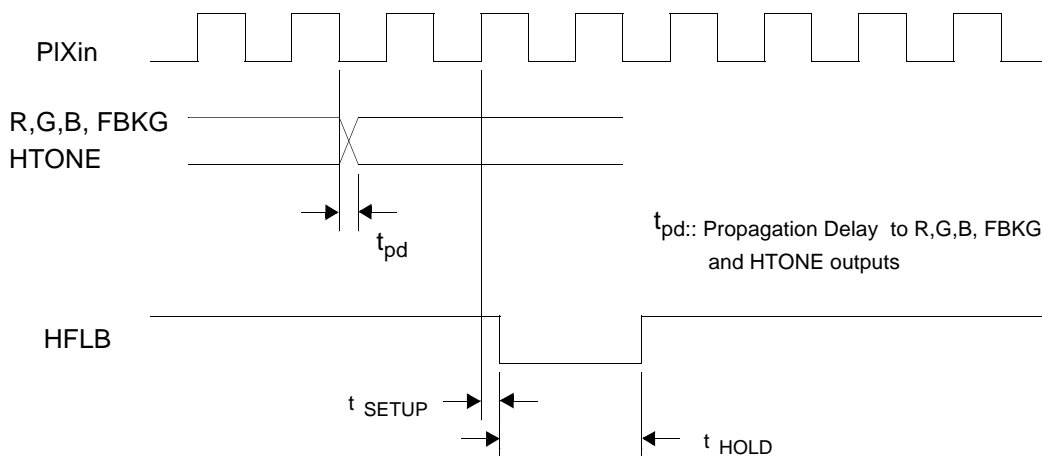
**8.0 TIMING DIAGRAMS**



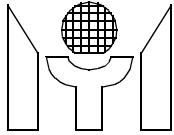
**FIGURE 7. Data Interface Timing (SPI)**



**FIGURE 8. Data Interface Timing (I<sup>2</sup>C)**



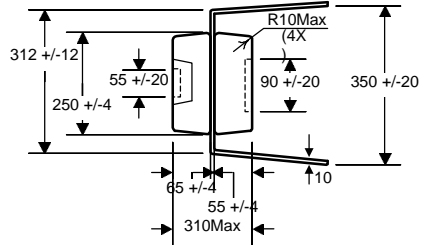
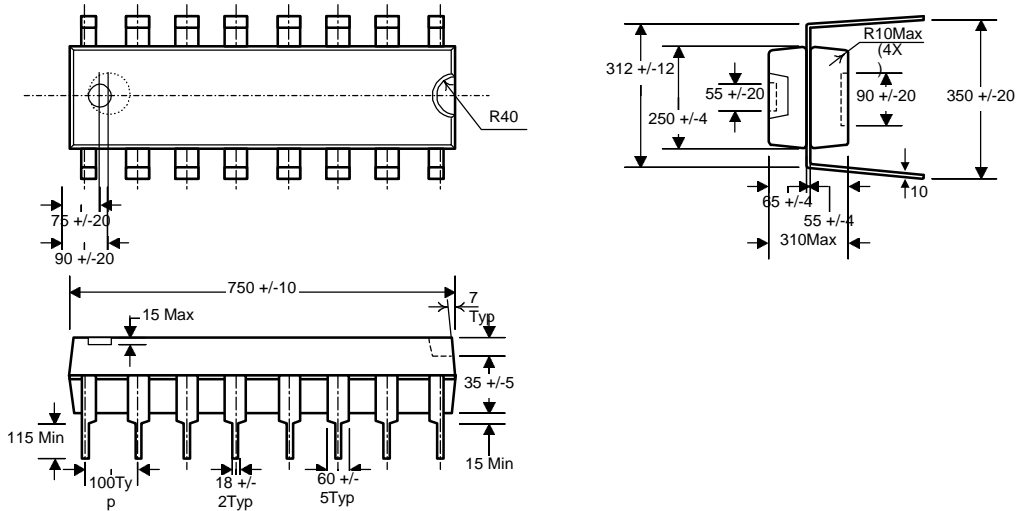
**FIGURE 9. Output and HFLB Timing to Pixel Clock**



**9.0 PACKAGE DIMENSION**

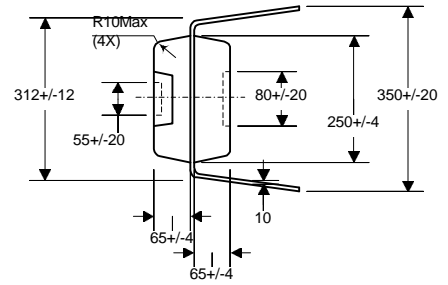
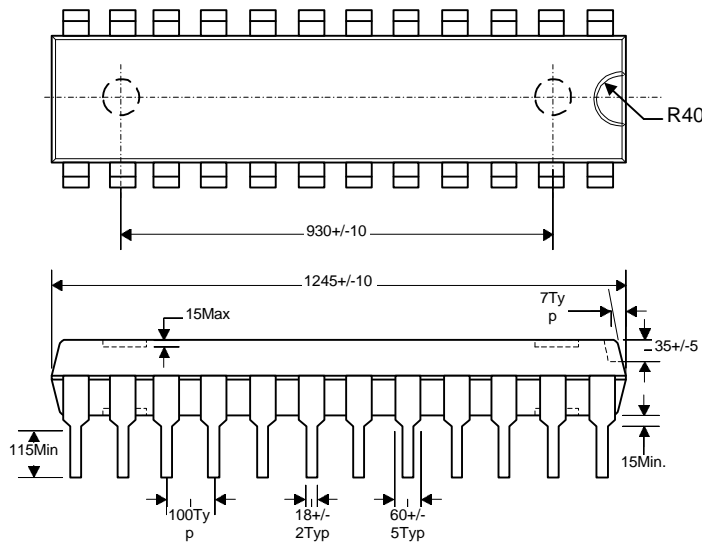
**9.1 16 PDIP 300Mil**

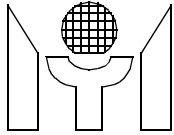
Unit:Mil



**9.2 24 PDIP 300Mil**

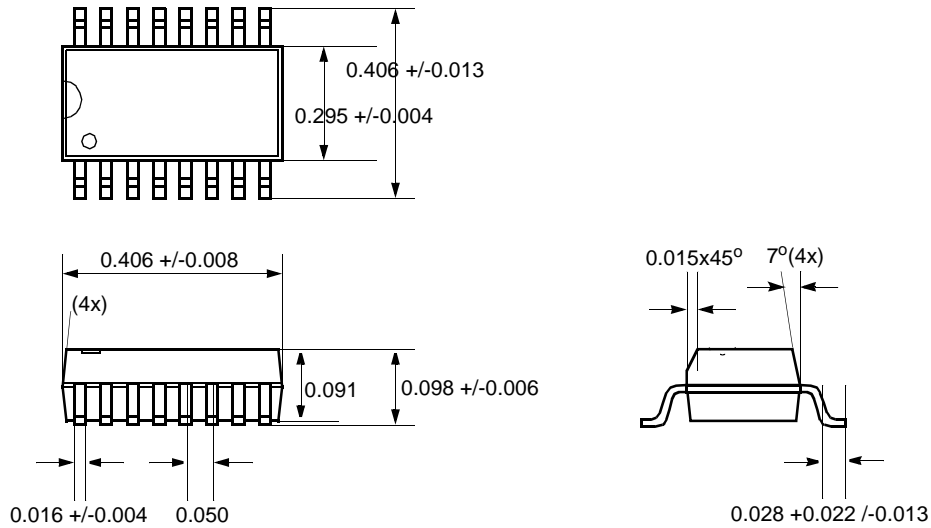
Unit: Mil



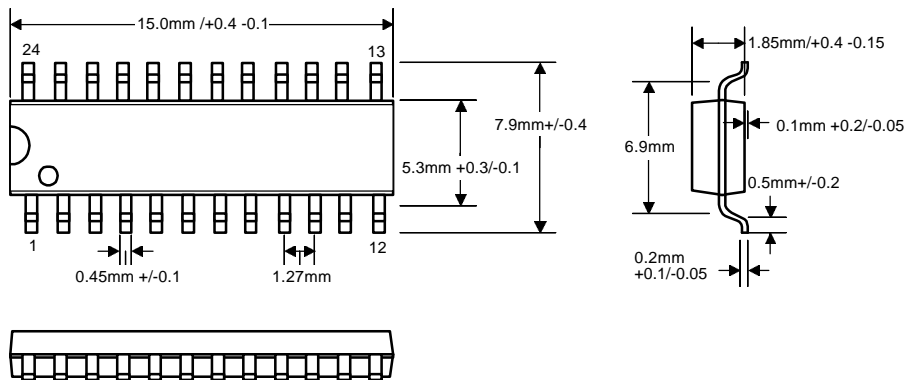


### 9.3 16-pin SOP 300Mil

Unit: Mil

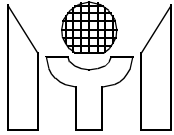


### 9.4 24-pin SOP 300Mil



## 10.0 CHARACTER AND SYMBOL PATTERN

Please see the attachment.



## On-Screen-Display for LCD Monitor

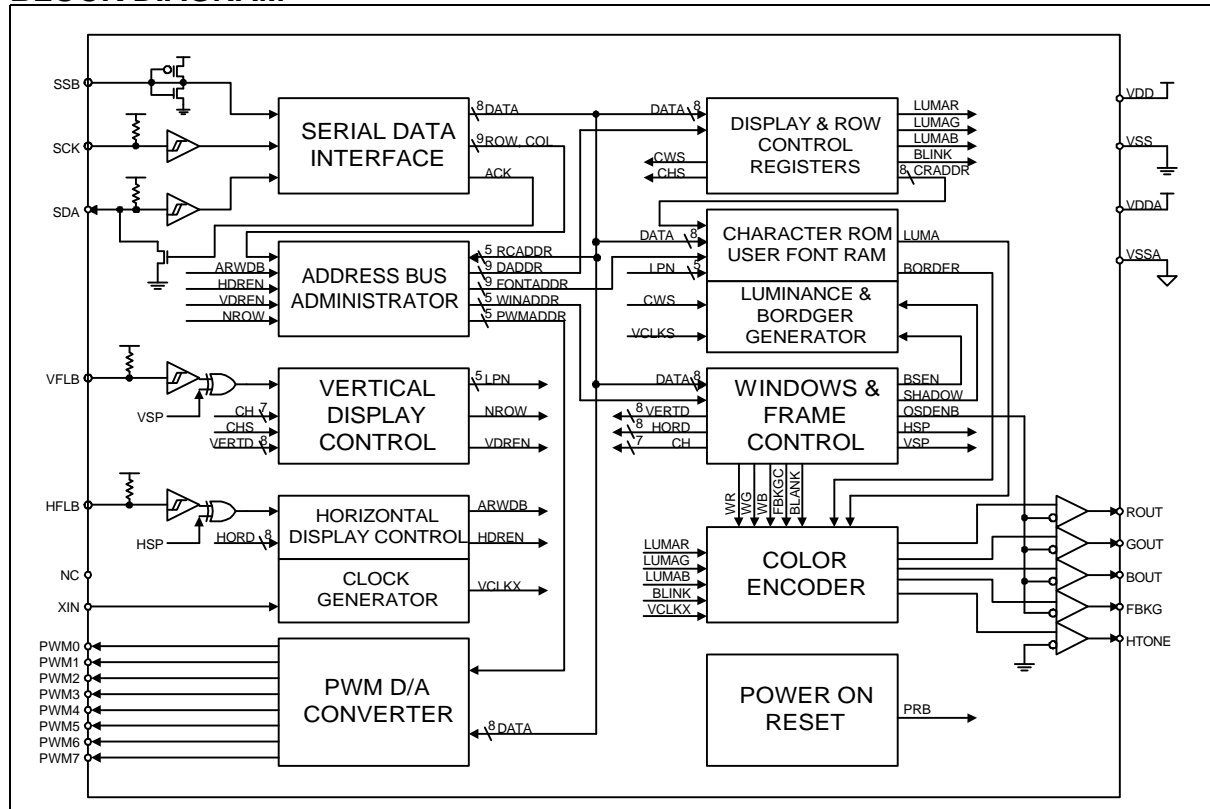
### FEATURES

- Horizontal sync input may be up to 120 KHz.
- Acceptable wide-range pixel clock up to 96MHz from XIN pin.
- Full-screen display consists of 15 (rows) by 30 (columns) characters.
- 12 x 18 dot matrix per character.
- Total of 256 characters and graphic fonts including 248 mask ROM fonts and 8 programmable RAM fonts.
- 8 color selection maximum per display character.
- Double character height and/or width control.
- Programmable positioning for display screen center.
- Bordering, shadowing and blinking effect.
- Programmable vertical character height (18 to 71 lines) control.
- Row to row spacing register to manipulate the constant display height.
- 4 programmable background windows with multi-level operation.
- Software clears for display frame.
- Half tone and fast blanking output.
- 8-channel/8-bit PWM D/A converter output.
- Compatible with SPI bus or I<sup>2</sup>C interface with address 7AH (slave address is mask option).
- 16 or 24-pin PDIP/SOP package.

### GENERAL DESCRIPTION

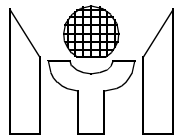
MTV118 is designed for LCD monitor applications to display the built-in characters or fonts onto an LCD monitor screen. The display operates by transferring data and control information from the micro controller to the RAM through a serial data interface. It can execute full screen displays automatically and specific functions such as character bordering, shadowing, blinking, double height and width, font by font color control, frame positioning, frame size control by character height and windowing effect. Moreover, MTV118 also provides 8 PWM DAC channels with 8-bit resolution and a PWM clock output for external digital-to-analog control.

### BLOCK DIAGRAM

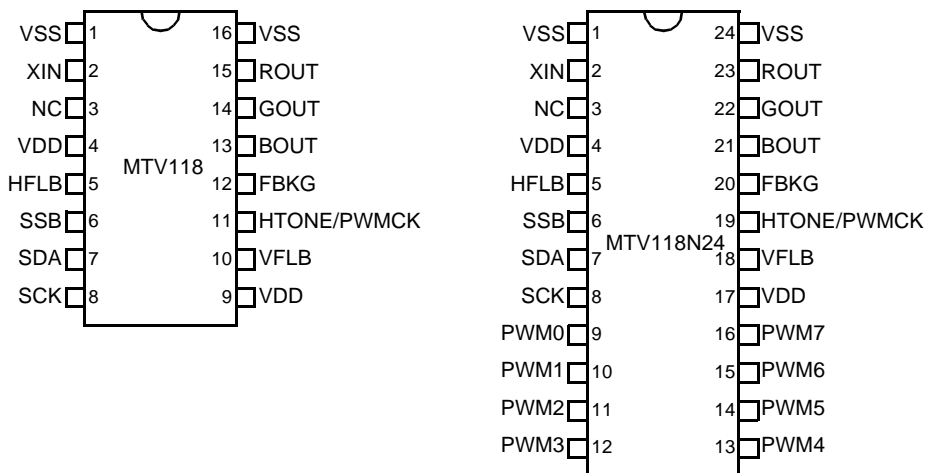


This datasheet contains new product information. Myson Technology reserves the rights to modify the product specification without notice. No liability is assumed as a result of the use of this product. No rights under any patent accompany the sales of the product.



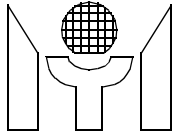


## 1.0 PIN CONNECTION



## 2.0 PIN DESCRIPTIONS

Name	I/O	Pin #		Descriptions
		N16	N24	
VSS	-	1	1	<b>Ground.</b> This ground pin is used for internal circuitry.
XIN	I	2	2	<b>Pixel Clock Input.</b> This is a clock input pin. MTV118 is driven by an external pixel clock source for all the logics inside. The frequency of XIN must be the integral time of pin HFLB.
NC	I	3	3	<b>No connection.</b>
VDD	-	4	4	<b>Power supply.</b> Positive 5 V DC supply for internal circuitry. A 0.1uF decoupling capacitor should be connected across VDD and VSS.
HFLB	I	5	5	<b>Horizontal Input.</b> This pin is used to input the horizontal synchronizing signal. It is a leading edge trigger and has an internal pull-up resistor.
SSB	I	6	6	<b>Serial Interface Enabler.</b> It is used to enable the serial data and is also used to select the operation of I <sup>2</sup> C or SPI bus. If this pin is left floating, I <sup>2</sup> C bus is enabled, otherwise the SPI bus is enabled.
SDA	I	7	7	<b>Serial Data Input.</b> The external data transfers through this pin to internal display registers and control registers. It has an internal pull-up resistor.
SCK	I	8	8	<b>Serial Clock Input.</b> The clock-input pin is used to synchronize the data transfer. It has an internal pull-up resistor.
PWM0	O	-	9	<b>Open-Drain PWM D/A Converter 0.</b> The output pulse width is programmable by the register of row 15, column 19.
PWM1	O	-	10	<b>Open-Drain PWM D/A Converter 1.</b> The output pulse width is programmable by the register of row 15, column 20.
PWM2	O	-	11	<b>Open-Drain PWM D/A Converter 2.</b> The output pulse width is programmable by the register of row 15, column 21.



Name	I/O	Pin #		Descriptions
		N16	N24	
PWM3	O	-	12	<b>Open-Drain PWM D/A Converter 3.</b> The output pulse width is programmable by the register of row 15, column 22.
PWM4	O	-	13	<b>Open-Drain PWM D/A Converter 4.</b> The output pulse width is programmable by the register of row 15, column 23.
PWM5	O	-	14	<b>Open-Drain PWM D/A Converter 5.</b> The output pulse width is programmable by the register of row 15, column 24.
PWM6	O	-	15	<b>Open-Drain PWM D/A Converter 6.</b> The output pulse width is programmable by the register of row 15, column 25.
PWM7	O	-	16	<b>Open-Drain PWM D/A Converter 7.</b> The output pulse width is programmable by the register of row 15, column 26.
VDD	-	9	17	<b>Power Supply.</b> Positive 5 V DC supply for internal circuitry and a 0.1uF decoupling capacitor should be connected across VDD and VSS.
VFLB	I	10	18	<b>Vertical Input.</b> This pin is used to input the vertical synchronizing signal. It is triggered by lead and has an internal pull-up resistor.
HTONE / PWMCK	O	11	19	<b>Half Tone Output / PWM Clock Output.</b> This is a multiplexed pin selected by the PWMCK bit. This pin can be a PWM clock or used to attenuate R, G, B gain of VGA for the transparent windowing effect.
FBKG	O	12	20	<b>Fast Blanking Output.</b> It is used to cut off external R, G, B signals of VGA while this chip is displaying characters or windows.
BOUT	O	13	21	<b>Blue Color Output.</b> This is a blue color video signal output.
GOUT	O	14	22	<b>Green Color Output.</b> This is a green color video signal output.
ROUT	O	15	23	<b>Red Color Output.</b> This is a red color video signal output.
VSS	-	16	24	<b>Ground.</b> This ground pin is used for internal circuitry.

### 3.0 FUNCTIONAL DESCRIPTIONS

#### 3.1 Serial Data Interface

The serial data interface receives data transmitted from an external controller. There are 2 types of bus which can be accessed through the serial data interface: SPI bus and I<sup>2</sup>C bus.

##### 3.1.1 SPI Bus

When the SSB pin is pulled to a HIGH or LOW level, the SPI bus operation is selected. A valid transmission should start from pulling SSB to LOW level, enabling the MTV118 receiving mode and retaining the LOW level until the last cycle for a complete data packet transfer. The protocol is shown in Figure 1 on page 4.

There are 3 transmission formats as shown below:

Format (a) R - C - D → R - C - D → R - C - D

Format (b) R - C - D → C - D → C - D → C - D

Format (c) R - C - D → D → D → D → D → D

R=row address, C=column address, D=display data

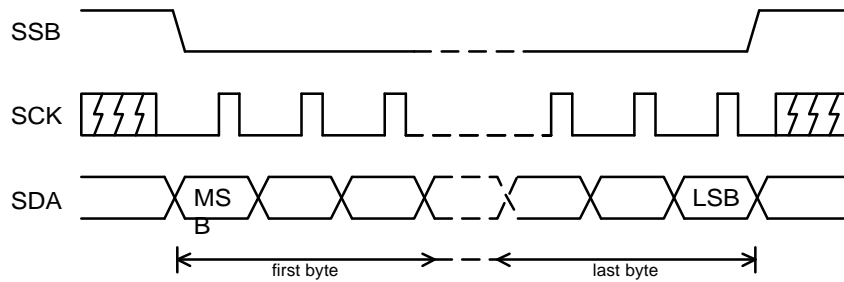
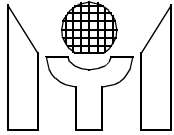


FIGURE 1. Data Transmission Protocol (SPI)

3.1.2 I<sup>2</sup>C Bus

I<sup>2</sup>C bus operation is only selected when the SSB pin is left floating. A valid transmission should begin from writing the slave address 7AH, which is mask option, to MTV118. The protocol is shown in Figure 2 on page 4..

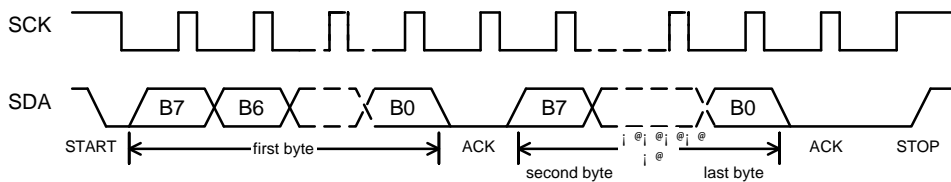


FIGURE 2. Data Transmission Protocol (I<sup>2</sup>C)

There are 3 transmission formats as shown below:

Format (a) S - R - C - D → R - C - D → R - C - D

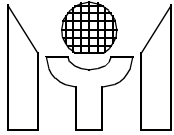
Format (b) S - R - C - D → C - D → C - D → C - D

Format (c) S - R - C - D → D → D → D → D → D

S=slave address, R=row address, C=column address, D=display data

Each arbitrary length of data packet consists of 3 portions: row address (R), column address (C) and display data (D). Format (a) is suitable for updating small amounts of data which will be allocated with different row and column addresses. Format (b) is recommended for updating data that has the same row address but a different column address. Massive data updating or full screen data changes should be done in format (c) to increase transmission efficiency. The row and column addresses will be incremented automatically when format (c) is applied. Furthermore, the undefined locations in display or font RAM should be filled with dummy data.

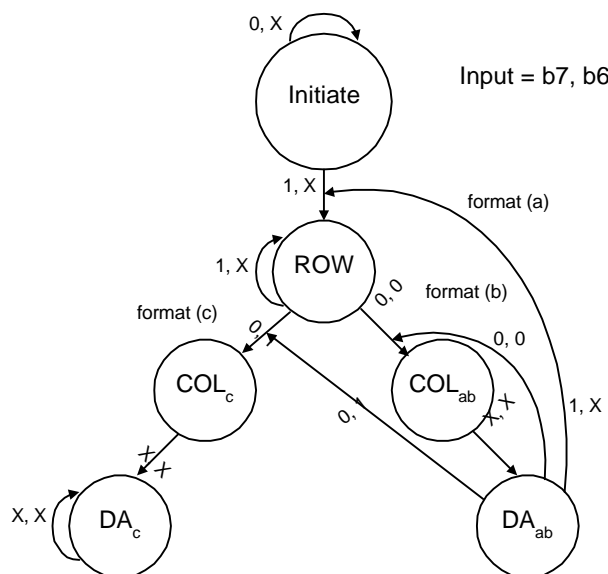
There are 3 types of data which should be accessed through the serial data interface: address bytes of display registers, attribute bytes of display registers and user font RAM data. The protocol is the same for all except bits 5 and 6 of the row addresses. The MSB(b7) is used to distinguish row and column addresses when transferring data from an external controller. Bit 6 of the row address is used to distinguish display registers and user font RAM data and bit6 of the column address is used to differentiate the column address for formats (a), (b) and (c), respectively. Bit 5 of the row address for display registers is used to distinguish the address byte when it is set to "0" and the attribute byte when it is set to "1". The configuration of transmission formats is shown in Table 1 on page 5.



**TABLE 1. Configuration of Transmission Formats**

	Address	b7	b6	b5	b4	b3	b2	b1	b0	Format
<b>Address Bytes of Display Reg.</b>	Row	1	0	0	x	R3	R2	R1	R0	a,b,c
	Column <sub>ab</sub>	0	0	x	C4	C3	C2	C1	C0	a,b
	Column <sub>c</sub>	0	1	x	C4	C3	C2	C1	C0	c
<b>Attribute Bytes of Display Reg.</b>	Row	1	0	1	x	R3	R2	R1	R0	a,b,c
	Column <sub>ab</sub>	0	0	x	C4	C3	C2	C1	C0	a,b
	Column <sub>c</sub>	0	1	x	C4	C3	C2	C1	C0	c
<b>User Fonts RAM</b>	Row	1	1	x	x	x	R2	R1	R0	a,b,c
	Column <sub>ab</sub>	0	0	C5	C4	C3	C2	C1	C0	a,b
	Column <sub>c</sub>	0	1	C5	C4	C3	C2	C1	C0	c

The data transmission is permitted to change from format (a) to format (b) and (c), or from format (b) to format (a), but not from format (c) back to format (a) and (b). The alternation between transmission formats is configured as the state diagram shown in Figure 3 on page 5.



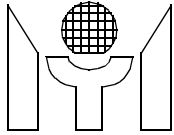
**FIGURE 3. Transmission State Diagram**

**3.2 Address Bus Administrator**

The administrator manages bus address arbitration of internal registers or user font RAM during external data write-in. The external data write through serial data interface to registers must be synchronized by internal display timing. In addition, the administrator also provides automatic incrementation to the address bus when external writing occurs using format (c).

**3.3 Vertical Display Control**

The vertical display control can generate different vertical display sizes for most display standards in current monitors. The vertical display size is calculated with the information of a double character height bit(CH5) and a vertical display height control register(CH6-CH0).The algorithms of a repeating character line display are shown in Tables 2 and 3. The programmable vertical size range is 270 lines to maximum 2130 lines.



The vertical display center for a full-screen display may be figured out according to the information of the vertical starting position register (VERTD) and VFLB input. The vertical delay starting from the leading edge of VFLB is calculated using the following equation:

$$\text{Vertical delay time} = (\text{VERTD} * 4 + 1) * H$$

Where H = 1 horizontal line display time

**TABLE 2. Repeat Line Weight of Character**

CH6-CH0	Repeat Line Weight
CH6,CH5=11	+18*3
CH6,CH5=10	+18*2
CH6,CH5=0x	+18
CH4=1	+16
CH3=1	+8
CH2=1	+4
CH1=1	+2
CH0=1	+1

**TABLE 3. Repeat Line Number of Character**

Repeater Line Weight	Repeat Line #																	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
+1	-	-	-	-	-	-	-	-	v	-	-	-	-	-	-	-	-	-
+2	-	-	-	-	v	-	-	-	-	-	-	-	v	-	-	-	-	-
+4	-	-	v	-	-	-	v	-	-	-	v	-	-	-	v	-	-	-
+8	-	v	-	v	-	v	-	v	-	v	-	v	-	v	-	v	-	-
+16	-	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	-
+17	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	-
+18	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v

Note: "v" means the nth line in the character would be repeated once, while "-" means the nth line in the character would not be repeated.

### 3.4 Horizontal Display Control

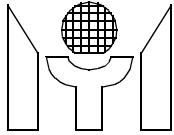
The horizontal display control is used to generate control timing for a horizontal display based on double character width bit (CWS), horizontal positioning register (HORD) and HFLB input. A horizontal display line includes 360 dots for 30 display characters and the remaining dots for a blank region. The horizontal delay starting from the HFLB leading edge is calculated using the following equation:

$$\text{Horizontal delay time} = (\text{HORD} * 6 + 49) * P$$

Where P = 1 XIN pixel display time

### 3.5 Display & Row Control Registers

The internal RAM contains display and row control registers. The display registers have 450 locations which are allocated between row 0/column 0 and row 14/column 29 as shown in Figure 4. Each display register has its corresponding character address on the address byte, and 1 blink bit and its corresponding color bits on attribute bytes. The row control register is allocated at column 30 for row 0 to row 14; it is used to set character size for each respective row. If the double width character (CWS) is cho-



sen, only even column characters may be displayed on-screen and the odd column characters will be hidden.

ROW #	COLUMN #					
	0	1	28	29	30	31
0	DISPLAY REGISTERS				ROW CTRL REG	RESERVED
1						
13						
14						

ROW 15	COLUMN#											
	0	2	3	5	6	8	9	11	12	18	19	26
	WINDOW1		WINDOW2		WINDOW3		WINDOW4		FRAME CTRL REG		PWM D/A CTRL REG	

**FIGURE 4. Memory map**

**3.5.1 Register Descriptions**

1. (i) Display Register, (Row 0 - 14, Column 0 - 29)

ADDRESS BYTE

b7	b6	b5	b4	b3	b2	b1	b0
CRADDR							
MSB				LSB			

CRADDR - Defines ROM character and user-programmable fonts address.

(a) 0 ~ 247 ⇒ 248 built-in characters and graphic symbols

(b) 248 ~ 255 ⇒ 8 user-programmable fonts

ATTRIBUTE BYTE

b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	BLINK	R1	G1	B1

BLINK - Enables blinking effect when this bit is set to " 1 ". The blinking is alternated per 32 vertical frames.

R1, G1, B1 - These bits are used to specify its relative address character color 1.

2. Row Control Registers, (Row 0 - 14)

COLN 30	b7	b6	b5	b4	b3	b2	b1	b0
	-	-	-	R2	G2	B2	CHS	CWS

R2, G2, B2 - These bits are used to specify its relative row character color 2. While the corresponding CCS bit is set to 1, color 2 should be chosen.

CHS - Defines double height character to the respective row.

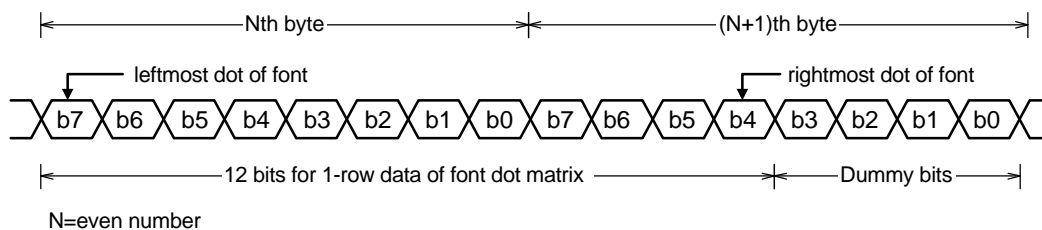
CWS - Defines double width character to the respective row.

### 3.6 User Font RAM

The user font RAM has 288 locations which are allocated between row 0/column 0 and row 7/column 35 to specify 8 user-programmable fonts, as shown in Figure 5. Each programmable font consists of a 12x18 dot matrix. Each row of dot matrix consists of 2 bytes of data which include 4 dummy bits as shown in figure 6. That is, the dot matrix data of each font is stored in 36-byte registers. For example, font 0 is stored in row 0 from column 0 to column 35 and font 1 is stored in row 1 from column 0 to column 35, etc.

ROW #	COLUMN #					
	0	1	34	35	36	63
0	USER FONT RAM				RESERVED	
1						
2						
3						
4						
5						
6						
7						

**FIGURE 5. User Font RAM Memory Map**



**FIGURE 6. Data Format of Font Dot Matrix**

### 3.7 Character ROM

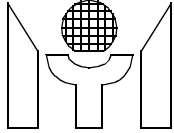
The character ROM contains 248 built-in characters and symbols from addresses 0 to 247. Each character and symbol consists of a 12x18 dot matrix. The detail pattern structures for each character and symbol are shown in 10.0“CHARACTER AND SYMBOL PATTERN” on page 15.

### 3.8 Luminance & Border Generator

There are 2 shift registers included in the design which can shift out of luminance and border dots to the color encoder. The bordering and shadowing feature is configured in this block. For bordering effect, the character will be enveloped with blackedge on 4 sides. For shadowing effect, the character is enveloped with blackedge on right and bottom sides only.

### 3.9 Window and Frame Control

The display frame position is completely controlled by the contents of VERTD and HORD. The window size and position control are specified in columns 0 to 11 on row 15 of the memory map, as shown in Figure 4. Window 1 has the highest priority and window 4 has the least, when 2 windows are overlapping. More detailed information is described as follows:



## 1. Window control registers:

### ROW 15

Column	b7	b6	b5	b4	b3	b2	b1	b0
0,3,6,OR 9	ROW START ADDR				ROW END ADDR			
	MSB				LSB			

Column	b7	b6	b5	b4	b3	b2	b1	b0
1,4,7,OR 10	COL START ADDR				WEN	CCS	-	
	MSB				LSB			

Column	b7	b6	b5	b4	b3	b2	b1	b0
2,5,8,OR 11	COL END ADDR				R	G	B	
	MSB				LSB			

START(END) ADDR - These addresses are used to specify the window size. It should be noted that when the start address is greater than the end address, the window will be disabled.

WEN - Enables the window display.

CCS - When a window is overlapping with the character, character color 2 should be chosen while this bit is set to 1. Color 1 is selected otherwise.

R, G, B - Specifies the color of the relative background window.

## 2. Frame control registers:

### ROW 15

Column 12	b7	b6	b5	b4	b3	b2	b1	b0
	VERTD							
	MSB							
	LSB							

VERTD - Specifies the starting position for vertical display. The total steps are 256, and the increment of each step is 4 horizontal display lines. The initial value is 4 after power-up.

Column 13	b7	b6	b5	b4	b3	b2	b1	b0
	HORD							
	MSB							
	LSB							

HORD - Defines the starting position for horizontal display. The total steps are 256 and the increment of each step is 6 dots. The initial value is 15 after power-up.

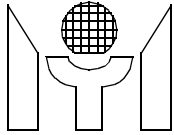
Column 14	b7	b6	b5	b4	b3	b2	b1	b0
	-	CH6	CH5	CH4	CH3	CH2	CH1	CH0

CH6-CH0 - Defines the character vertical height, which is programmable from 18 to 71 lines. The character vertical height is at least 18 lines if the contents of CH6-CH0 are less than 18. For example, when the content is " 2 ", the character vertical height is regarded as equal to 20 lines. If the contents of CH4-CH0 are greater than or equal to 18, it will be regarded as equal to 17. See Tables 2 and 3 for a detailed description of this operation.

Column 15	b7	b6	b5	b4	b3	b2	b1	b0
	Reserved							

This byte is reserved for internal testing.





Column 16	b7	b6	B5	b4	b3	b2	b1	b0
	-	-	-	RSPACE				MSB

RSPACE - Defines the row to row spacing in each unit of the horizontal line. That is, extra RSPACE horizontal lines will be appended below each display row, and the maximum space is 31 lines. The initial value is "0" after power-up.

Column 17	b7	b6	b5	b4	b3	b2	b1	b0
	OSDEN	BSEN	SHADOW	TRIC	BLANK	WENCLR	RAMCLR	FBKGC

OSDEN - Activates the OSD operation when this bit is set to "1". The initial value is "0" after power-up.

BSEN - Enables the bordering and shadowing effect.

SHADOW - Activates the shadowing effect if this bit is set, otherwise the bordering is chosen.

TRIC - Defines the driving state of output pins ROUT, GOUT, BOUT and FBKG when OSD is disabled. That is, while OSD is disabled, these 4 pins will drive LOW if this bit is set to "1", otherwise these pins are in high-impedance state. The initial value is "0" after power-up.

BLANK - Forces the FBKG pin output to HIGH while this bit is set to "1".

WENCLR - Clears all WEN bits of window control registers when this bit is set to "1". The initial value is "0" after power-up.

RAMCLR - Clears all ADDRESS bytes of display registers when this bit is set to "1". The initial value is "0" after power-up.

FBKGC - Defines the output configuration for FBKG pin. When it is set to "0", the FBKG outputs during the display of characters or windows, otherwise, it outputs only during the display of characters.

Column 18	B7	b6	b5	b4	b3	b2	b1	b0
	TEST	FBKGP	PWMCK	DWE	HSP	VSP	PWM1	PWM0

**TEST - = 0 ⇒ Normal mode.**  
**= 1 ⇒ Test mode, not allowed in applications.**

FBKGP - Selects the polarity of the output pin FBKG.  
 = 1 ⇒ Positive polarity FBKG output is selected.  
 = 0 ⇒ Negative polarity FBKG output is selected.  
 The initial value is "1" after power-up.

PWMCK - Selects the output options to the HTONE/PWMCK pin.  
 = 0 ⇒ HTONE option is selected.  
 = 1 ⇒ PWMCK option is selected with 50/50 duty cycle and is synchronous with the input HFLB. The frequency is selected by PWM1, PWM0 as shown in table 4.  
 The initial value is "0" after power-up.

DWE - Enables double width. When the bit is set to "1", the display of the OSD menu can change to half resolution for double character width, and then the number of pixels of each line should be even.

HSP - = 1 ⇒ Accepts positive polarity Hsync input.

= 0 ⇒ Accepts negative polarity Hsync input.

VSP - = 1 ⇒ Accepts positive polarity Vsync input.  
 = 0 ⇒ Accepts negative polarity Vsync input.

PWM1, PWM0 - Selects the PWMCK output frequency.  
 = (0, 0) ⇒ XIN frequency /8  
 = (0, 1) ⇒ XIN frequency /4  
 = (1, 0) ⇒ XIN frequency /2  
 = (1, 1) ⇒ XIN frequency /1  
 The initial value is 0, 0 after power-up.

**Notes :** When XIN is not present, don't write data in any address. If data is written in any address, a malfunction may occur.

**TABLE 4.** PWMCK Frequency and PWMDA Sampling Rate

(PWM1, PWM0)	PWMCK Freq.	PWMDA sampling rate
( 0, 0 )	XIN frequency /8	XIN frequency /(8 * 256)
( 0, 1 )	XIN frequency /4	XIN frequency /(4 * 256)
( 1, 0 )	XIN frequency /2	XIN frequency /(2 * 256)
( 1, 1 )	XIN frequency /1	XIN frequency /(1 * 256)

### 3.10 PWM D/A Converter

There are 8 open-drain PWM D/A outputs (PWM0 to PWM7). The PWM D/A converter output pulse width is programmable by writing data to columns 19-26 registers of row 15 with 8-bit resolution to control the pulse width duration from 0/256 to 255/256. The sampling rate is selected by PWM1, PWM0 as shown in table 4. In applications, all open-drain output pins should be pulled up by external resistors to supply voltage (5V to 9V) for the desired output range.

ROW 15

	b7	b6	b5	b4	b3	b2	b1	b0
Column 19	PWMDA0							
Column 26	PWMDA7							
	MSB							LSB

PWMDA0 - PWMDA7 - Defines the output pulse width of pins PWM0 to PWM7.

### 3.11 Color Encoder

The decoder generates the video output to ROUT, GOUT and BOUT by integrating window color, border blackedge, luminance output and color selection output (R, G, B) to form the desired video outputs.

## 4.0 ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage(VDD,VDDA)	-0.3 to +7 V
Ground Voltage	-0.3 to VDD+0.3 V
Storage Temperature	-65 to +150 °C
Ambient Operating Temperature	0 to +70 °C

## 5.0 OPERATING CONDITIONS

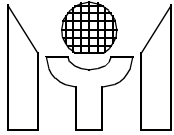
DC Supply Voltage(VDD,VDDA)	+4.75 to +5.25 V
Operating Temperature	0 to +70 °C

## 6.0 ELECTRICAL CHARACTERISTICS (Under Operating Conditions)

Symbol	Parameter	Conditions(Notes)	Min.	Max.	Unit
V <sub>IH</sub>	Input High Voltage	-	0.7 * VDD	VDD+0.3	V
V <sub>IL</sub>	Input Low Voltage	-	VSS-0.3	0.3 * VDD (0.2*VDD for SSB pin )	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> ≥ -24 mA	VDD-0.8	-	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> ≤ 24 mA	-	0.5	V
V <sub>ODH</sub>	Open Drain Output High Voltage	- (For all OD pins, pulled up by external 5 to 9V power supply)	5	9	V
V <sub>ODL</sub>	Open Drain Output Low Voltage	5 mA ≥ I <sub>DOL</sub> ( For all OD pins )	-	0.5	V
I <sub>SB</sub>	Standby Current	V <sub>in</sub> = VDD, I <sub>load</sub> = 0uA	-	12	mA
I <sub>CC</sub>	Operating Current	Pixel rate=96MHz I <sub>load</sub> = 0uA	-	20	mA

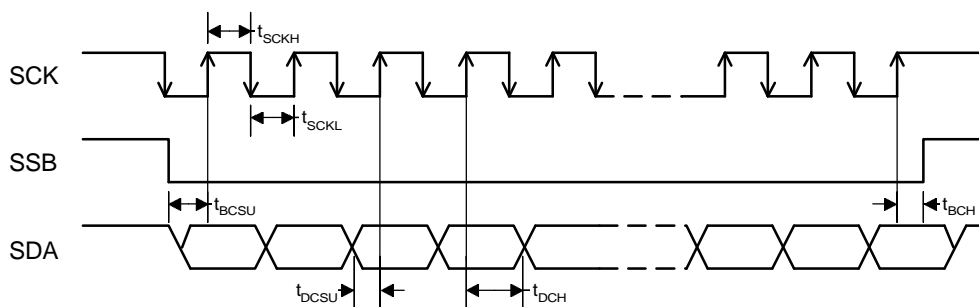
## 7.0 SWITCHING CHARACTERISTIC (Under Operating Conditions)

Symbol	Parameter	Min.	Typ.	Max.	Unit
f <sub>HFLB</sub>	HFLB input frequency	15	-	120	KHz
T <sub>r</sub>	Output rise time	-	-	5	ns
T <sub>f</sub>	Output fall time	-	-	5	ns
t <sub>BCSU</sub>	SSB to SCK set-up time	200	-	-	ns
t <sub>BCH</sub>	SSB to SCK hold time	100	-	-	ns
t <sub>DCSU</sub>	SDA to SCK set-up time	200	-	-	ns
t <sub>DCH</sub>	SDA to SCK hold time	100	-	-	ns
t <sub>SCKH</sub>	SCK HIGH time	500	-	-	ns
t <sub>SCKL</sub>	SCK LOW time	500	-	-	ns
t <sub>SU:STA</sub>	START condition set-up time	500	-	-	ns
t <sub>HD:STA</sub>	START condition hold time	500	-	-	ns
t <sub>SU:STO</sub>	STOP condition set-up time	500	-	-	ns

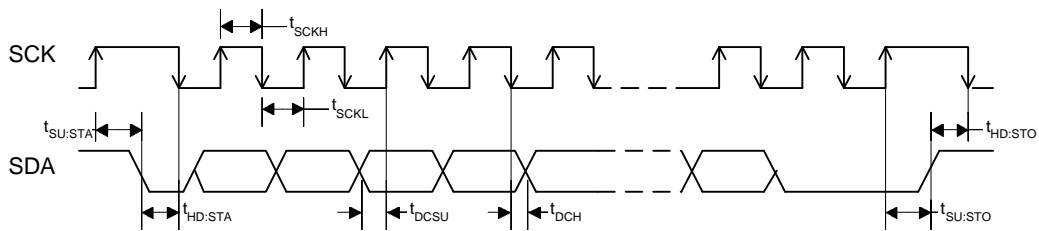


Symbol	Parameter	Min.	Typ.	Max.	Unit
$t_{HD:STO}$	STOP condition hold time	500	-	-	ns
$t_{SETUP}$	HFLB delay to rising edge of pixel clock	2		6	ns
$t_{HOLD}$	minimum pulse width of HFLB	25			ns
$t_{pd}$	propagation delay of output to pixel clock			10	ns
PIXin	pixel clock input	6		96	MHz

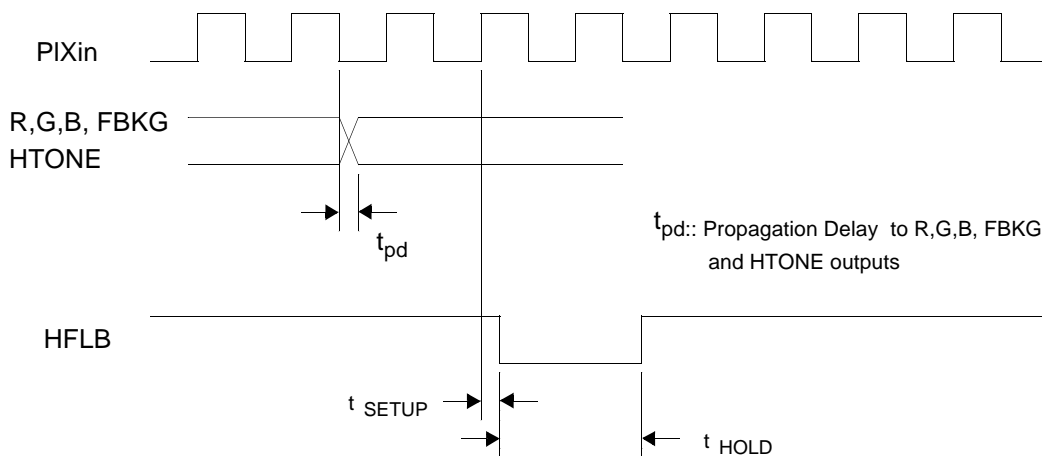
**8.0 TIMING DIAGRAMS**



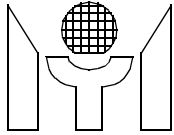
**FIGURE 7. Data Interface Timing (SPI)**



**FIGURE 8. Data Interface Timing (I<sup>2</sup>C)**



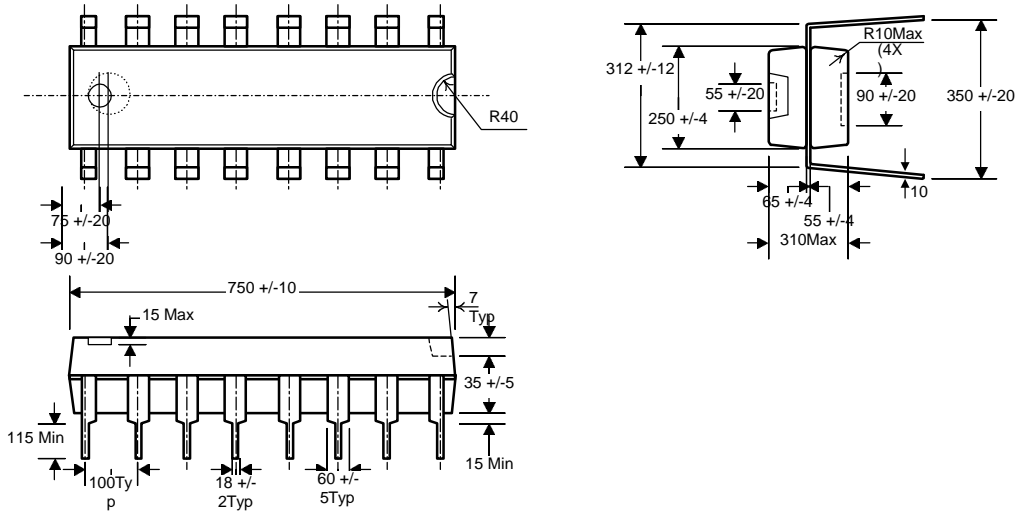
**FIGURE 9. Output and HFLB Timing to Pixel Clock**



**9.0 PACKAGE DIMENSION**

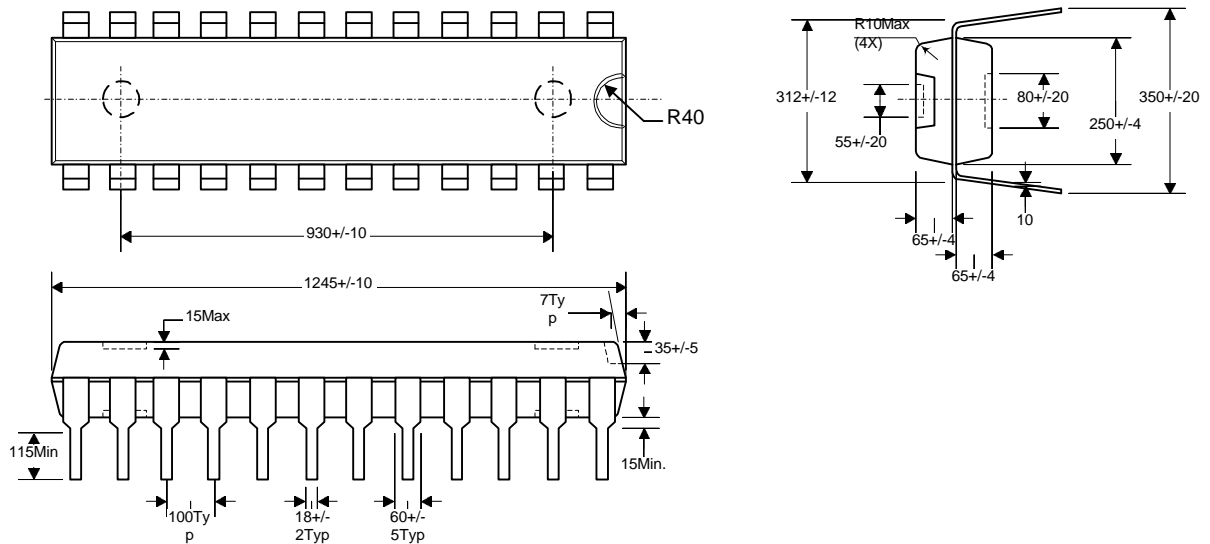
**9.1 16 PDIP 300Mil**

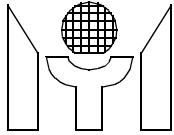
Unit:Mil



**9.2 24 PDIP 300Mil**

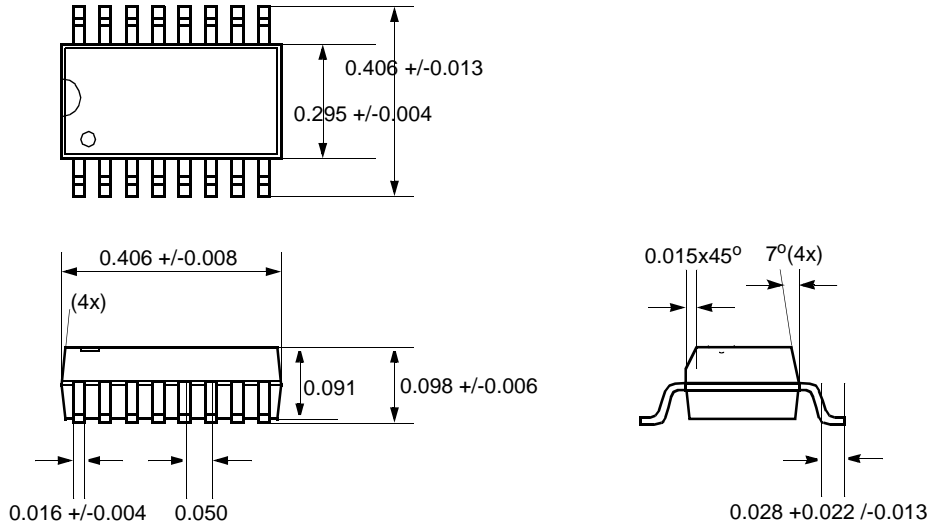
Unit: Mil



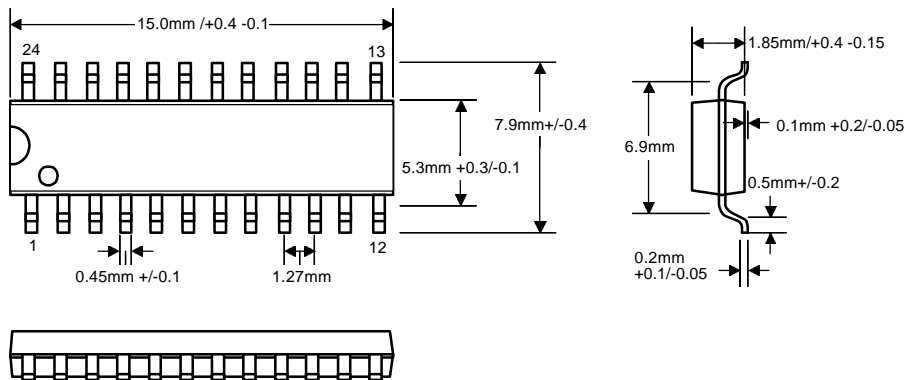


**9.3 16-pin SOP 300Mil**

Unit: Mil



**9.4 24-pin SOP 300Mil**



**10.0 CHARACTER AND SYMBOL PATTERN**

Please see the attachment.