M50427FP

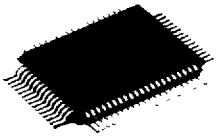
CD PLAYER DIGITAL SIGNAL PROCESSOR

DESCRIPTION

The M50427FP is a CMOS IC developed for compact disc (CD) sound reproducing applications. It has adjustment-free PLL, error correction circuitry, etc. and is used in a CD digital signal processing section. Applications include also CD-ROM and CD-G, as well as CD-DA.

FEATURES

- Adjustment free EFM-PLL circuit (built-in VCO)
- ± 8 frames jitter margin
- Easy-to-handle CLV servo commands
- Subcode parallel/serial interface
- 2 times over sampling
- Capable of double speed sound reproduction



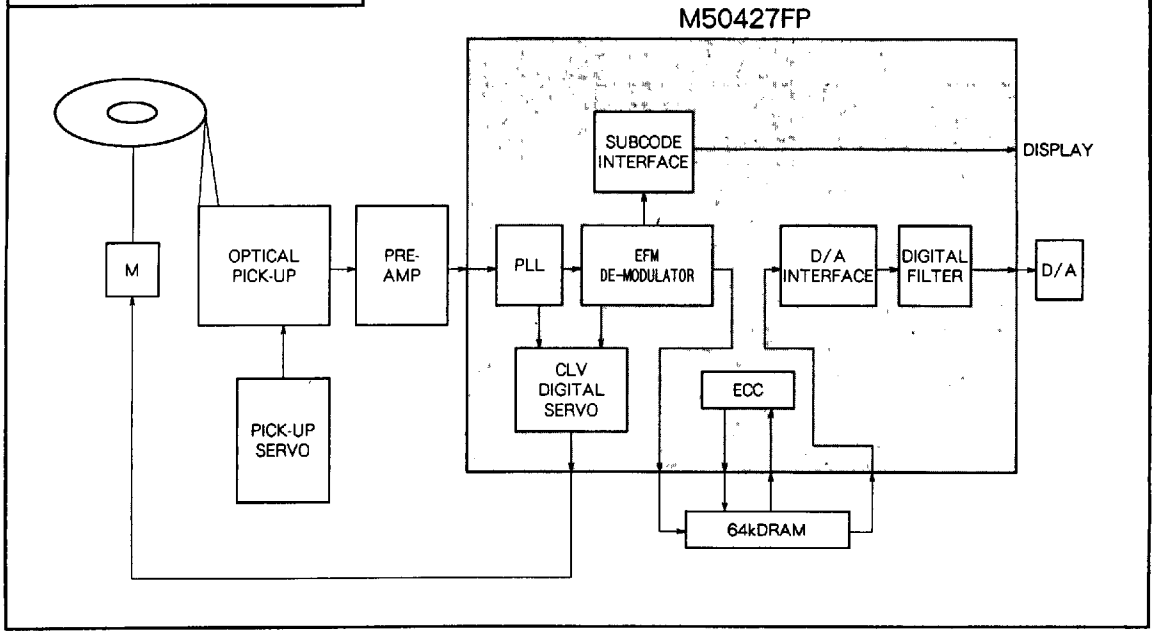
Outline 72P6-B

0.8mm pitch QFP
(18.0mm × 13.2mm × 2.0mm)

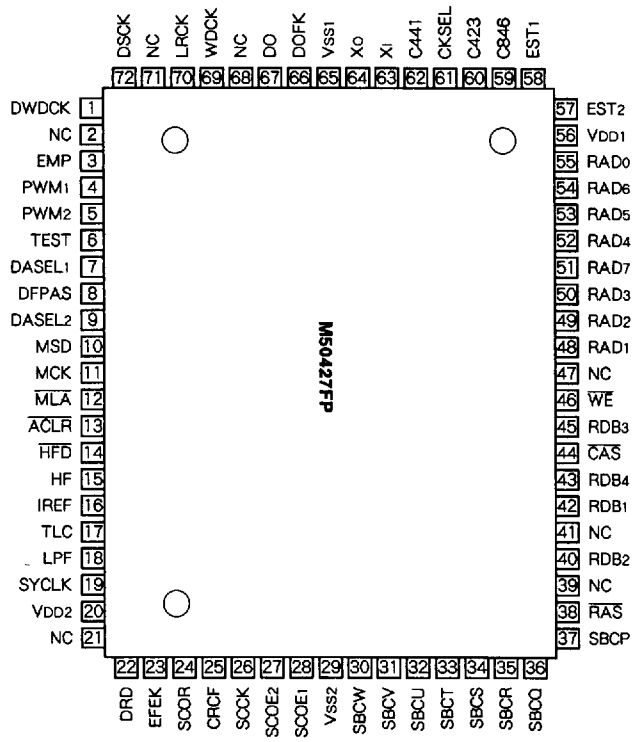
RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... V_{DD} = 4.5~5.5V
Rated voltage range ..... V_{DD} = 5V
Rated power dissipation 90mW

SYSTEM CONFIGURATION



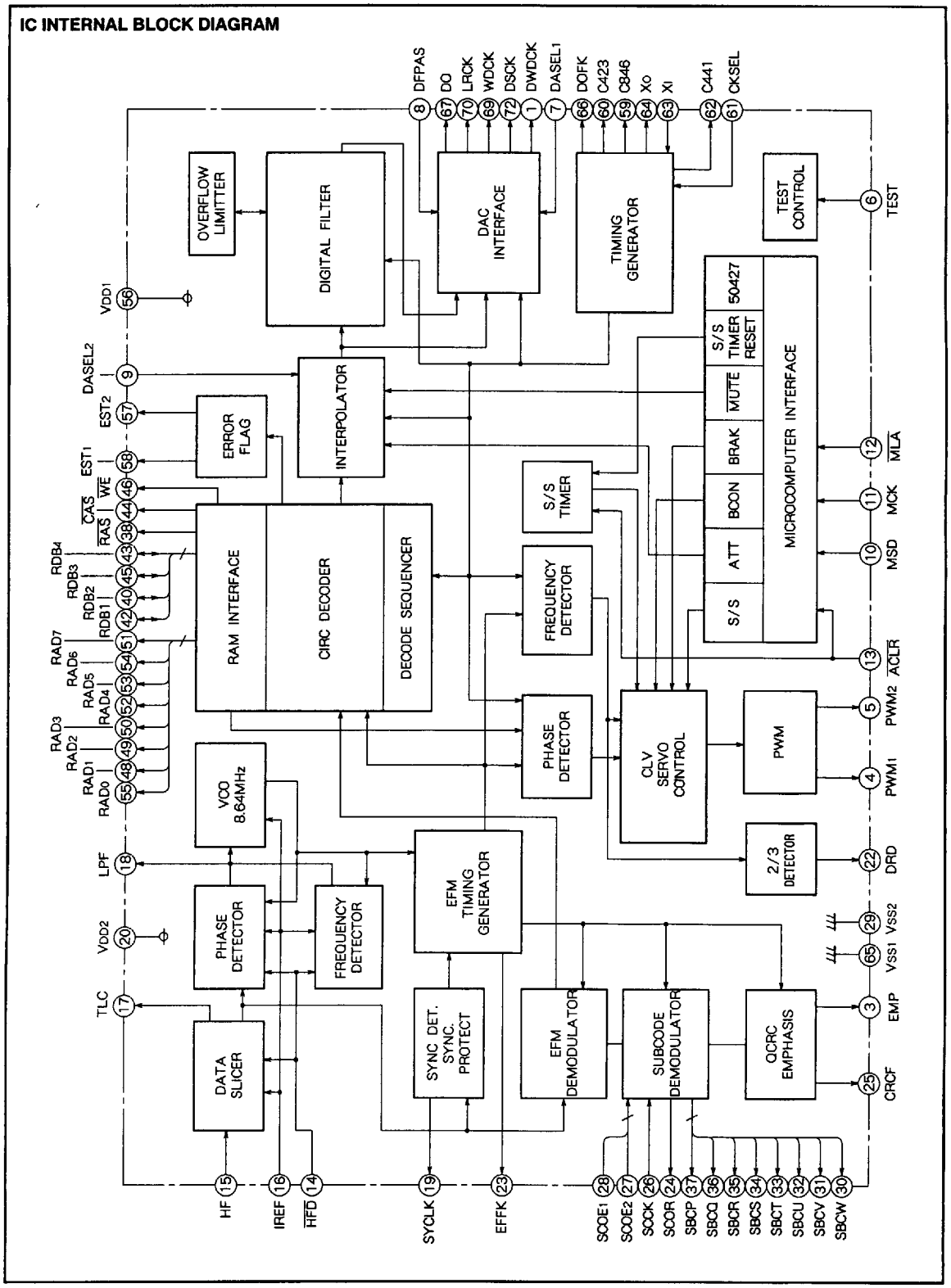
PIN CONFIGURATION



Outline 72P6-B

NC : NO CONNECTION

IC INTERNAL BLOCK DIAGRAM



PIN DESCRIPTION

Name	I/O	Function
DWDCK	O	Mode3 word clock to DAC
EMP	O	Emphasis flag output, Emphasis = 1
PWM_1	O	Disc motor driving PWM output 1, −
PWM_2	O	Disc motor driving PWM output 2, +
TEST	I	Test control input, Normal = 0
$DASEL_1$	I	DAC interface format select 1
DFPAS	I	Digital filter pass select, Bypass = 1
$DASEL_2$	I	DAC interface format select 2
MSD	I	Microcomputer interface serial data input
MCK	I	Microcomputer interface shift clock input
$\overline{MLA}$	I	Microcomputer interface data latch clock input
$\overline{ACLR}$	I	Microcomputer interface register clear input, All clear = 0 SS timer reset = 1 MUTE, S/S, BCON = 0 become
$\overline{HFD}$	I	High frequency detect
HF	I	High frequency input
IREF	I	Current referance
TLC	O	Output from slice level control
LPF	I/O	PLL loop filter
SYCLK	O	Frame lock status output, Lock = 1
V_{DD2}	I	V_{DD} for data slicer and VCO
DRD	O	Low disc rotation status
EFFK	O	EFM frame clock duty = 50 %
SCOR	O	Subcode sync output $S_0 + S_1$
CRCF	O	Subcode Q, CRC check flag output CROCK = 1
SCCK	I	Shift clock input for serial subcode data output
$SCOE_2$	I	Enable input of subcode T~Wch output 0 : High Z
$SCOE_1$	I	Enable input of subcode P~Sch output 0 : High Z
V_{SS2}	I	Ground
SBCW	O	Subcode Wch output
SBCV	O	Subcode Vch output
SBCU	O	Subcode Uch output
SBCT	O	Subcode Tch output
SBCS	O	Subcode Sch output
SBCR	O	Subcode Rch output

Name	I/O	Function
SBCQ	O	Subcode Qch output
SBCP	O	Subcode Pch output Pch~Wch serial data output
$\overline{RAS}$	O	Row address strobe output to RAM
RDB_2	I/O	Data input/output 2 to RAM
RDB_1	I/O	Data input/output 1 to RAM
RDB_4	I/O	Data input/output 4 to RAM
$\overline{CAS}$	O	Column address strobe output to RAM
RDB_3	I/O	Data input/output 3 to RAM
$\overline{WE}$	O	Write enable output to RAM
RAD_1	O	Address output 1 to RAM
RAD_2	O	Address output 2 to RAM
RAD_3	O	Address output 3 to RAM
RAD_7	O	Address output 7 to RAM
RAD_4	O	Address output 4 to RAM
RAD_5	O	Address output 5 to RAM
RAD_6	O	Address output 6 to RAM
RAD_0	O	Address output 0 to RAM
V_{DD1}	I	Power supply 5V
EST_2	O	Error status 2, Error to be interpolated detected at C2 decoder = 1
EST_1	O	Error status 2, Error detected at C1 decoder = 1
C846	O	Clock output 8.4672MHz
C423	O	Clock output 4.2336MHz, duty = 50 %
CKSEL	I	Crystal selector input L = 8.4672MHz H = 16.9344MHz
C441	O	Clock output 44.1kHz (crystal = 16.9344MHz)
X_I	I	Crystal oscillator input with internal feedback resister
X_O	O	Crystal oscillator output
V_{SS1}	I	Ground
DOFK	O	OSC frame clock output 7.35kHz, duty = 50 %
DO	O	Serial data output to DAC
WDCK	O	Word clock to DAC or APTL clock
LRCK	O	Lch/Rch clock to DAC or APTR clock
DSCK	O	Data shift clock to DAC

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{DD}-V_{SS}	Supply voltage		−0.3～+7.0	V
V_I	Input voltage	(R_P = 0 Ω)	V_{SS}-0.3≦ V_I ≦ V_{DD}+0.3	V
V_O	Output voltage	(R_P = 0 Ω)	V_{SS}-0.3 ≦ V_O ≦ V_{DD}	V
V_P	Pull up voltage		V_P ≦ V_{DD} + 2mA * R_P	V
T_{opr}	Operating temperature		−10～+70	℃
T_{stg}	Storage temperature		−40～+125	℃
P_d	Power dissipation		350	mW

R_P : Pulling up resistor

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test conditions	Applied pin	Limits			Unit
				Min	Typ	Max	
V_{DD}	Supply voltage			3.5	5.0	5.5	V
V_{IH1}	High-level input voltage 1		2)	V_{DD} *0.5	–	V_{DD}	V
V_{IH2}	High-level input voltage 2		1)	V_{DD} *0.7	–	V_{DD}	V
V_{IL1}	Low-level input voltage 1		2)	Vss	–	V_{DD} *0.08	V
V_{IL2}	Low-level input voltage 2		1)	Vss	–	V_{DD} *0.3	V
fosc	Oscillation frequency (X'tal)			–	8.46	–	MHz
fvco	Oscillation frequency (VCO)			–	8.64	–	MHz

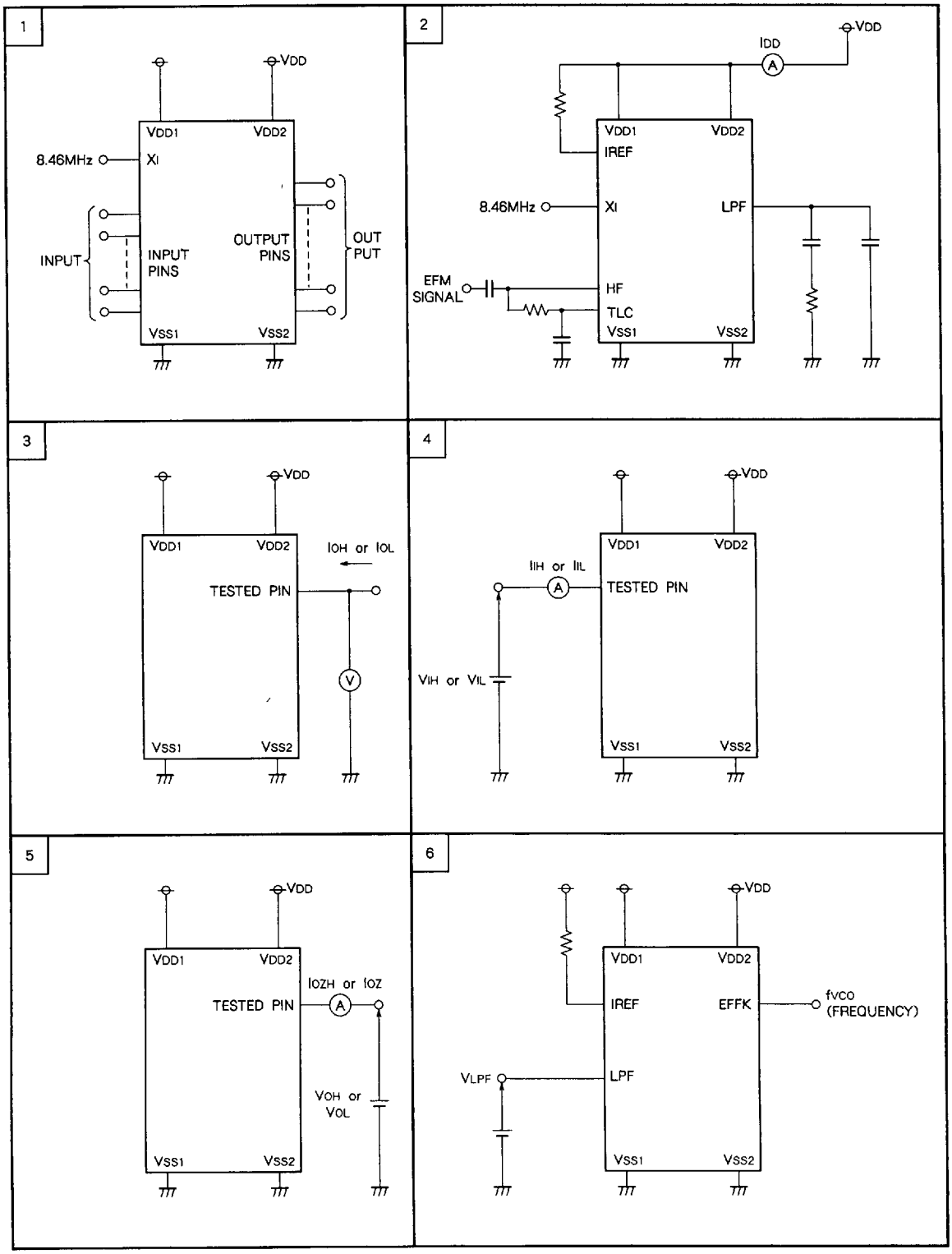
Note 1. Applied pin
1) DASEL1, DFPAS, DASEL2, CKSEL, TEST
2) HFD, SCOE1, SCOE2, SCCK, MSD, MCK, MLA, ACLR, RDB1～RDB4

ELECTRICAL CHARACTERISTICS (Ta = 25℃, V_{DD} = 5V, unless otherwise noted)

Symbol	Parameter	Test conditions	Applied pin	Test circuit	Limits			Unit
					Min	Typ	Max	
V_{DD}	Supply voltage	T_a = −10～+70℃		1	3.5	5.0	5.5	V
I_{DD}	Circuit current	fosc = 8.4672MHz fvco = 8.6436MHz		2	–	15	30	mA
V_{OH}	High-level output voltage	V_{DD}=4.5V, I_{OH}=−0.8mA	3)	3	3.5	–	–	V
V_{OL}	Low-level output voltage	V_{DD}=4.5V, I_{OL}=0.8mA	3)	3	–	–	0.4	V
I_{IH}	High-level input current	V_{IH}=4.5V	4)	4	–	–	2	μA
I_{IL}	Low-level input current	V_{IL}=0.5V	4)	4	–	–	−2	μA
I_{OZH}	Off state high-level output current	V_{OH}=4.5V	5)	5	–	–	2	μA
I_{OZL}	Off state low-level output current	V_{OL}=0.5V	5)	5	–	–	−2	μA
fvco1	VCO (EFFK) Free running frequency	V_{LPF}= 1.0V		6	–	–	3.0	kHz
fvco2		V_{LPF}= 2.5V		6	8.0	10.0	–	kHz
fvco3		V_{LPF}= 4.0V		6	11.0	–	–	kHz

Note 2. Applied pin
3) Output and input/output pin except XO, TLC, LPF
4) Input pin except XI, IREF
5) RDB1～RDB4, SBCP～SBCW

TEST CIRCUIT



FUNCTIONAL DESCRIPTION

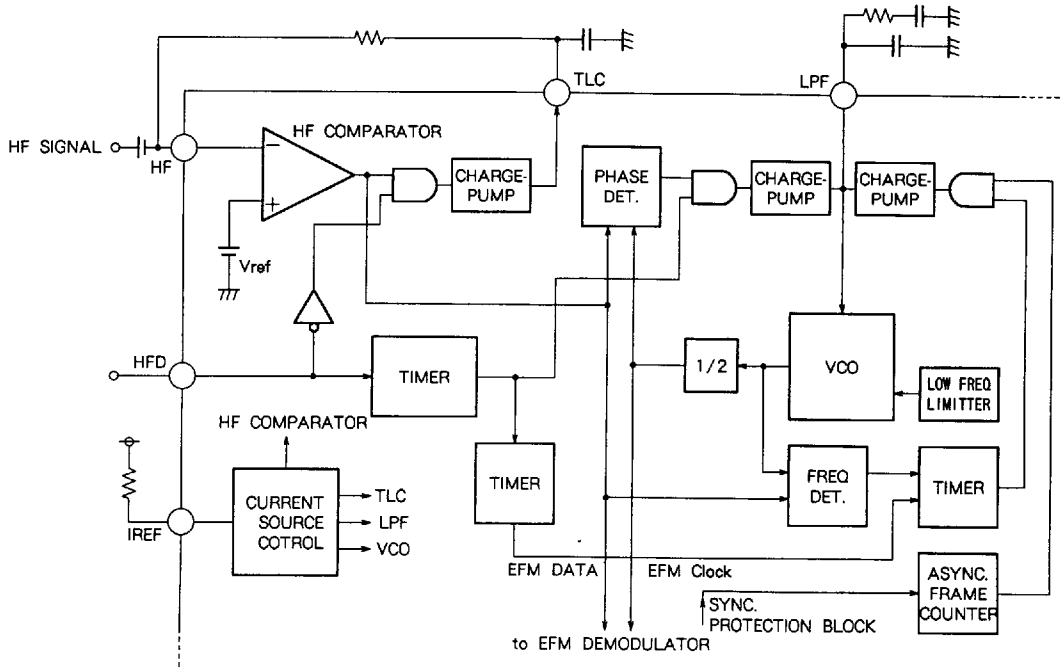
1. Data slicing/PLL

The M50427FP has an analog front-end for incoming EFM (HF) signal. Using CMOS-Analog technology, the front-end comprises an automatic slice level control circuit and EFM-PLL circuit with internal adjust-free VCO. The HF signal is sliced by the HF comparator and a DC level is feed back from TLC to HF through the external CR. If HFD goes High because of a defect an disc, then TLC froms off and holds the DC level. The block-diagram shows the analog front-end.

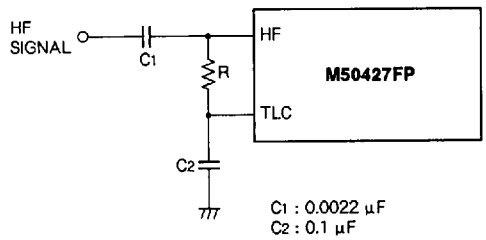
EFM-PLL extracts the EFM clock signal from the HF signal. The PLL circuit has a phase/frequency comparator providing the M50427FP with a wide capture/lock range. There is no need to adjust the VCO. LPF is the charge-pump output and same-time control voltage input to the VCO. LPF froms off state if HFD goes high.

IREF is the reference current input used to determine the current of charge pumps of TLC and LPF, operating point of HF comparator and VCO free running frequency. If IREF is connected to a noisy power supply through a resistor, VCO is modulated and the error-rate increases. Therefore, power supply noise at IREF must be held to a minimum.

BLOCK DIAGRAM (Data slicing/PLL)

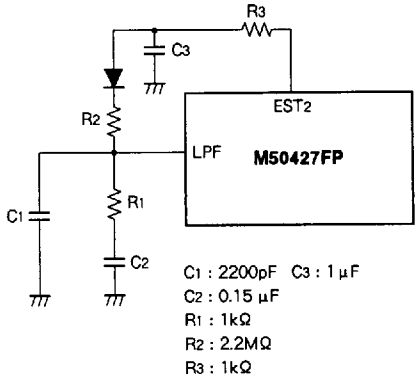


(1) Automatic slice level control



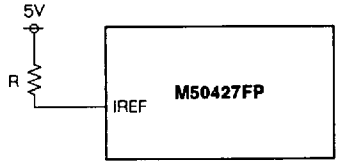
The slice level control circuit is formed by connecting a resistor and capacitors to the HF (High-Frequency signal input) pin and TLC (slice level control output) pin.

(2) PLL



Since the adjustment-free VCO is built in, the adjustment-free PLL circuit can be formed by connecting a resistor and capacitors to the LPG (low-pass filter) pin.

(3) Reference current

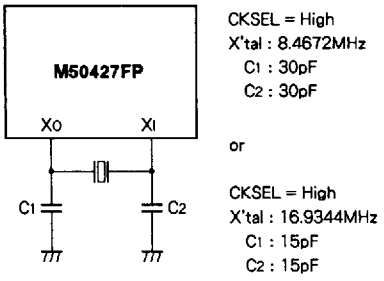


R : 51k Ω

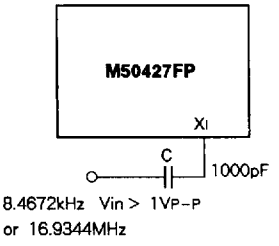
Connect the resistor between the IREF pin and V_{DD} to set the reference current that determines the current values of the TLC pin and LPG pin, the comparator operating current of the slice level control circuit and the VOC free-run frequency.

2. Demodulation/Decoding

(1) Clock generator



(a) The oscillation circuit can be formed by connecting the X'tal osillator (8.4672MHz or 16.9344MHz) and load capacitors to pins X_I and X_O.



b) When the system contains a clock (8.4672MHz or 16.9344MHz), the clock can be input to pin X_I via a capacitor without using the X'tal oscillator.

If the input signal is the logical level, the capacitor is not necessary.

(2) Frame Synchronization

The EFM signal is demodulated by synchronizing the demodulation circuit at frame level. The block diagram shows this frame synchronization control part.

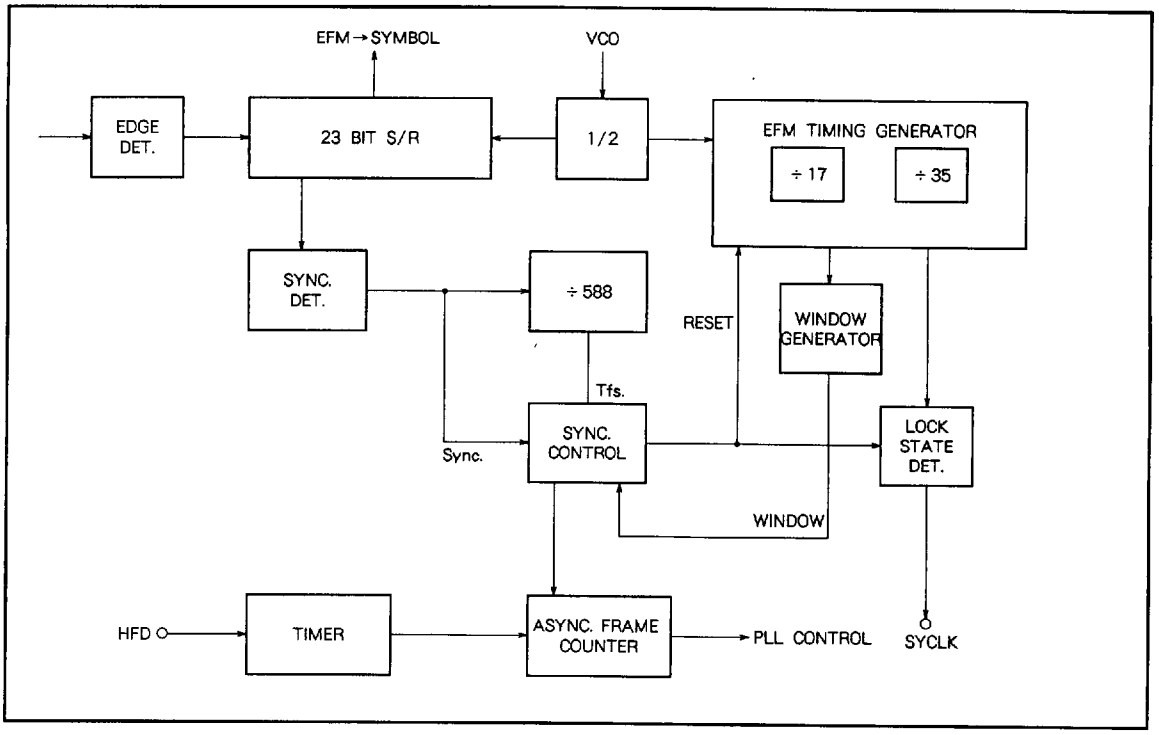


Fig. 1 Frame synchronization block diagram

The generating condition of the counter reset signal (Reset) in the EFM timing generator part is indicated as follows :

Reset = Sync * Tfs + Sync * Window

* : Logical product

\+ : Logical sum

Sync. : Synchronizing signal

Tfs : Detection signal of synchronizing signal space = 588

Window : Window signal ± 7ck

In the synchronous state, Sync and Tfs generate simultaneously and Sync comes to the center of the window. At this time, 1 is output to the SYCLK pin.

(3) Subcode demodulation

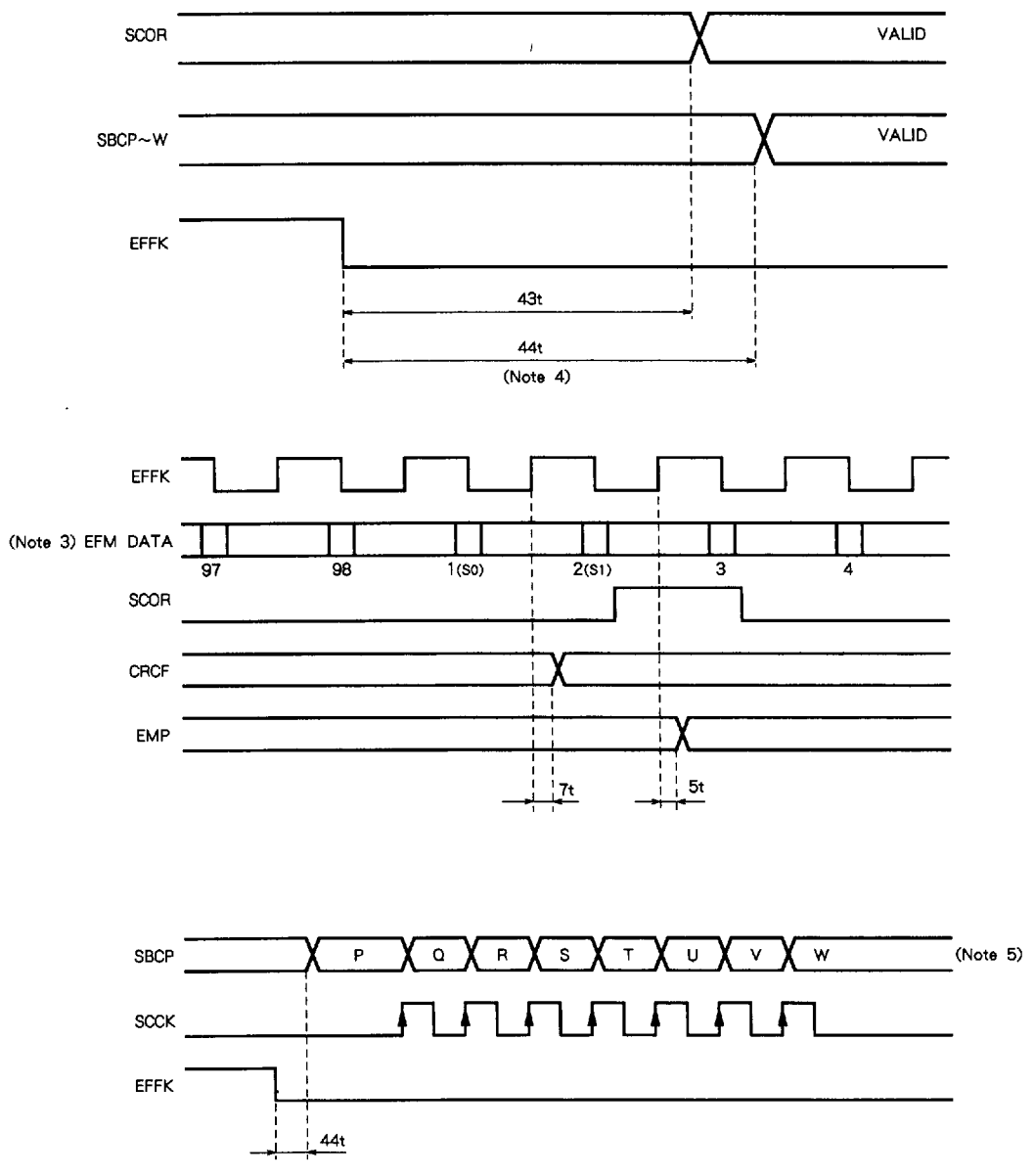
Among data converted from 14-bit EFM signals to 8-bit symbols, subcode P, Q, R, S, T, U, V and W are output to pins SBCP - SPCW respectively. When the subcode synchronizing patterns S0 or S1 are detected as the synchronizing signals of the subcode data, the synchronizing signal are output to the SCOR pin. The pins SBCP-SBCW are a Three-State output system and control the output by 4-bit through two external pins $SCOE_1$ and $SCOE_2$.

SUBCODE DEMODULATION

$SCOE_1$	$SCOE_2$	SBCP	SBCQ	SBCR	SBCS	SBCT	SBCU	SBCV	SBCW
0	0	High-impedance				High-impedance			
1	0	P	Q	R	S	High-impedance			
0	1	High-impedance				T	U	V	W
1	1	P	Q	R	S	T	U	V	W

A CRC check is made for the Q channel data and if the data is correct, 1 is output to the CRCF pin. Whether or not there is emphasis is output to the EMP pin. The subcode data is not only output in parallel but also can be obtained serialy via pin SBCP by inputting a clock to pin SCCK.

Fig. 2 shows the timing of each signal.



Notes 3. Subcode block No. in the EFM data

4. t : Oscillating frequency (VCO)

(Average : 1/8.6436MHz = 115.7ns.)

5. When input to SCCK is more than 8ck, SBCP becomes 0.

Fig. 2 Subcode output timing

(4) RAM interface/CIRC decoding

A 64K/256K dynamic RAM is used as the external memory for temporary storage process CIRC decoding (C1 decoding, C2 decoding, unscramble and de-interleave) and output interpotion.

By using a 64K/256K RAM, jitter is absorbed up to ±8 frames (max.).

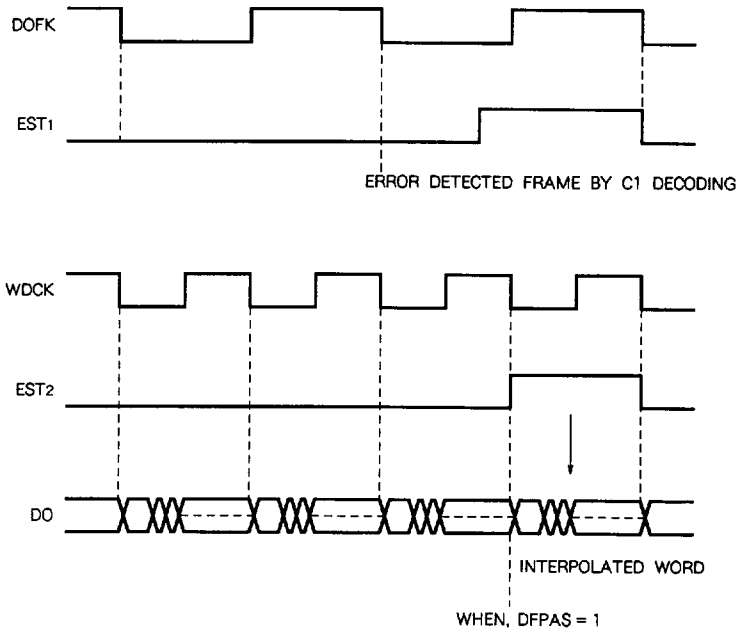
Fig. 3 shows the timing for reading from and writing to the RAM.

In CIRC decoding, double error correction is done for both C1 and C2 decoding. When correction is not possible, average interpolation or pre-hold interpolation is performed. Error states which are detected during, decoding are output to pins EST_1 and EST_2.

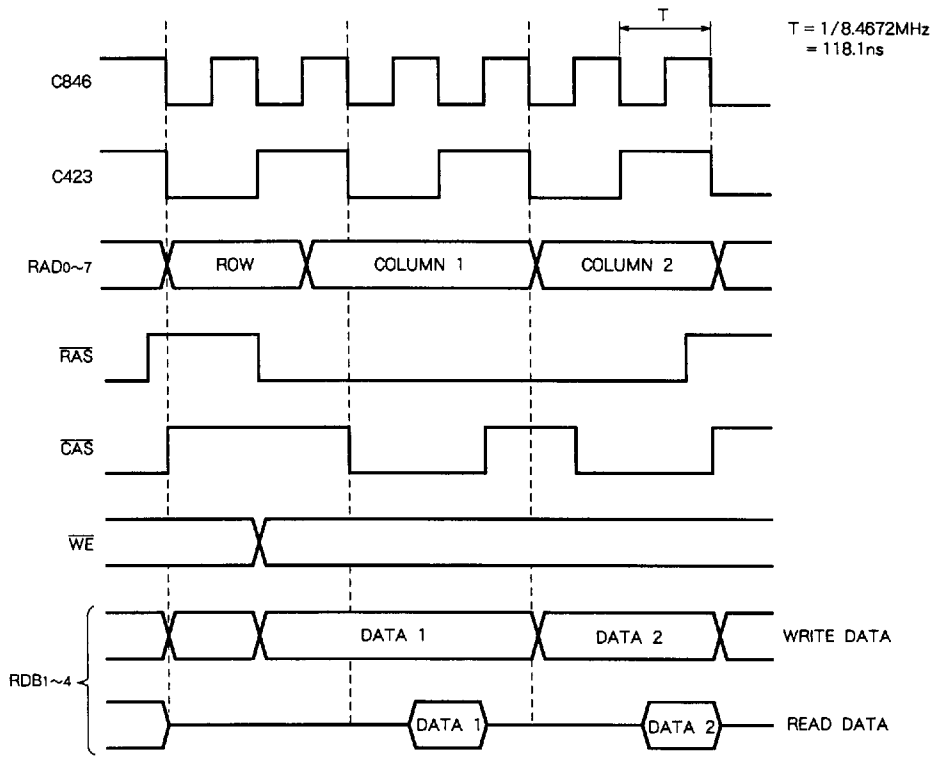
When an error is detected by C1 decoding, 1 is output to pin EST_1. When an error word is judged un-correctable by C2 decoding, 1 is output to pins EST_2.

The output timings for pins EST_1 and EST_2 are as follows:

Timing chart



(a) Symbol data/flag, read/write timing



(b) C1/C2 flag, read/write timing

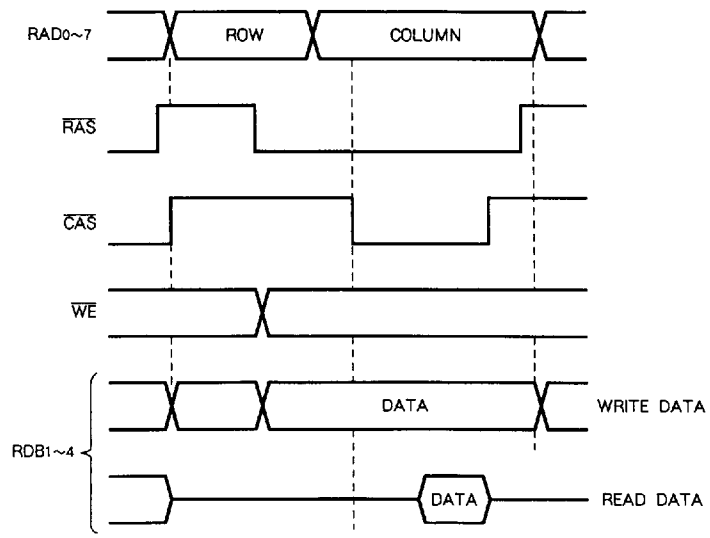
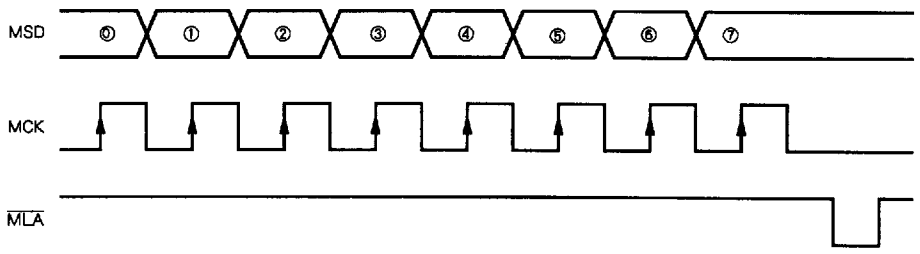


Fig. 3 RAM interface timing

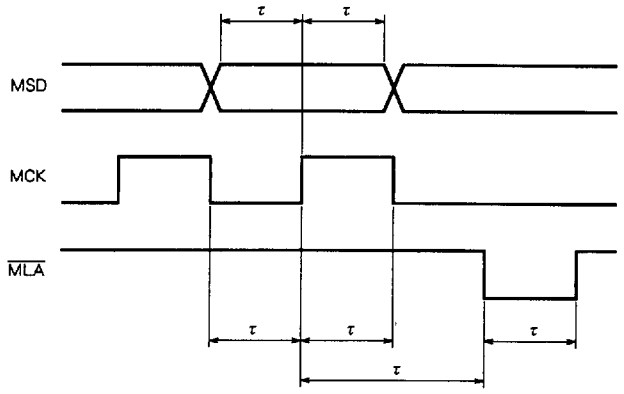
3. Microcomputer Interface

CLV servo, MUTE and ATT system control is done by serial command from the microcomputer. The timing, and names and functions of each control register are as follows :

Timing chart



⓪ DUMMY (Don't care)	X
① S/S(START/STOP) register.	start = 1
② BCON(BRAKECONTROL) register.	enable = 1
③ BRAK(BRAKE) register.	brake = 1
④ ATT(ATTENUATE) register.	−12dB = 1
⑤ $\overline{\text{MUTE}}$ register.	mute = 0
⑥ S/S timer reset register.	reset = 1
⑦ IC code.	M50427FP = 1



τ min ∗ 500ns

Function of interface resisters

Register No.	Register name	Function	Operation		Note
			0	1	
⓪	DUMMY	Don't care	–	–	
①	S/S (START/STOP)	Controls START/STOP of the disk motor	DISC MOTOR STOP (OFF)	DISC MOTOR START (ON)	0 by $\overline{ACLR}$
②	BCON (BRAKECONTROL)	Determines if BRAKE control is necessary	BRAKE 0.3sec.	BRAKE is controlled by BRAK register	0 by $\overline{ACLR}$
③	BRAK (BRAKE)	Controls BRAKE	BRAKE OFF (MOTOR OFF)	BRAKE ON	When BCON = 1
④	ATT (ATTENUATE)	Sets attenuation (−12dB)	0dB	−12dB	When MUTE = 1
⑤	MUTE	Sets the muting	−∞dB	0dB	0 by $\overline{ACLR}$
⑥	S/S timer reset	Resets the S/S timer which sets the time of KICK and BRAKE to 0.3sec	S/S timer enable	S/S timer disable	1 by $\overline{ACLR}$
⑦	IC code	Distinguishes the command to the M50427FP	–	Executing command	0 is code for servo IC

Examples of system control are as follows :

Operation \ Register name	⓪ DUMMY	① S/S	② BCON	③ BRAK	④ ATT	⑤ $\overline{MUTE}$	⑥ S/S timer reset	⑦ IC code
								0
MUTE						0		1
ATT					1	1		1
0.3sec.KICK→CLV		1					0	1
0.3sec.BRAKE→MOTOR OFF		0	0				0	1
BRAKE		0	1	1			0	1
MOTOR OFF		0	1	0			0	1
0.3sec. timer disable							1	1
MOTOR off (without 0.3sec. BRAKE)		0	0				1	1
CLV (without 0.3sec. KICK)		1	0				1	1
The following is example of the most simplified system control sequence.								
STOP		0	0	0	0	0	1	1
0.3sec. KICK→CLV		1	0	0	0	0	0	1
PLAY		1	0	0	0	1	0	1
FF/FR		1	0	0	1	1	0	1
PLAY		1	0	0	0	1	0	1
0.3sec. BRAKE→STOP		0	0	0	0	0	0	1

* The blanks mean "Don't care" or that other commands can be used simultaneously.

When the M50427FP detects whether the number of rotations is 2/3 that of the normal play state and outputs the disk rotation deterioration signal to the DRD pin.

The rotation of the disk can be correctly stopped by means of the following stop sequence.

Operation or μ-COM Operation \ Register name	⓪ DUMMY	① S/S	② BCON	③ BRAK	④ ATT	⑤ $\overline{MUTE}$	⑥ S/S timer reset	⑦ IC code
PLAY		1	0	0	0	1	0	1
BRAKE		0	1	1	0	0	0	1
($\overline{HFD}$: H checking by microcomputer)								
(Measuring t_{DRD} (DRD : 0→1) after BRAKE start								
(Stop $\overline{HFD}$ checking and) additional BRAKE time 2 × t_{DRD}								
MOTOR OFF		0	1	0	0	0	0	1

To re-initiative the microcomputer interface register, after power supply on, execute $\overline{ACLR}$ (M50427FP clear).

4. Digital filter

The sampling frequency of the data is coverted from 44.1 kHz to 88.2kHz by the digital filter.

The filter is a 27-tap FIR phase linear filter and includes an overflow limitter.

The digital filter can be by-passed by means of the DFPAS pin. At this time, all the D-A interface timing signals are changed according to the sampling frequency (44.1kHz).

Fig. 4 shows the characteristics of the digital filter.

5. Interface to the D-A converter

The interface to the D-A converter is via the MSB first or LSB first serial data and timing signals. Interface mode selection is done by the DASEL1 and DASEL2. The data and the timing signals are as follows :

MODE	DASEL 2	DASEL 1	DO	DSCK	WDCK	LRCK	DWDCK
0	0	0	MSB 1st	DATA SHIFT CLOCK	Word clock	L/R clock	–
1	0	1	LSB 1st	DATA SHIFT CLOCK	Lch sampling clock	Rch sampling clock	–
2	1	0	MSB1st Without interpolation	DATA SHIFT CLOCK	Word clock	L/R clock	–
3	1	1	MSB 1st	DATA SHIFT CLOCK	Lch sampling clock	Rch sampling clock	Word clock

Fig. 5 (a) shows the timing diagram of mode0 and mode2 (without interpolation).

Fig. 5 (b) shows the timing diagram of mode1.

Fig. 5 (c) shows the timing diagram of mode2.

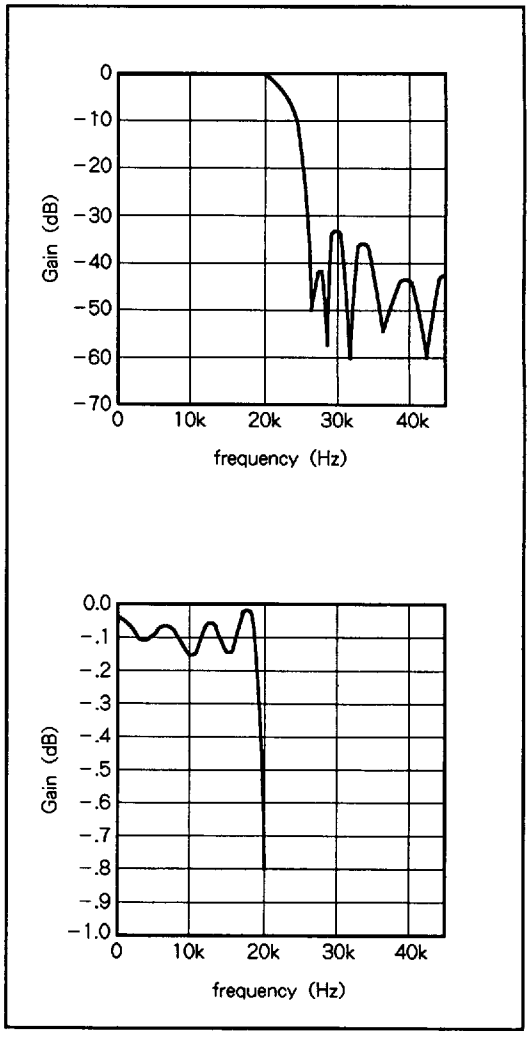
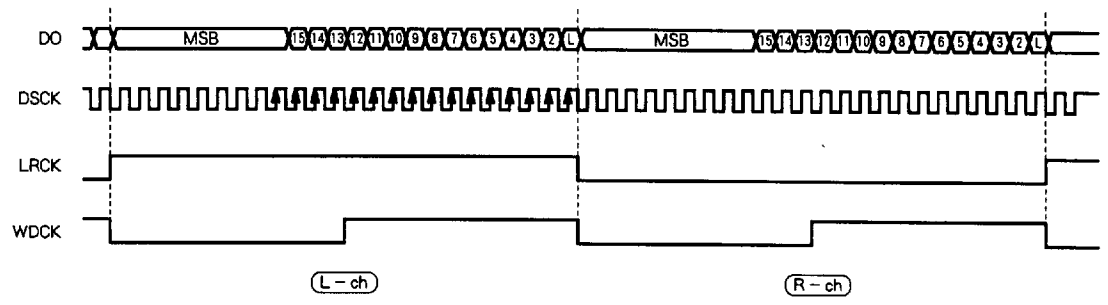


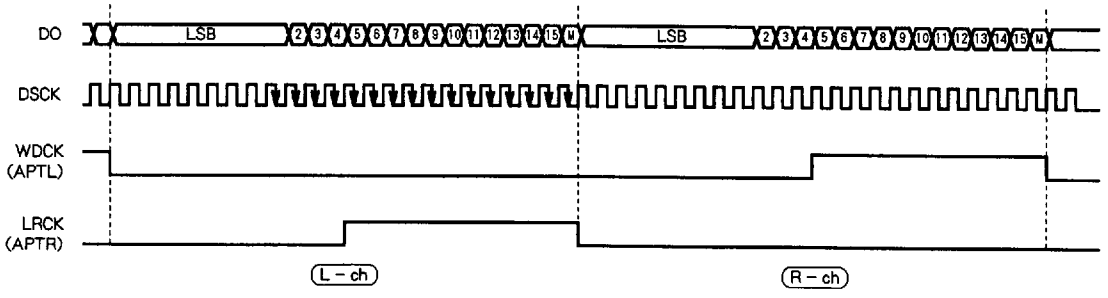
Fig. 4 Frequency characteristics of the digital filter

(a) Mode 0/2



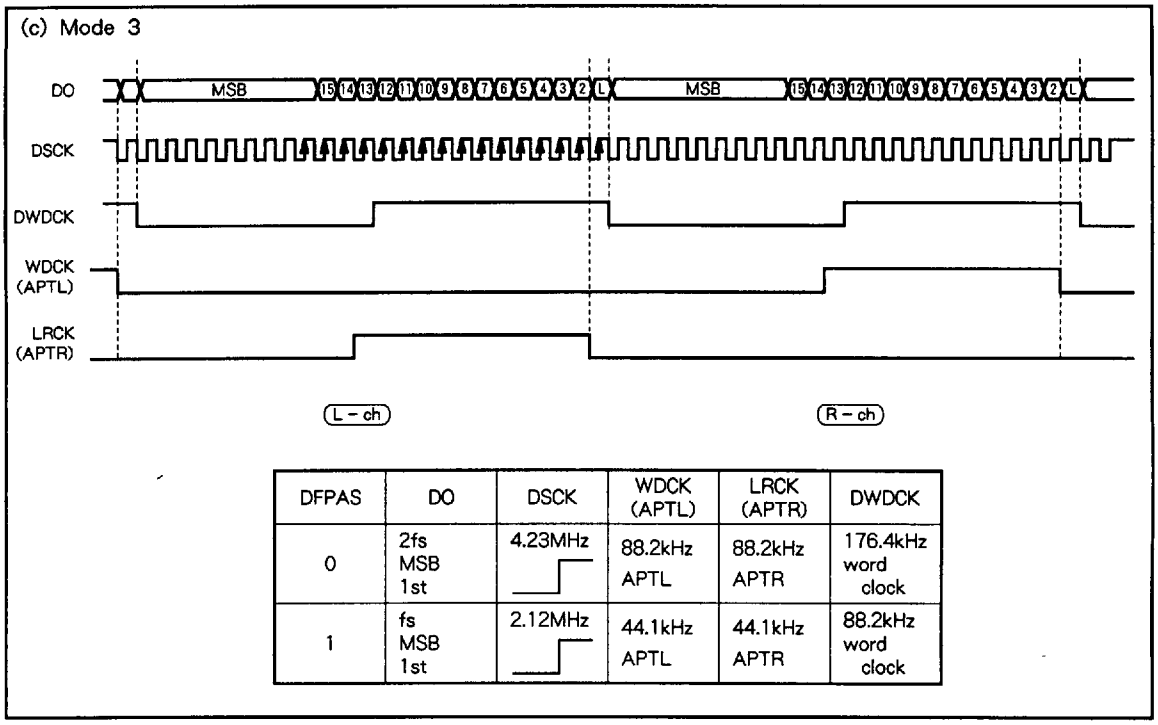
DFPAS	DO	DSCK	WDCK	LRCK
0	2fs MSB 1st	4.23MHz	176.4kHz word clock	88.2kHz L/R clock
1	fs MSB 1st	2.12MHz	88.2kHz word clock	44.1kHz L/R clock

(b) Mode 1



DFPAS	DO	DSCK	WDCK (APTL)	LRCK (APTR)
0	2fs LSB 1st	4.23MHz	88.2kHz APTL	88.2kHz APTR
1	fs LSB 1st	2.12MHz	44.1kHz APTL	44.1kHz APTR

Fig. 5 DAC interface timing

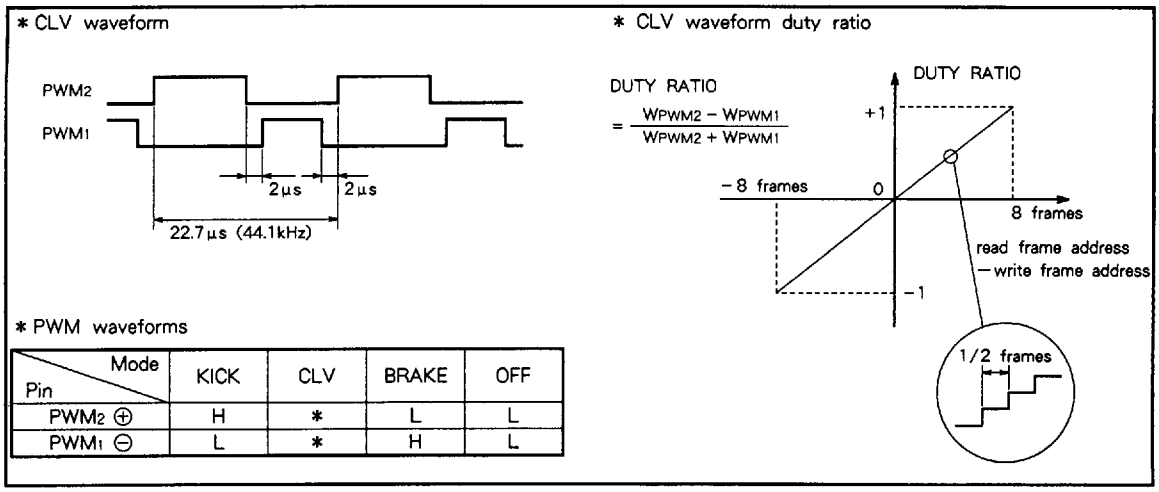


DFPAS	DO	DSCK	WDCK (APTL)	LRCK (APTR)	DWDCK
0	2fs MSB 1st	4.23MHz	88.2kHz APTL	88.2kHz APTR	176.4kHz word clock
1	fs MSB 1st	2.12MHz	44.1kHz APTL	44.1kHz APTR	88.2kHz word clock

Fig. 5 DAC interface timing

6. CLV servo control

CLV servo control circuit operates using two signals. The first is the frequency difference of EFM clock and X'tal clock. The second is the phase difference of write frame address and read frame address of external, 64K/256K RAM. The M50427FP has CLV servo control circuit internal phase compensated.



* PWM waveforms

Pin \ Mode	KICK	CLV	BRAKE	OFF
PWM2 ⊕	H	*	L	L
PWM1 ⊖	L	*	H	L

Fig. 6 CLV waveform