Ordering number: EN※4273

CMOS LSI

SANYO No. ※4273

LC89561

CD-ROM XA Error Correction and ADPCM Decoder LSI with Host CPU

Preliminary

OVERVIEW

The LC89561 is an error correction and ADPCM decoder for CD-ROM XA that features a single data and control bus, making it ideal for small-sized and portable CD-ROM drives where one CPU performs indication control, key control and similar functions from the CD drive.

The LC89561 supports CD-ROM XA using a built-in ADPCM decoder, and data transfer when communicating with a word processor or similar device using a built-in serial interface.

Functional Blocks

Error correction block

- The error correction block corrects errors in CD-ROM output data from the CD player. Data is buffered and stored in external SRAM. Errors are automatically corrected after one-sector buffering (errors are detected and corrected only once).
- The CPU checks that errors have been corrected and then reads data from SRAM.
- Buffering, error correction and data reads are performed in real time using pipeline processing.
- Error-corrected ADPCM data (actually, it is not corrected) is transferred to the audio block under CPU control.
- Buffering and error correction are controlled by the settings of the registers.

ADPCM decoder block

- Error-corrected ADPCM data is transferred to the ADPCM decoder block (audio block) under CPU control. More correctly, the data is read/written from the error correction area of external SRAM to the audio block. The audio block then reads data from the audio block for reproduction.
- Automatic reproduction of levels A, B, C and stereo/monaural is controlled using sub-header information.
- Direct interface connection with LC7883K (8 times over-sampling digital filter + D/A converter). CD-DA output is controlled by the settings of the internal register.

Serial interface block

- The LC89561 has a built-in asynchronous serial interface that is equivalent to the 8251.
- TXRDY and RXRDY interrupt signals are output on ZINT.
- The CPU can write data to the serial interface block one byte at a time, or transfer data automatically by reading the required number of bytes from SRAM, based on the settings of the registers. It is not necessary for the CPU to do anything on the serial interface until a transfer completion interrupt occurs.
- The communications clock pulses, for the serial interface block (TXCLK, RXCLK), can be generated from the clock pulse on XTAL. The division is completed within one XTAL period (divider value is set in the internal register).

DMA controller block

- The LC89561 has a simple built-in DMA controller that transfers data from the external SRAM to system RAM.
- The controller performs dual, burst-mode addressing with a 120 ns RAM access time (360 ns when TWSPD (R2-Bit0) is 0).
- When the CPU transfers data to the LC89561, the LC89561 sets ZBUSRQ LOW and requests release of the bus. The CPU releases the bus and DMA transfer commences after a LOW level is output on ZBUSACK.
- After transfer is completed, the LC89561 releases the bus and sets ZBUSRQ HIGH. At the same time as the CPU outputs a HIGH level on ZBUSACK, the LC89561 generates a completion of decoder transfer interrupt to the CPU.
  The DMA controller can also transfer data inside external SRAM. For example, it is possible to transfer data from an error correction area to a user area, and hold data in RAM. (User area refers to areas other than those set aside for error correction and the ADPCM decoder.)

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3.5 V Operation

The LC89561 can also operate at 3.5 V. The operating characteristics are shown in the following table.

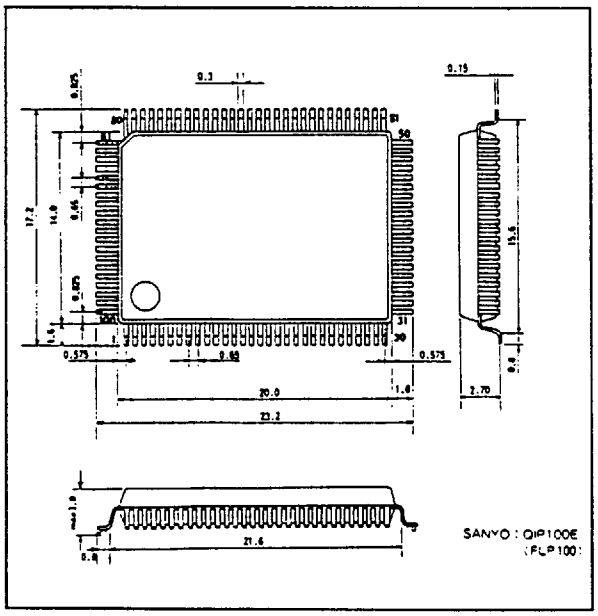
Internal flag (TWSPD)	SRAM address access time	DMA controller transfer speed	Comments
0	360	0.658M byte/s (3.11 ms/sector)	3.5 V operating voltage, Normal-speed
1	180	1.316M byte/s (1.56 ms/sector)	5.0 V operating voltage, Normal- or Double-speed

Note
For 3.5 V operation, the SRAM access time is 360 ns. For standard SRAMs, however, the transfer speed is slower.

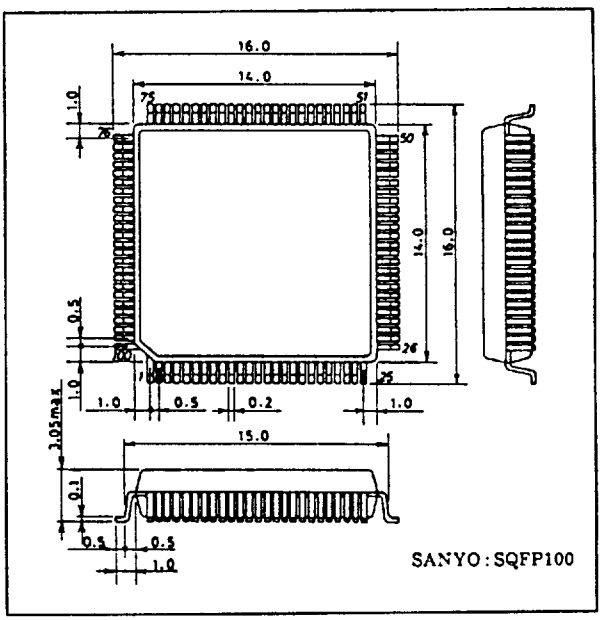
PACKAGE DIMENSIONS

Unit: mm

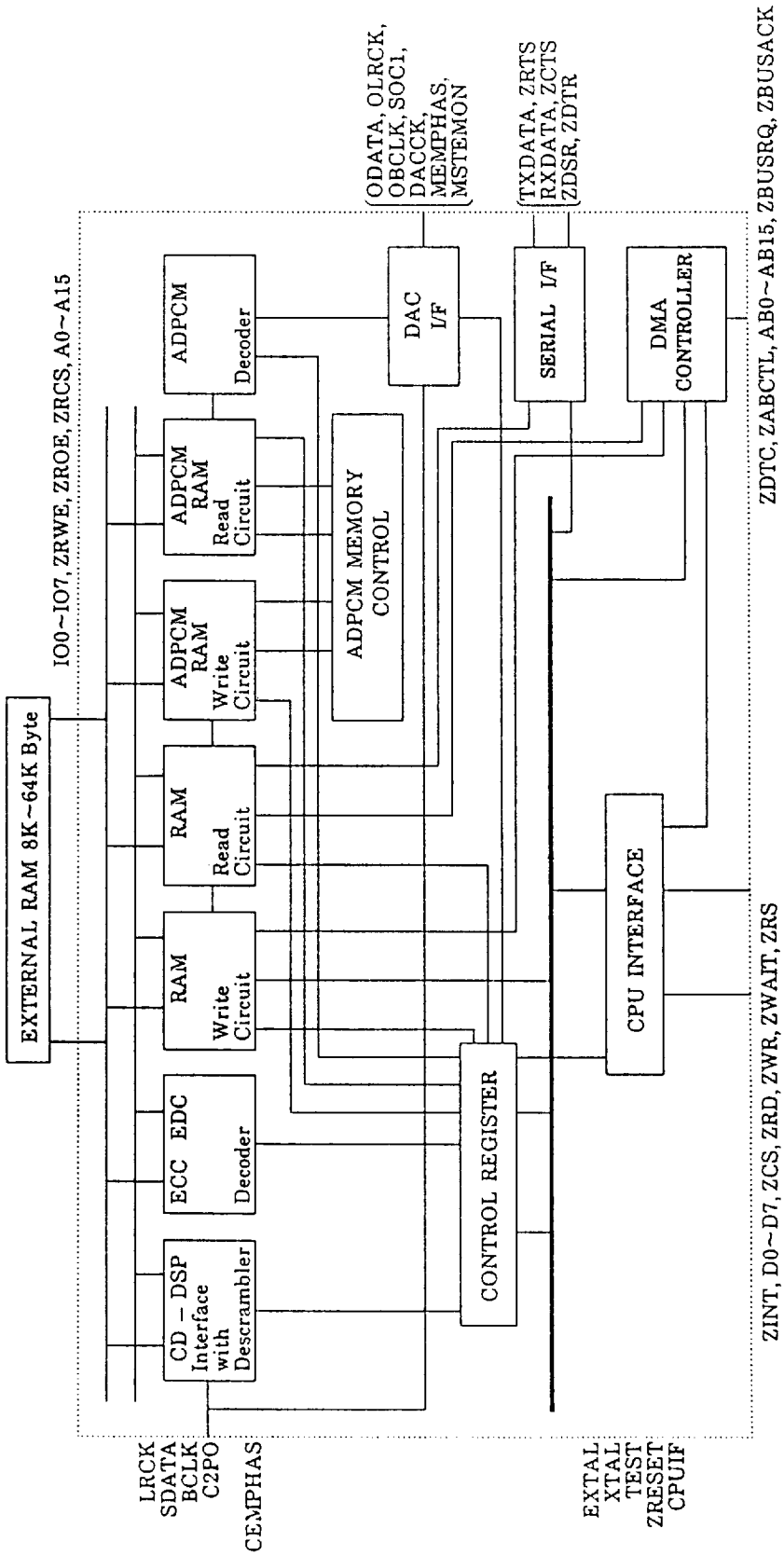
3151-QFP100E



3181-SQFP100



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	I/O	Description
1	TXCLK	I	Serial communications clock input (When generated internally, connect to V_{SS})
2	TXDATA	I	Serial communications input data
3	RXDATA	O	Serial communications output data
4	ZCTS	I	Serial communications control input pin
5	ZRTS	O	Serial communications control output pin
6	ZRESET	I	Reset pin (1 µs LOW-level reset)
7	CPUIF	I	CPU interface set pin
8	V_{SS}	–	Ground pin
9	TEST	O	Test pin. Tie LOW.
10	V_{SS}	–	Ground pin
11	MCK	O	Clock output pin (16.9344 or 8.4672 MHz)
12	V_{DD}	–	Supply pin
13	XTAL	I	Crystal oscillator pins
14	EXTAL	O	
15	V_{SS}	–	Ground pin
16	LRCK	I	CD digital signal processor connection pin
17	SDATA	I	
18	BCK	I	
19	C2PO	I	
20	CEMPHAS	I	
21	DACCK	O	D/A converter clock output
22	SOC1	O	CD-DA/CD-ROMXA distinguish pin
23	OLRCK	O	D/A converter connection pin
24	ODATA	O	
25	OBCLK	O	
26	MEMPHAS	O	Audio block monitor pins
27	MSTEMON	O	
28	ZRCS	O	SRAM chip select pin
29	ZRWE	O	SRAM write pin
30	ZROE	O	SRAM read pin
31	V_{SS}	–	Ground pin
32	IO0	I/O	RAM data input/output pins
33	IO1	I/O	
34	IO2	I/O	
35	IO3	I/O	
36	IO4	I/O	
37	IO5	I/O	
38	IO6	I/O	

Number	Name	I/O	Description
39	IO7	I/O	RAM data input/output pins
40	V_{SS}	-	Ground pin
41	V_{DD}	-	Supply pin
42	RA15	O	RAM address output pins
43	RA14	O	
44	RA13	O	
45	RA12	O	
46	RA11	O	
47	RA10	O	
48	RA9	O	
49	RA8	O	
50	RA7	O	
51	RA6	O	
52	RA5	O	
53	RA4	O	
54	RA3	O	
55	RA2	O	
56	RA1	O	
57	RA0	O	
58	V_{SS}	-	Ground pin
59	V_{DD}	-	Supply pin
60	ABCTL	O	Address bus control pin
61	AB15	O	Address bus connection pins with tristate outputs
62	AB14	O	
63	AB13	O	
64	AB12	O	
65	AB11	O	
66	AB10	O	
67	AB9	O	
68	AB8	O	
69	AB7	O	
70	AB6	O	
71	AB5	O	
72	AB4	I/O	Address bus connection pins and bus pins (direct addressing input only)
73	AB3	I/O	
74	AB2	I/O	
75	AB1	I/O	
76	AB0	I/O	
77	V_{SS}	-	Ground pin

Number	Name	I/O	Description
78	V_{DD}	–	Supply pin
79	RS	I	Register select pin
80	ZCS	I	CPU interface chip select pin
81	ZRD	I	CPU interface read pin
82	ZWR	I	CPU interface write pin
83	ZWAIT	O	CPU interface wait output pin
84	ZINT	O	CPU interface interrupt pin with open-drain output
85	ZBUSRQ	O	DMA bus release request with open-drain output
86	ZBUSACK	I	Bus release acknowledge input from CPU
87	D0	I/O	CPU interface data bus input/output pins
88	D1	I/O	
89	V_{DD}	–	Supply pin
90	V_{SS}	–	Ground pin
91	D2	I/O	CPU interface data bus input/output pins
92	D3	I/O	
93	D4	I/O	
94	D5	I/O	
95	D6	I/O	
96	D7	I/O	
97	ZDTC	I	DMAC data transfer stop input. Connect to V_{DD} if not used.
98	V_{SS}	–	Ground pin
99	ZDSR	I	Serial communications control input pin
100	ZDTR	O	Serial communications control output pin

SPECIFICATIONS

Absolute Maximum Ratings

V_{SS} = 0 V

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage range	V_{DD}	T_a = 25 °C	–0.3 to + 7.0	V
Input and output voltage range	V_I, V_O	T_a = 25 °C	–0.3 to V_{DD} +0.3	V
Power dissipation	P_D	$T_a \leq$ 70 °C	350	mW
Operating temperature range	T_{opg}		–30 to 70	°C
Storage temperature range	T_{stg}		–55 to 125	°C
Soldering temperature	T_{sol}	10 s	260	°C

Recommend Operating Conditions

T_a = −30 to 70 °C, V_{SS} = 0 V

Parameter	Symbol	Rating			Unit
		min	typ	max	
Supply voltage	V_{DD}	3.5	5.0	5.5	V
Input voltage range	V_{IN}	0	–	V_{DD}	V

Electrical Characteristics

V_{SS} = 0 V, V_{DD} = 3.5 to 5.5 V, T_a = −30 to 70 °C

Parameter	Symbol	Conditions	Rating			Unit
			min	typ	max	
HIGH-level input voltage	V_{IH1}	All input pins except XTALCK and those in note 1.	2.2	–	–	V
LOW-level input voltage	V_{IL1}	All input pins except XTALCK and those in note 1.	–	–	0.8	V
HIGH-level input voltage	V_{IH2}	See note 1.	2.5	–	–	V
LOW-level input voltage	V_{IL2}	See note 1.	–	–	0.6	V
HIGH-level output voltage	V_{OH1}	I_{OH1} = −3 mA, all output pins except XTAL, bus pins and those in note 2.	2.4	–	–	V
LOW-level output voltage	V_{OL1}	I_{OL1} = 3 mA, all output pins except XTAL, bus pins and those in note 2.	–	–	0.4	V
LOW-level output voltage	V_{OL2}	I_{OL2} = 3 mA. See note 2.	–	–	0.4	V
Input leakage current	I_L	V_I = V_{SS}, V_{DD}. All input pins.	−25	–	25	μA
Pull-up resistance	R_{UP}	IO0 to IO7	10	20	40	kΩ

Notes

1. Pins TRXCLK, RXDATA, ZCTS, ZRESET, RS, ZCS, ZRD, ZWR, ZBUSACK, ZDTC, ZDSR and IO0 to IO7
2. Pins ZINT and ZBUSRQ (connect pull-up resistors if used)

Recommended Oscillator Circuit