PRELIMINARY

Integrated Circuit Systems, Inc.

ICS83904-02

LOW SKEW, 1-TO-4 CRYSTAL-TO-LVCMOS/LVTTL FANOUT BUFFER

GENERAL DESCRIPTION

The ICS83904-02 is a low skew, high performance 1-to-4 Crystal Oscillator/Crystal-to-LVCMOS Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS83904-02 has selectable single ended clock or two crystal-oscillator inputs. There is an output enable to disable the outputs by placing them into a high-impedance state.

Guaranteed output and part-to-part skew characteristics make the ICS83904-02 ideal for those applications demanding well defined performance and repeatability.

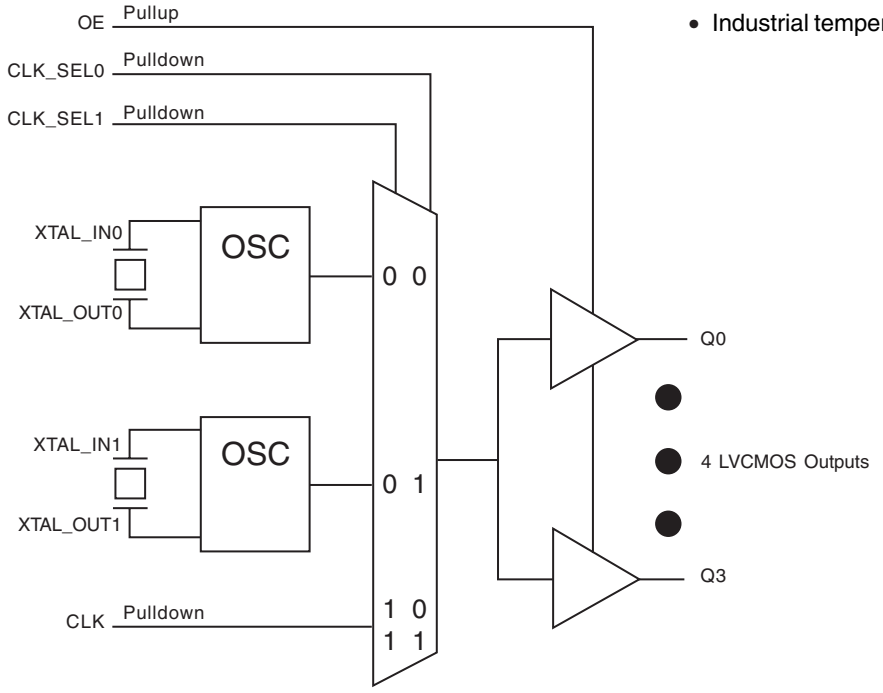
FEATURES

- Four LVCMOS/LVTTL outputs, 19Ω typical output impedance
- Two Crystal oscillator input pairs
  One LVCMOS/LVTTL clock input
- Crystal input frequencry range: 10MHz - 40MHz
- Output frequency: 200MHz (typical)
- Output Skew: TBD
- Part to Part Skew: TBD
- RMS phase jitter @ 25MHz output, using a 25MHz crystal (100Hz - 1MHz): 0.16ps (typical) @ $V_{DD} = V_{DDO} = 3.3V$
- RMS phase noise at 25MHz:

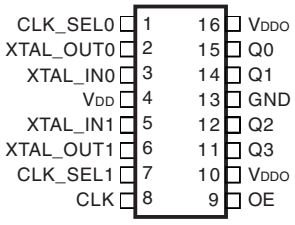
Offset	Noise Power
100Hz	-118.4 dBc/Hz
1kHz	-141.5 dBc/Hz
10kHz	-157.2 dBc/Hz
100kHz	-157.2 dBc/Hz

- Supply Voltage Modes:
  (Core/Output)
  3.3V/3.3V
  3.3V/2.5V
  3.3V/1.8V
  2.5V/2.5V
  2.5V/1.8V
- 0°C to 70°C ambient operating temperature
- Industrial temperature available upon request

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS83904-02
16-Lead TSSOP
4.4mm x 5.0mm x 0.92mm
package body
G Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 7	CLK_SEL0, CLK_SEL1	Input	Pulldown	Clock select inputs. See Table 3, Input Reference Function Table. LVCMOS / LVTTL interface levels.
2, 3	XTAL_OUT0, XTAL_IN0	Input		Crystal oscillator interface. XTAL_IN0 is the input. XTAL_OUT0 is the output.
4	V_{DD}	Power		Core supply pin.
5, 6	XTAL_IN1, XTAL_OUT1	Input		Crystal oscillator interface. XTAL_IN1 is the input. XTAL_OUT1 is the output.
8	CLK	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTL interface levels.
9	OE	Input	Pullup	Output enable. When LOW, outputs are in HIGH impedance state. When HIGH, outputs are active. LVCMOS / LVTTL interface levels.
10, 16	V_{DDO}	Power		Output supply pins.
11, 12, 14, 15	Q3, Q2, Q1, Q0	Output		Single-ended clock outputs. LVCMOS/LVTTL interface levels.
13	GND	Power		Power supply ground.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
C_{PD}	Power Dissipation Capacitance (per output)	V_{DDO} = 3.465V		8		pF
		V_{DDO} = 2.625V		7		pF
		V_{DDO} = 2.0V		7		pF
R_{OUT}	Output Impedance	V_{DDO} = 3.3V ± 5%		19		Ω
		V_{DDO} = 2.5V ± 5%		TBD		Ω
		V_{DDO} = 1.8V ± 0.2V		TBD		Ω

TABLE 3. INPUT REFERENCE FUNCTION TABLE

Control Inputs		Reference
CLK_SEL1	CLK_SEL0	
0	0	XTAL0 (default)
0	1	XTAL1
1	0	CLK
1	1	CLK

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	89°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			28		mA
I_{DDO}	Output Supply Current			50		mA

TABLE 4B. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			28		mA
I_{DDO}	Output Supply Current			33		mA

TABLE 4C. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		1.6	1.8	2.0	V
I_{DD}	Power Supply Current			29		mA
I_{DDO}	Output Supply Current			25		mA

TABLE 4D. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			15		mA
I_{DDO}	Output Supply Current			41		mA

TABLE 4E. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = 2.5V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		1.6	1.8	2.0	V
I_{DD}	Power Supply Current			15		mA
I_{DDO}	Output Supply Current			32		mA

TABLE 4F. LVCMOS/LVTTL DC CHARACTERISTICS, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V ± 5%	2.0		V_{DD} + 0.3	V
			V_{DD} = 2.5V ± 5%	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V ± 5%	-0.3		0.8	V
			V_{DD} = 2.5V ± 5%	-0.3		0.7	V
I_{IH}	Input High Current	CLK, CLK_SEL0:1	V_{DD} = 3.3V or 2.5V ± 5%			150	µA
		OE	V_{DD} = 3.3V or 2.5V ± 5%			5	µA
I_{IL}	Input Low Current	CLK, CLK_SEL0:1	V_{DD} = 3.3V or 2.5V ± 5%	-5			µA
		OE	V_{DD} = 3.3V or 2.5V ± 5%	-150			µA
V_{OH}	Output HighVoltage		V_{DDO} = 3.3V ± 5%; NOTE 1	2.6			V
			V_{DDO} = 2.5V ± 5%; NOTE 1	1.8			V
			V_{DDO} = 1.8V ± 0.2V; NOTE 1	1.5			V
V_{OL}	Output Low Voltage		V_{DDO} = 3.3V ± 5%; NOTE 1			0.5	V
			V_{DDO} = 2.5V ± 5%; NOTE 1			0.5	V
			V_{DDO} = 1.8V ± 0.2V; NOTE 1			0.4	V

NOTE 1: Outputs terminated with 50Ω to V_{DDO}/2. See Parameter Measurement section, "Load Test Circuit" diagrams.

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation / cut		Fundamental			
Frequency		10		40	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

TABLE 6A. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	w/External XTAL		10		40	MHz
		w/External CLK			200		MHz
tp_{LH}	Propagation Delay, Low-to-High; NOTE 1				1.8		ns
*t*sk(o)	Output Skew; NOTE 2				TBD		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3				TBD		ps
*t*jit(Ø)	RMS Phase Jitter, Random; NOTE 2, 4		25MHz, Integration Range: 100Hz - 1MHz		0.16		ps
t_R / t_F	Output Rise/Fall Time		20% to 80%		420		ps
odc	Output Duty Cycle				50		%
t_{EN}	Output Enable Time; NOTE 5					10	ns
t_{DIS}	Output Disable Time; NOTE 5					8	ns

NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDO}/2$.
NOTE 4: Phase jitter is dependent on the input source used.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.

TABLE 6B. AC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	w/External XTAL		10		40	MHz
		w/External CLK			200		MHz
tp_{LH}	Propagation Delay, Low-to-High; NOTE 1				2		ns
*t*sk(o)	Output Skew; NOTE 2				TBD		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3				TBD		ps
*t*jit(Ø)	RMS Phase Jitter, Random; NOTE 2, 4		25MHz, Integration Range: 100Hz - 1MHz		0.16		ps
t_R / t_F	Output Rise/Fall Time		20% to 80%		440		ps
odc	Output Duty Cycle				50		%
t_{EN}	Output Enable Time; NOTE 5					10	ns
t_{DIS}	Output Disable Time; NOTE 5					8	ns

NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDO}/2$.
NOTE 4: Phase jitter is dependent on the input source used.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.

TABLE 6C. AC CHARACTERISTICS, V_{DD} = 3.3V ± 5%, V_{DDO} = 1.8V±0.2V, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	w/External XTAL		10		40	MHz
		w/External CLK			200		MHz
tp_{LH}	Propagation Delay, Low-to-High; NOTE 1				2.3		ns
*t*sk(o)	Output Skew; NOTE 2				TBD		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3				TBD		ps
*t*jit(Ø)	RMS Phase Jitter, Random; NOTE 2, 4		25MHz, Integration Range: 100Hz - 1MHz		0.16		ps
t_R / t_F	Output Rise/Fall Time		20% to 80%		490		ps
odc	Output Duty Cycle				50		%
t_{EN}	Output Enable Time; NOTE 5					10	ns
t_{DIS}	Output Disable Time; NOTE 5					8	ns

NOTE 1: Measured from V_{DD}/2 of the input to V_{DDO}/2 of the output.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at V_{DDO}/2.
NOTE 4: Phase jitter is dependent on the input source used.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.

TABLE 6D. AC CHARACTERISTICS, V_{DD} = V_{DDO} = 2.5V ± 5%, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	w/External XTAL		10		40	MHz
		w/External CLK			200		MHz
tp_{LH}	Propagation Delay, Low-to-High; NOTE 1				2.1		ns
*t*sk(o)	Output Skew; NOTE 2				TBD		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3				TBD		ps
*t*jit(Ø)	RMS Phase Jitter, Random; NOTE 2, 4		25MHz, Integration Range: 100Hz - 1MHz		0.20		ps
t_R / t_F	Output Rise/Fall Time		20% to 80%		448		ps
odc	Output Duty Cycle				50		%
t_{EN}	Output Enable Time; NOTE 5					10	ns
t_{DIS}	Output Disable Time; NOTE 5					8	ns

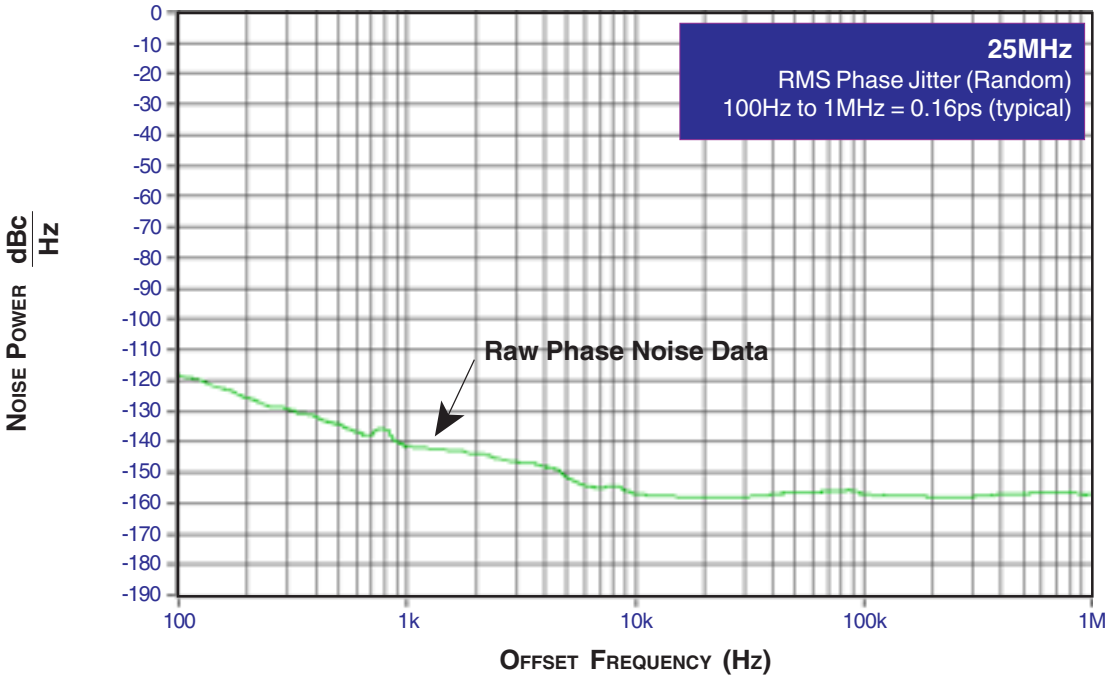
NOTE 1: Measured from V_{DD}/2 of the input to V_{DDO}/2 of the output.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at V_{DDO}/2.
NOTE 4: Phase jitter is dependent on the input source used.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.

TABLE 6E. AC CHARACTERISTICS, V_{DD} = 2.5V ± 5%, V_{DDO} = 1.8V±0.2V, T_A = 0°C TO 70°C

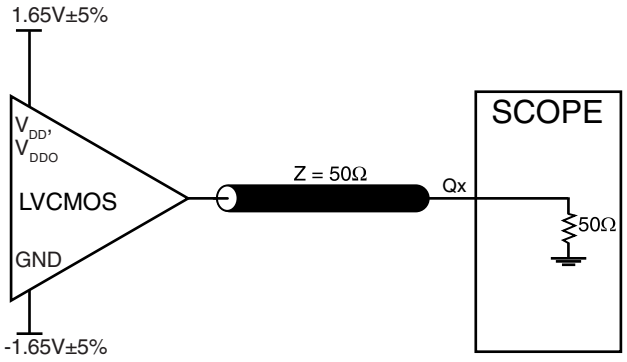
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	w/External XTAL		10		40	MHz
		w/External CLK			200		MHz
tp_{LH}	Propagation Delay, Low-to-High; NOTE 1				2.4		ns
*t*sk(o)	Output Skew; NOTE 2				TBD		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3				TBD		ps
*t*jit(Ø)	RMS Phase Jitter, Random; NOTE 2, 4		25MHz, Integration Range: 100Hz - 1MHz		0.19		ps
t_R / t_F	Output Rise/Fall Time		20% to 80%		490		ps
odc	Output Duty Cycle				50		%
t_{EN}	Output Enable Time; NOTE 5					10	ns
t_{DIS}	Output Disable Time; NOTE 5					8	ns

NOTE 1: Measured from V_{DD}/2 of the input to V_{DDO}/2 of the output.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at V_{DDO}/2.
NOTE 4: Phase jitter is dependent on the input source used.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.

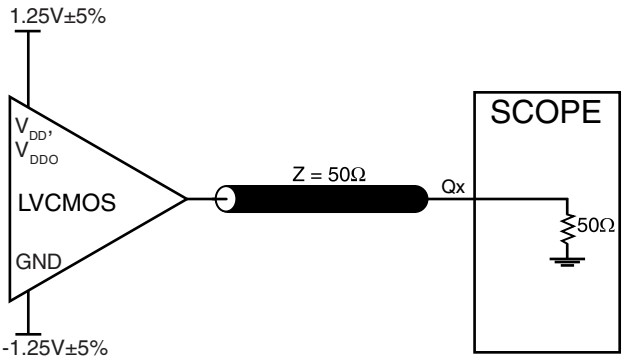
TYPICAL PHASE NOISE AT 25MHZ



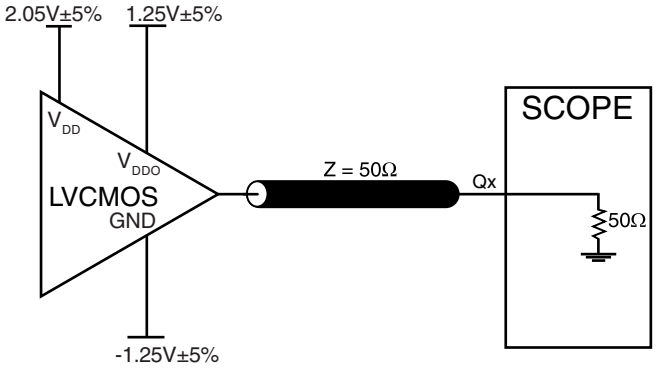
PARAMETER MEASUREMENT INFORMATION



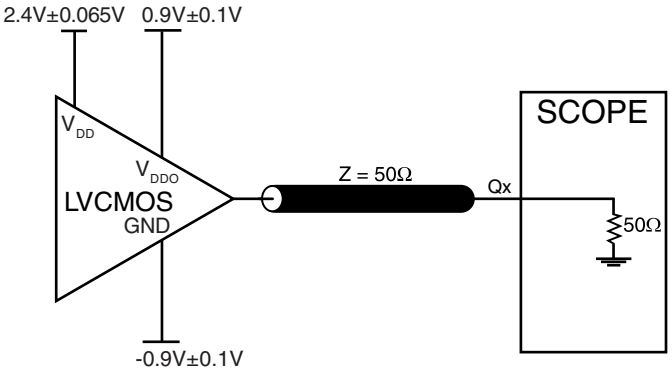
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



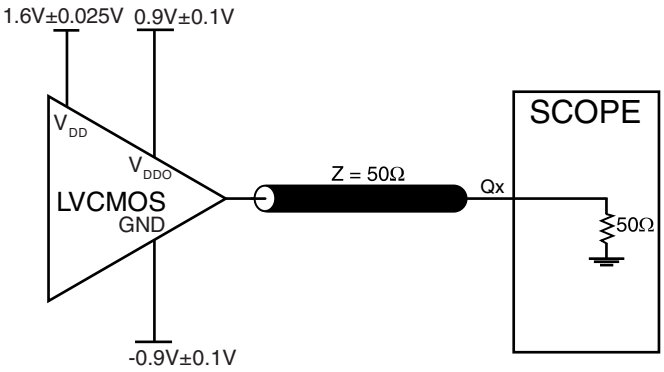
2.5V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



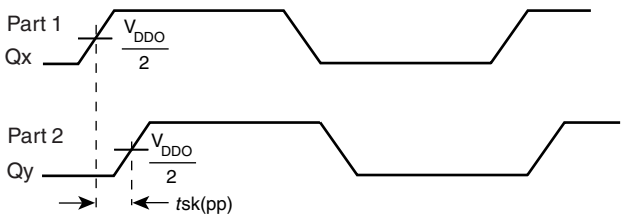
3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



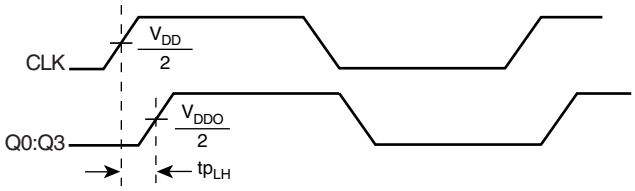
3.3V CORE/1.8V OUTPUT LOAD AC TEST CIRCUIT



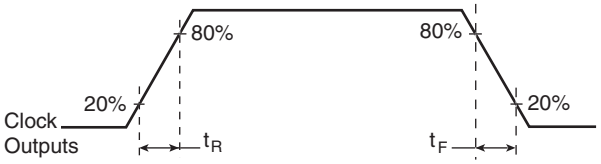
2.5 CORE/1.8V OUTPUT LOAD AC TEST CIRCUIT



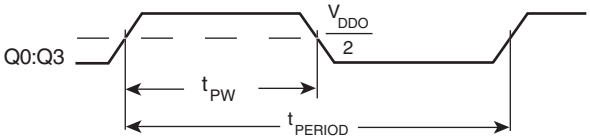
PART-TO-PART SKEW



PROPAGATION DELAY



OUTPUT RISE/FALL TIME



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

CRYSTAL INPUT INTERFACE

A crystal can be characterized for either series or parallel mode operation. The ICS83904-02 has a built-in crystal oscillator circuit. This interface can accept either a series or parallel crystal without additional components and generate frequencies with accuracy suitable for most applications. Additional accuracy can be achieved by adding two small capacitors C1 and C2 as shown in *Figure 1*. Typical results using parallel 18pF crystals are shown in Table 5.

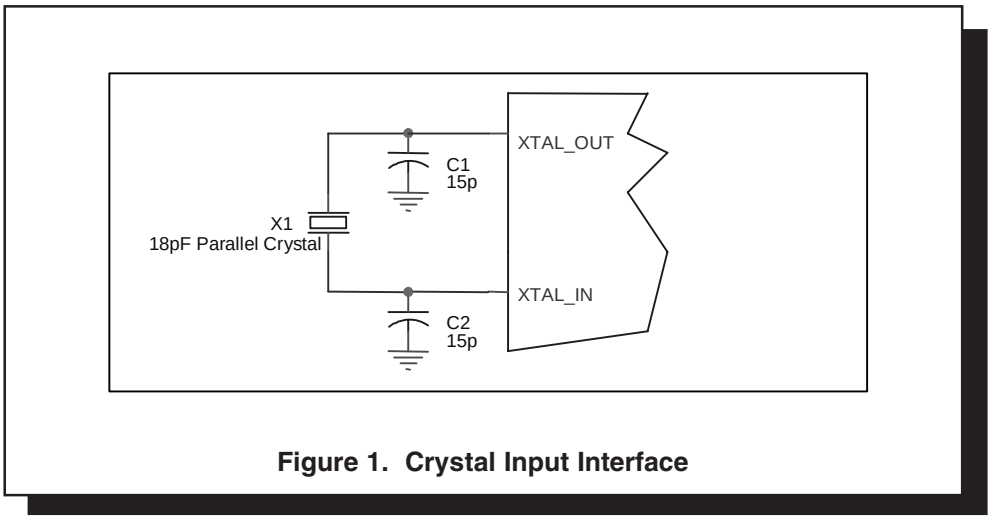


Figure 1. Crystal Input Interface

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CRYSTAL INPUT:
For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resister can be tied from XTAL_IN to ground.

CLK INPUT:
For applications not requiring the use of the test clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resister can be tied from the CLK input to ground.

TEST CLK INPUT:
For applications not requiring the use of the test clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resister can be tied from the TEST_CLK to ground.

CLK/nCLK INPUT:
For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resister can be tied from CLK to ground.

PCLK/nPCLK INPUT:
For applications not requiring the use of a differential input, both the PCLK and nPCLK pins can be left floating. Though not required, but for additional protection, a 1kΩ resister can be tied from PCLK to ground.

SELECT PINS:
All select pins have internal pull-ups and pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resister can be used.

OUTPUTS:

LVCMOS OUTPUT:
All unused LVCMOS output can be left floating. We recommend that there is no trace attached.

LVPECL OUTPUT
All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVHSTL OUTPUT
All unused LVHSTL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVDS OUTPUT
All unused LVDS outputs should be terminated with 100Ω resister between the differential pair.

LVDS – Like OUTPUT
All unused LVDS outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

HCSL OUTPUT
All unused HCSL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

SSTL OUTPUT
All unused SSTL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 16 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	137.1°C/W	118.2°C/W	106.8°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	89.0°C/W	81.8°C/W	78.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS83904-02 is: 205

PACKAGE OUTLINE - G SUFFIX FOR 16 LEAD TSSOP

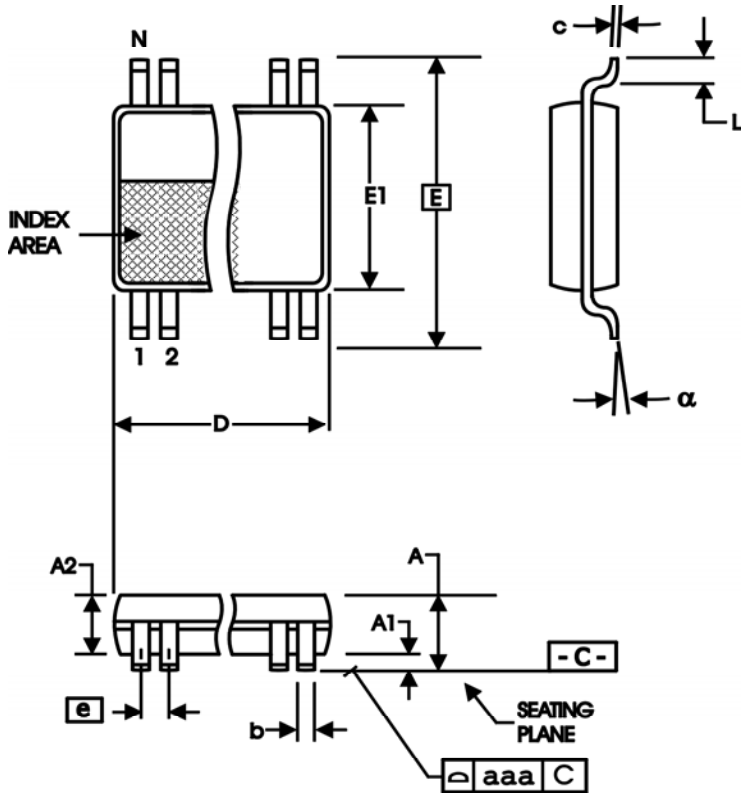


TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	16	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS83904AG-02	83904A02	16 Lead TSSOP	tube	0°C to 70°C
ICS83904AG-02T	83904A02	16 Lead TSSOP	2500 tape & reel	0°C to 70°C