CES7002A

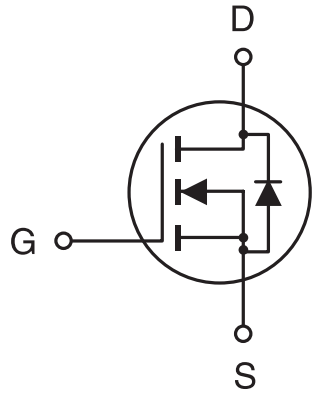
March 1998

N-Channel Enhancement Mode Field Effect Transistor

FEATURES

- 60V , 0.28A , $R_{DS(ON)}$=2Ω @V_{GS}=10V.
  $R_{DS(ON)}$=3Ω @V_{GS}=5V.
- High dense cell design for low $R_{DS(ON)}$.
- Rugged and reliable.
- SOT-23 Package.

SOT-23



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ABSOLUTE MAXIMUM RATINGS (T_A=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous[a] @T_J=125°C	I_D	280	mA
-Pulsed[b]	I_{DM}	1500	mA
Drain-Source Diode Forward Current[a]	I_S	280	mA
Maximum Power Dissipation[a]	P_D	300	mW
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient[a]	$R_{\theta JA}$	417	°C/W

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ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=10μA	60			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V, V_{GS}=0V			1	μA
Gate-Body Leakage	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
ON CHARACTERISTICS[b]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	1	2.1	2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=500mA		1.2	2	Ω
		V_{GS}=5V, I_D=50mA		1.7	3	Ω
On-State Drain Current	$I_{D(ON)}$	V_{DS}=7V, V_{GS}=10V	500			mA
Forward Transconductance	g_{FS}	V_{DS}=7V, I_D=200mA	80	170		mS
DYNAMIC CHARACTERISTICS[c]						
Input Capacitance	C_{ISS}	V_{DS}=25V, V_{GS}=0V f=1.0MHz		38	50	pF
Output Capacitance	C_{OSS}			19	25	pF
Reverse Transfer Capacitance	C_{RSS}			3	5	pF
SWITCHING CHARACTERISTICS[c]						
Turn-On Delay Time	$t_{D(ON)}$	V_{DD}=30V, I_D=200mA, V_{GS}=10V, R_{GEN}=25Ω		23	30	ns
Rise Time	t_r			15	20	ns
Turn-Off Delay Time	$t_{D(OFF)}$			76	100	ns
Fall Time	t_f			15	20	ns

ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS [b]						
Diode Forward Voltage	V_{SD}	V_{GS} = 0V, Is =400mA		0.8	1.2	V

Notes

a.Surface Mounted on FR4 Board, t ≤10sec.

b.Pulse Test:Pulse Width ≤300 μs, Duty Cycle ≤2%.

c.Guaranteed by design, not subject to production testing.

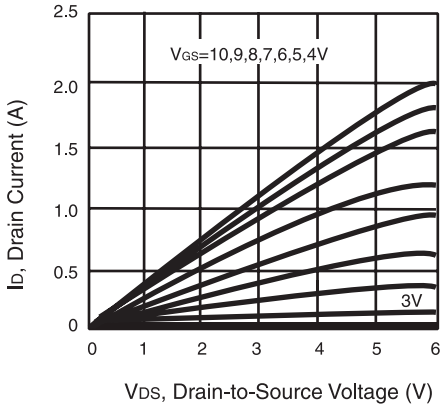


Figure 1. Output Characteristics

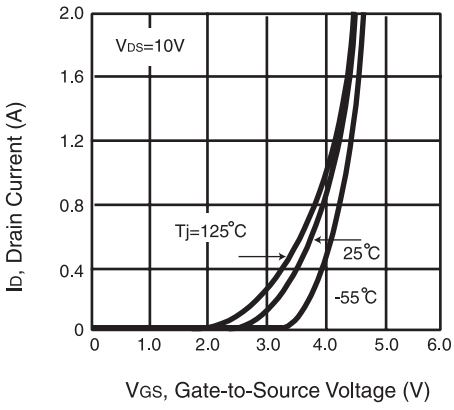


Figure 2. Transfer Characteristics

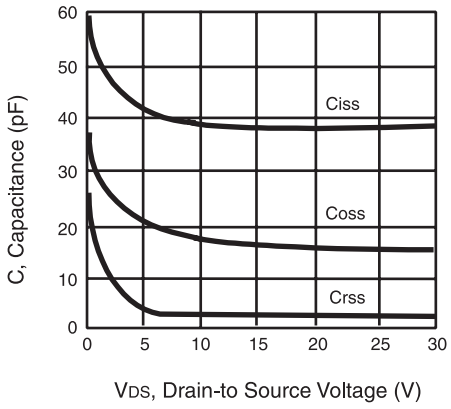


Figure 3. Capacitance

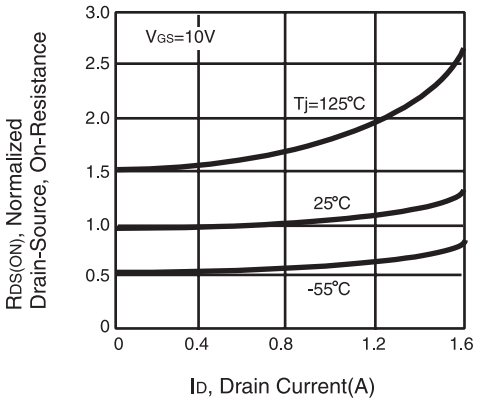


Figure 4. On-Resistance Variation with Drain Current and Temperature

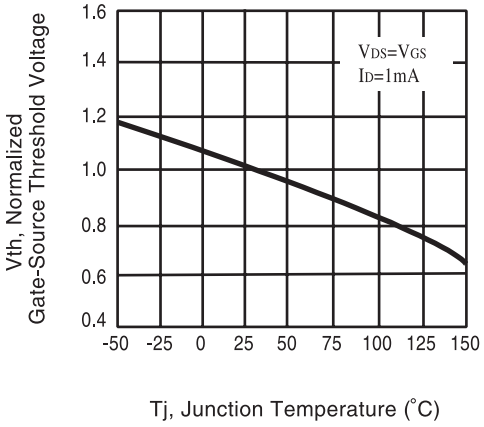


Figure 5. Gate Threshold Variation with Temperature

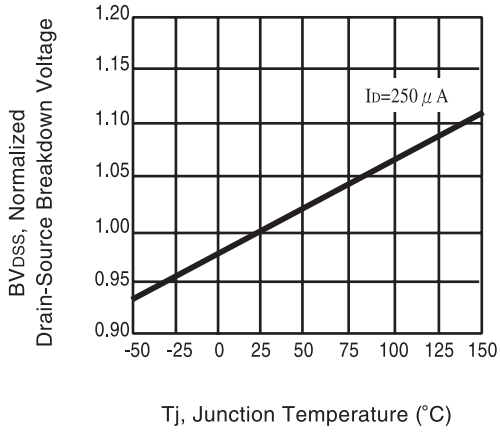
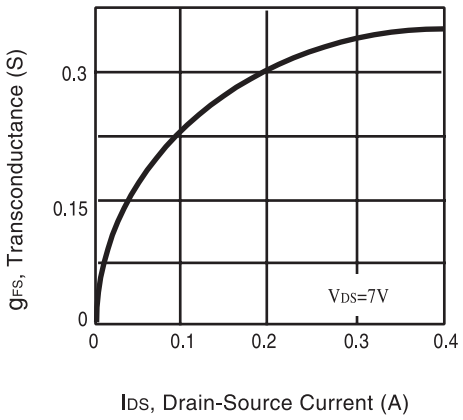


Figure 6. Breakdown Voltage Variation with Temperature



with Drain Current

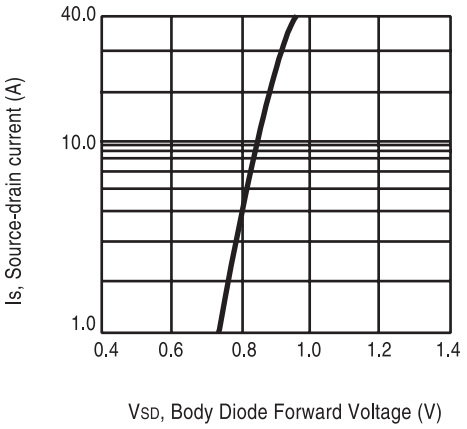


Figure 8. Body Diode Forward Voltage Variation with Source Current

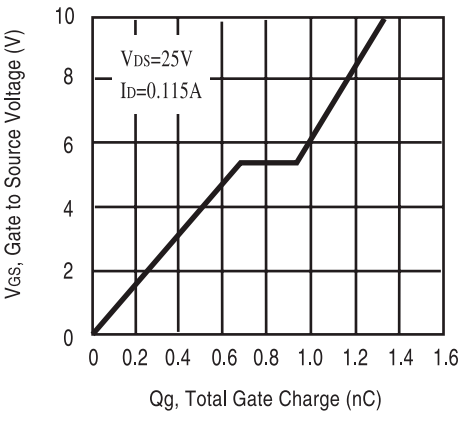


Figure 9. Gate Charge

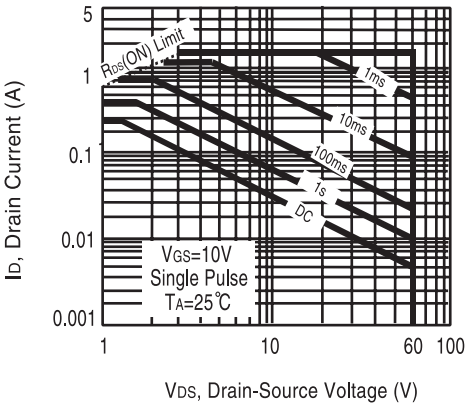


Figure 10. Maximum Safe Operating Area

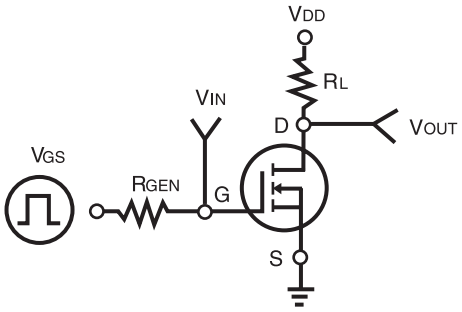


Figure 11. Switching Test Circuit

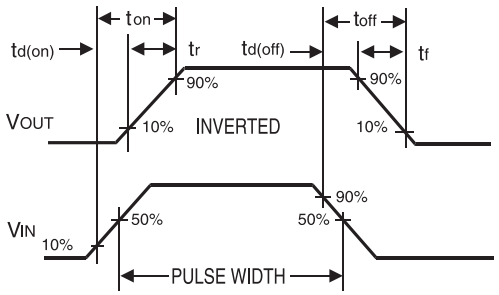


Figure 12. Switching Waveforms

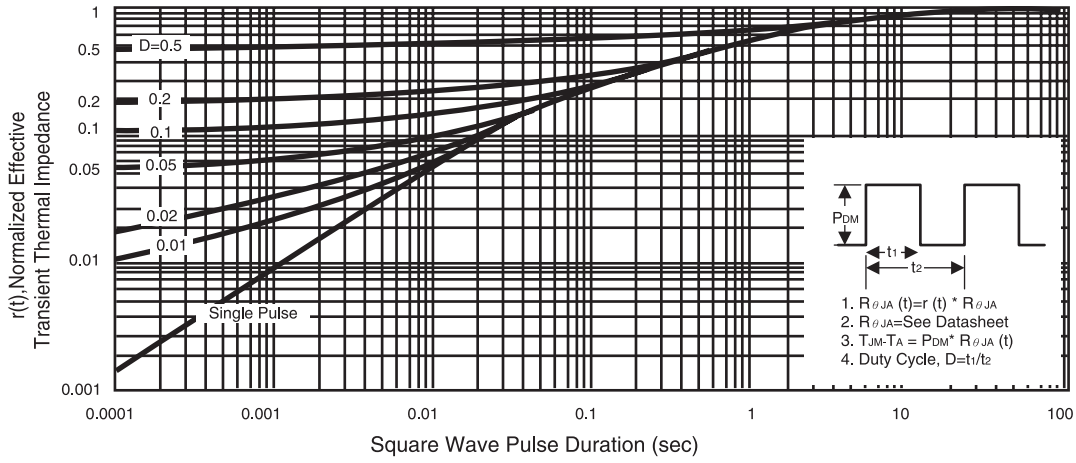


Figure 13. Normalized Thermal Transient Impedance Curve