ARM922T - AMIS Feature Sheet

AMI Semiconductor

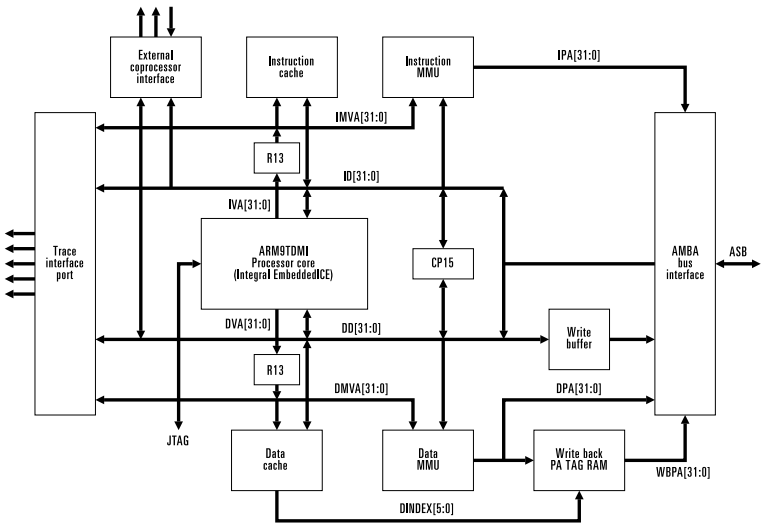
# Embedded RISC Macrocell Core ARM922T

## Key Features


- 32-bit RISC architecture
- Utilizes the ARM9TDMI™ processor core
- Two instruction sets:
  - ARM® high-performance 32-bit instruction set
  - Thumb® high-code-density 16-bit instruction set
- Lowest MIPS/watt power consumption
- High performance – over 200 MIPS
- Harvard architecture
  - 8K data cache
  - 8K instruction cache
  - Caches can be set to “write-through” or “write-back” mode
- Five-stage pipeline consisting of fetch, decode, execute, memory and write stages
- ARM922T™ macrocell includes:
  - Memory management unit
  - Write buffer
  - AMBA™ bus and embedded trace macrocell interfaces
- On-chip JTAG debug and in-circuit emulation
- Extensive range of third-party application development tools

## Product Description

Offering high performance and very low power consumption, the ARM922T embedded macrocell core is in the ARM family of general-purpose 32-bit microprocessors. A unique architectural implementation (Thumb) makes the ARM922T ideal for high-volume applications with memory restrictions or applications where code density is an issue. The ARM architecture is based on reduced instruction set computer (RISC) principles, making it much simpler to use than microprogrammed complex instruction set computer (CISC) devices. This simplicity delivers a higher rate of instruction throughput and an impressive real-time interrupt response time. Pipelined speed-critical control signals allow system control functions to be implemented in standard low-power logic. These control signals facilitate the exploitation of the fast local-access modes in industry-standard dynamic RAMs.




*Functional block diagram of the ARM922T*

### Process support at AMIS

AMI Semiconductor (AMIS) supports the ARM922T embedded macrocell in a 0.18µ technology. For your low-power applications that require exceptional customer service, backed by complementary digital and mixed-signal IP offerings, AMIS is a secure and reliable manufacturing source and the best source for your application-specific needs.

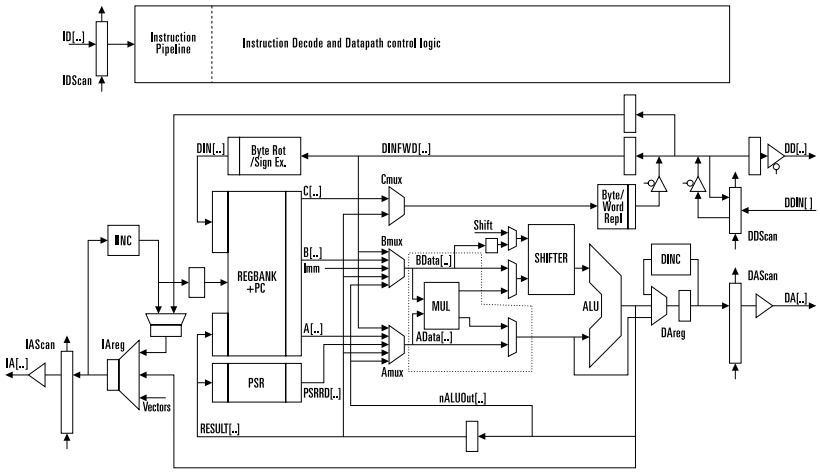
For an ARM922T data sheet or complete technical specifications please visit AMI Semiconductor’s Technical Library at www.amis.com.

## ARM9TDMI Architecture

The ARM9TDMI™ is a five-stage pipeline, 32-bit RISC processor. The processor architecture is a Harvard architecture, characterized by separate data and instruction caches and implementing a five-stage pipeline consisting of fetch, decode, execute, memory and write stages. The simple bus interface eases the connection to either a cached or static RAM-based memory system.

The core does support both bi-directional and unidirectional connection to external memory systems. The core also provides a simple handshake protocol for coprocessor support. The CPU has two instruction sets, the ARM and the Thumb instruction set.

The ARM instruction set has 32-bit wide instructions and provides maximum performance. Thumb instructions are 16-bits wide and give maximum code density. Instructions operate on 8-, 16- and 32-bit data types. Thumb instructions are decompressed to the equivalent ARM instructions in real time. This is done within the first phase of the decode stage and does not impact the micro-controller performance.




*Block Diagram of the ARM9TDMI processor*

## Thumb: The Key To Speed

A super-reduced instruction set actually gives the ARM922T processor two instruction sets:

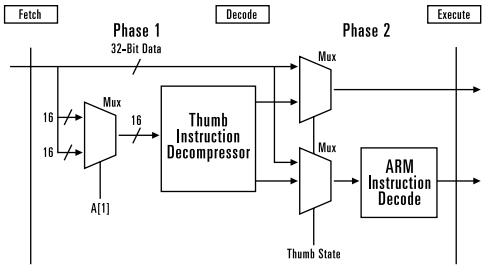
- A standard 32-bit ARM set
- A 16-bit Thumb instruction set

The Thumb set's 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARM's performance advantage over a traditional 16-bit processor using 16-bit registers. Thumb code is able to provide up to 65 percent of the code size of ARM, and 160 percent of the performance of an equivalent ARM processor connected to a 16-bit memory system.

Thumb instructions operate with the standard ARM register configuration, allowing excellent interoperability between ARM and Thumb states. Each 16-bit Thumb instruction has a corresponding 32-bit ARM instruction with the same effect on the processor.

Thumb implements a 16-bit instruction length on a 32-bit architecture, making the processing of 32-bit data efficient with a compact instruction coding. The performance exceeds that of a 16-bit architecture, with better code density than a 32-bit architecture.

Thumb can also switch back to full ARM code and execute at full speed, an advantage that other 32-bit architectures with 16-bit instructions can't deliver. This enables the coding of fast interrupts and DSP algorithms using the full ARM instruction set when linked with Thumb code. The overhead of switching from Thumb code to ARM code is folded into sub-routine entry time. Various portions of a system can be optimized for speed or for code density by switching between Thumb and ARM execution as appropriate.




*Flexible Section of ARM or Thumb Instruction Set*