1.0 Features

- 32-bit reduced instruction set computer (RISC) architecture
- Two instruction sets:
  - ARM® high-performance 32-bit instruction set
  - Thumb® high-code-density 16-bit instruction set
- Utilizes the ARM9TDMI™ processor core
- Very low power consumption
  - Industry-leader in MIPS/watt with performance > 200 MIPS
- Harvard architecture
  - 8K x 8 data cache
  - 8K x 8 instruction cache
  - Caches can be set to “write-through” or “write-back” mode
- Five-stage pipeline consisting of fetch, decode, execute, memory and write stages
- 8-, 16- and 32-bit data types
- ARM922T macrocell includes:
  - Memory management unit
  - Write buffer
  - AMBA™ bus interface
  - Embedded trace macrocell interface
- On-chip JTAG debug and in-circuit emulation
- Extensive range of third-party application development tools

2.0 Description

The ARM922T embedded macrocell is a member of the ARM family of general-purpose 32-bit microprocessors, which offer high performance and very low power consumption.

The ARM architecture is based on reduced instruction set computer (RISC) principles. The instruction set and related decode mechanism are much simpler than those of microprogrammed complex instruction set computers. This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective chip.

Pipelining is employed so that all parts of the processing and memory systems can operate continuously. The five-stage pipeline, utilizing a Harvard architecture consists of fetch, decode, execute, memory and write stages.

The ARM922T is targeted for use at multi-programmer applications where full memory management, high performance and low power are all important. The separate data and instruction caches are 8K x 8 in size. The macrocell also provides a version 4 (v4) MMU to provide translation and access permission checks for instruction and data addresses.

The ARM922T also supports the ARM debug architecture and includes logic to assist in hardware and software debug. Support is also provided on chip for coprocessors by exporting the instruction and data buses with simple handshaking signals. The ARM922T interfaces to the balance of the system over unified address and data buses, allowing implementation of either an advanced microcontroller architecture (AMBA), advanced system bus (ASB) or advanced high-performance bus (AHB) scheme either as a fully compliant AMBA bus master, or as a slave for production test.

Finally, the ARM922T provides the interface to, and supports the addition of an embedded trace macrocell (ETM) for real-time tracing of instructions and data.

The processor used with the ARM922T, the ARM9TDMI, employs a unique architectural implementation known as Thumb, which makes it ideally suited to high volume applications with memory restrictions or applications where code density is an issue.

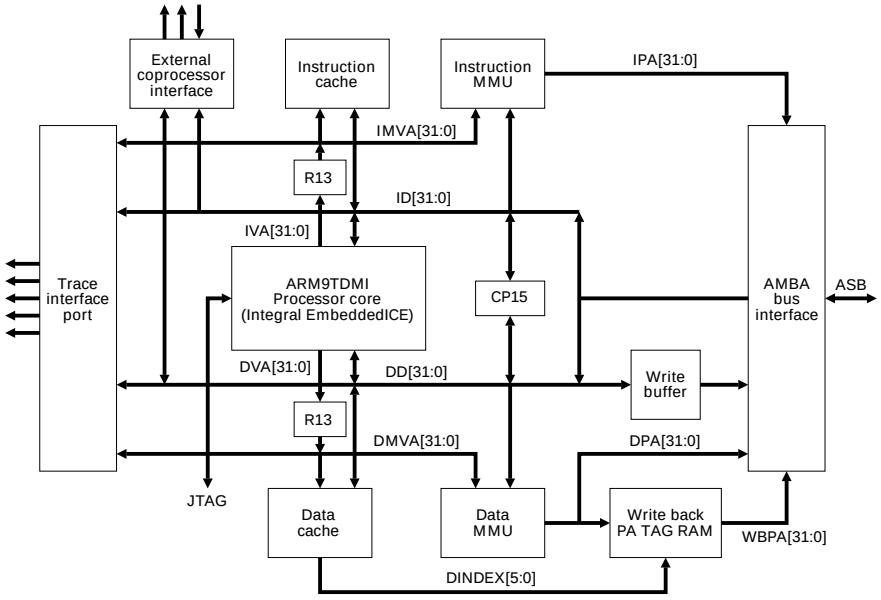
The key idea behind Thumb is that of a super-reduced instruction set. Essentially, the ARM9TDMI processor has two instruction sets:

- A standard 32-bit ARM set
- A 16-bit Thumb instruction set

The Thumb set’s 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARM’s performance advantage over a traditional 16-bit processor using 16-bit registers. This is possible because Thumb code operates on the same 32-bit register set as ARM code. Thumb code is able to provide up to 65 percent of the code size of ARM, and 160 percent of the performance of an equivalent ARM processor connected to a 16-bit memory system.

A functional diagram of the ARM922T macrocell is shown in Figure 1 on page 2.

Figure 1: *ARM922T Functional Block Diagram*



3.0 The Advantages of Thumb

Thumb instructions operate with the standard ARM register configuration, allowing excellent interoperability between ARM and Thumb states. Each 16-bit Thumb instruction has a corresponding 32-bit ARM instruction with the same effect on the processor model.

The major advantage of a 32-bit (ARM) architecture over a 16-bit architecture is its ability to manipulate 32-bit integers with single instructions, and to address a large address space efficiently. When processing 32-bit data, a 16-bit architecture will take at least two instructions to perform the same task as a single ARM instruction.

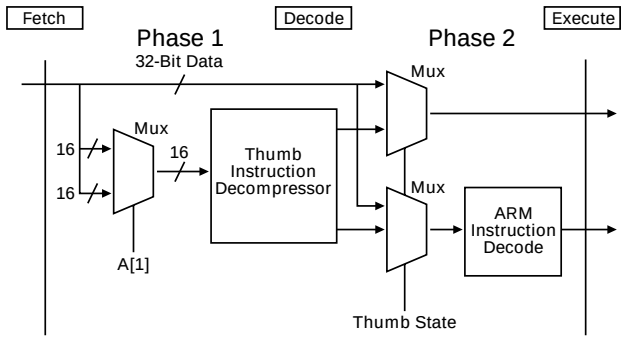
However, not all the code in a program will process 32-bit data (for example, code that performs character string handling), and other instructions, like branches, do not process any data at all.

When a 16-bit architecture only has 16-bit instructions, and a 32-bit architecture only has 32-bit instructions, the 16-bit architecture will have better code density, and better than one half the performance of the 32-bit architecture. Clearly 32-bit performance comes at the cost of code density.

Thumb breaks this constraint by implementing a 16-bit instruction length on a 32-bit architecture, making the processing of 32-bit data efficient with a compact instruction coding. This provides far better performance than a 16-bit architecture, with better code density than a 32-bit architecture.

Thumb also has a major advantage over other 32-bit architectures with 16-bit instructions. This is the ability to switch back to full ARM code and execute at full speed. Thus critical loops for applications such as fast interrupts and DSP algorithms can be coded using the full ARM instruction set, and linked with Thumb code. The overhead of switching from Thumb code to ARM code is folded into sub-routine entry time. Various portions of a system can be optimized for speed or for code density by switching between Thumb and ARM execution as appropriate.

Figure 2: *Flexible Section of ARM or Thumb Instruction Set*



4.0 ARM9TDMI Architecture

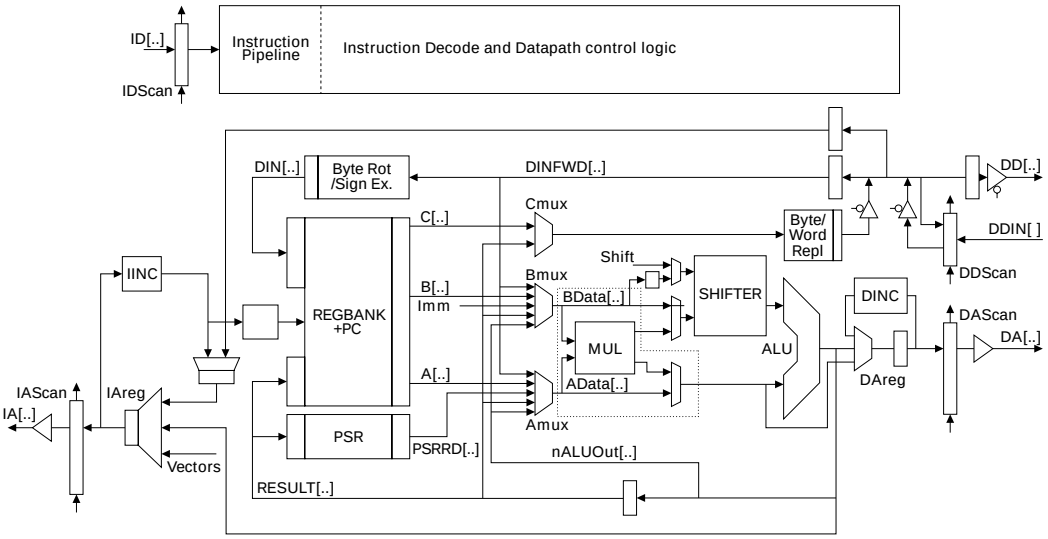
The ARM9TDMI is a five-stage pipeline, 32-bit RISC processor. The processor architecture is a Harvard architecture, characterized by separate data and instruction caches and implementing a five-stage pipeline consisting of fetch, decode, execute, memory and write stages. The simple bus interface eases connection to either a cached or static RAM-based memory system.

The core supports both bi-directional and unidirectional connection to external memory systems. Finally, the core also provides a simple handshake protocol for coprocessor support. The CPU also supports two instruction sets, the ARM and the Thumb instruction set as previously described.

The ARM instruction set has 32-bit wide instructions and provides maximum performance. Thumb instructions are 16-bits wide and give maximum code-density. Instructions operate on 8-, 16- and 32-bit data types. Thumb instructions are decompressed to the equivalent ARM instructions in real time. This is done within the first phase of the decode stage and does not impact the microcontroller performance.

The ARM9TDMI processor block diagram is shown in Figure 3.

Figure 3: *ARM9TDMI Processor Block Diagram*



5.0 Process Support at AMIS

AMI Semiconductor (AMIS) supports the ARM922T embedded macrocell in a 0.18µ technology. For your low-power applications that require exceptional customer service, backed by complementary digital and mixed-signal IP offerings, AMIS is a secure and reliable manufacturing source and the best source for your application-specific needs. For complete technical specifications on the ARM922T, please visit AMI Semiconductor's Technical Library at: www.amis.com/tech_library.cfm.