NEC

MOS INTEGRATED CIRCUIT

# μPD23C32000A

## 32M-BIT MASK-PROGRAMMABLE ROM
## 4M-WORD BY 8-BIT (BYTE MODE)/2M-WORD BY 16-BIT (WORD MODE)

### Description

The μPD23C32000A is a 33,554,432 bits mask-programmable ROM. The word organization is selectable (BYTE mode: 4,194,304 words by 8 bits, WORD mode: 2,097,152 words by 16 bits).

The active levels of OE (Output Enable Input) can be selected with mask-option.

The μPD23C32000A is packed in 44-pin plastic SOP, 48-pin plastic TSOP (I), and 44-pin plastic TSOP (II).

### Features

- Word organization
  - 4,194,304 words by 8 bits (BYTE mode)
  - 2,097,152 words by 16 bits (WORD mode)
- Access time 120 ns (MAX.)
- Low current consumption
  - Active ····· 70 mA (MAX.)
  - Standby ····· 100 μA (MAX.) (CMOS level input)

### ★ Ordering Information

| Part Number | Package |
|---|---|
| μPD23C32000AGX-×××  | 44-pin Plastic SOP (600 mil) |
| μPD23C32000AGY-×××-MJH | 48-pin Plastic TSOP (I) (12 × 18 mm) (Normal bent) |
| μPD23C32000AGY-×××-MKH | 48-pin Plastic TSOP (I) (12 × 18 mm) (Reverse bent) |
| μPD23C32000AG5-×××-7JF**Note** | 44-pin Plastic TSOP (II) (400 mil) (Normal bent) |

(×××: ROM code suffix No.)

**Note** Under development

**The information in this document is subject to change without notice.**

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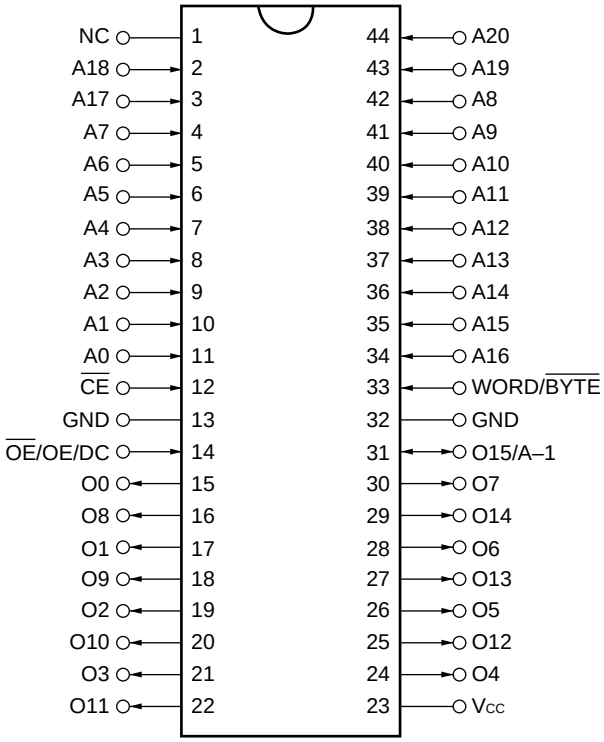
Printed in Japan

**The mark ★ shows major revised points.**

## ★ Pin Configuration (Marking Side)

**44-pin Plastic SOP (600 mil)**

**[μPD23C32000AGX]**



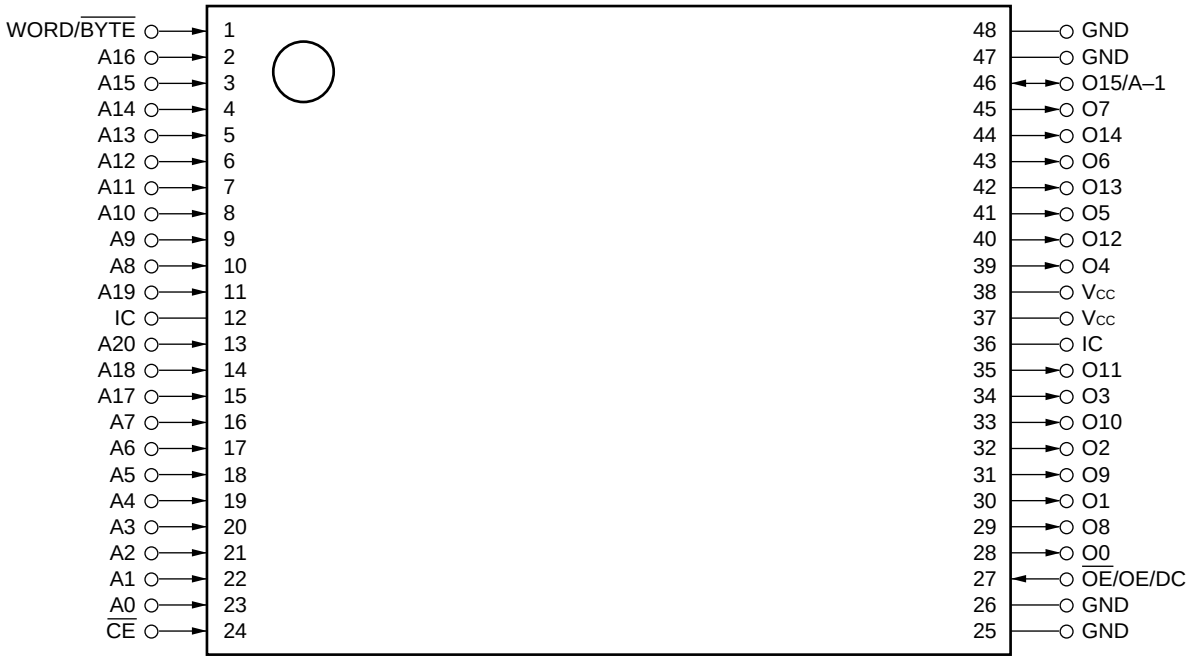

| | | |
|---|---|---|
| A0 - A20 | : | Address inputs |
| O0 - 07, O8 - O14 | : | Data outputs |
| O15/A–1 | : | Data 15 ouput (WORD mode)/LSB address input (BYTE mode) |
| WORD/$\overline{\text{BYTE}}$ | : | Mode select |
| $\overline{\text{CE}}$ | : | Chip enable |
| $\overline{\text{OE}}$/OE | : | Output enable |
| $V_{CC}$ | : | Supply voltage |
| GND | : | Ground |
| NC**Note 1** | : | No connection |
| IC**Note 2** | : | Internal connection |
| DC | : | Don't care |

**Notes 1.** Some signals can be applied because this pin is not connected to the inside of the chip.

**2.** Leave this pin unconnected or connect to GND.

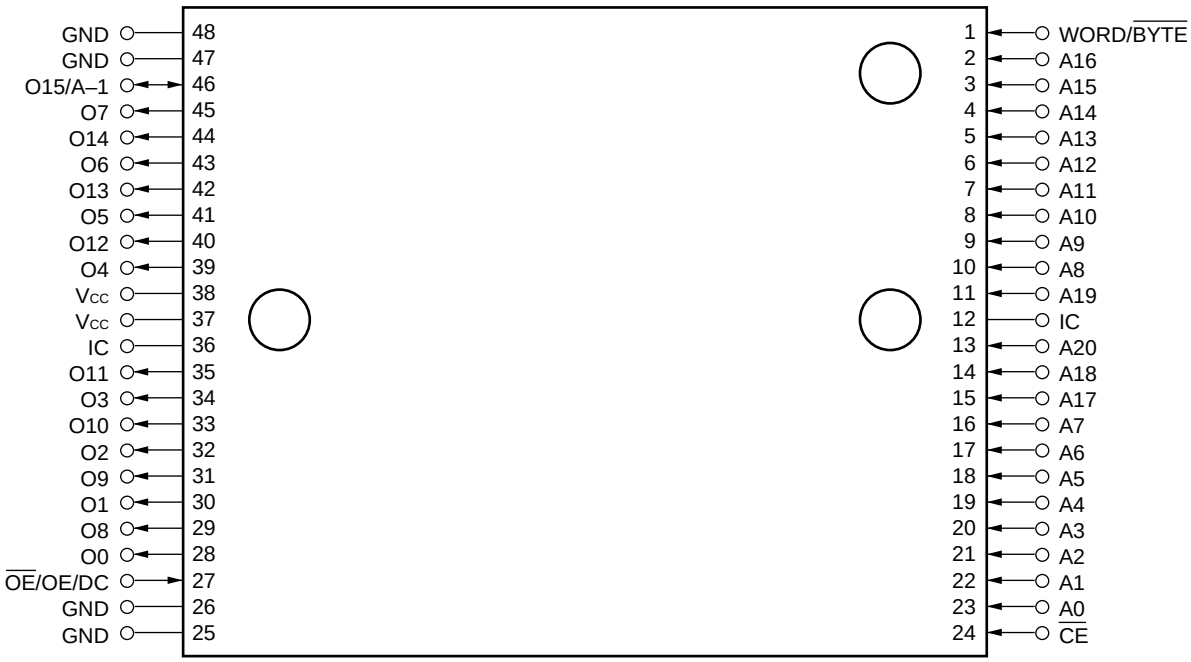
**48-pin Plastic TSOP (I) (12 × 18 mm) (Normal bent)**

**[μPD23C32000AGY-MJH]**



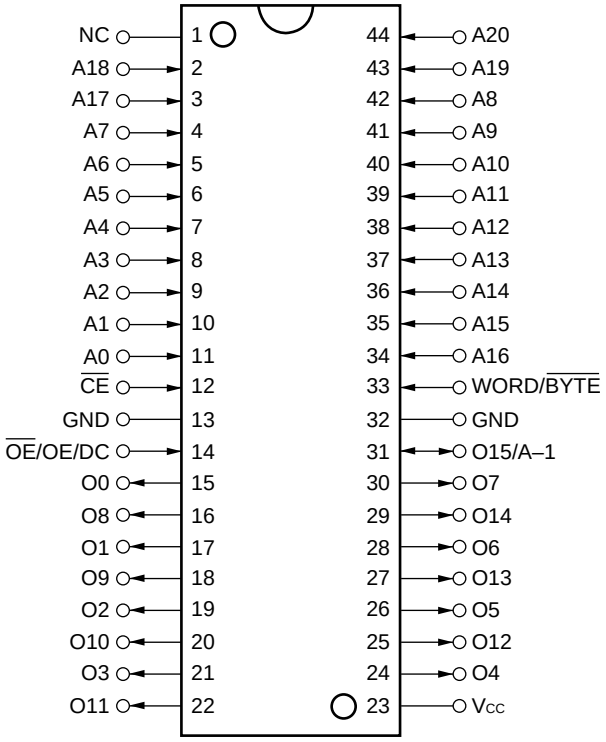

**48-pin Plastic TSOP (I) (12 × 18 mm) (Reverse bent)**

**[μPD23C32000AGY-MKH]**



**44-pin Plastic TSOP (II) (400 mil) (Normal bent)**

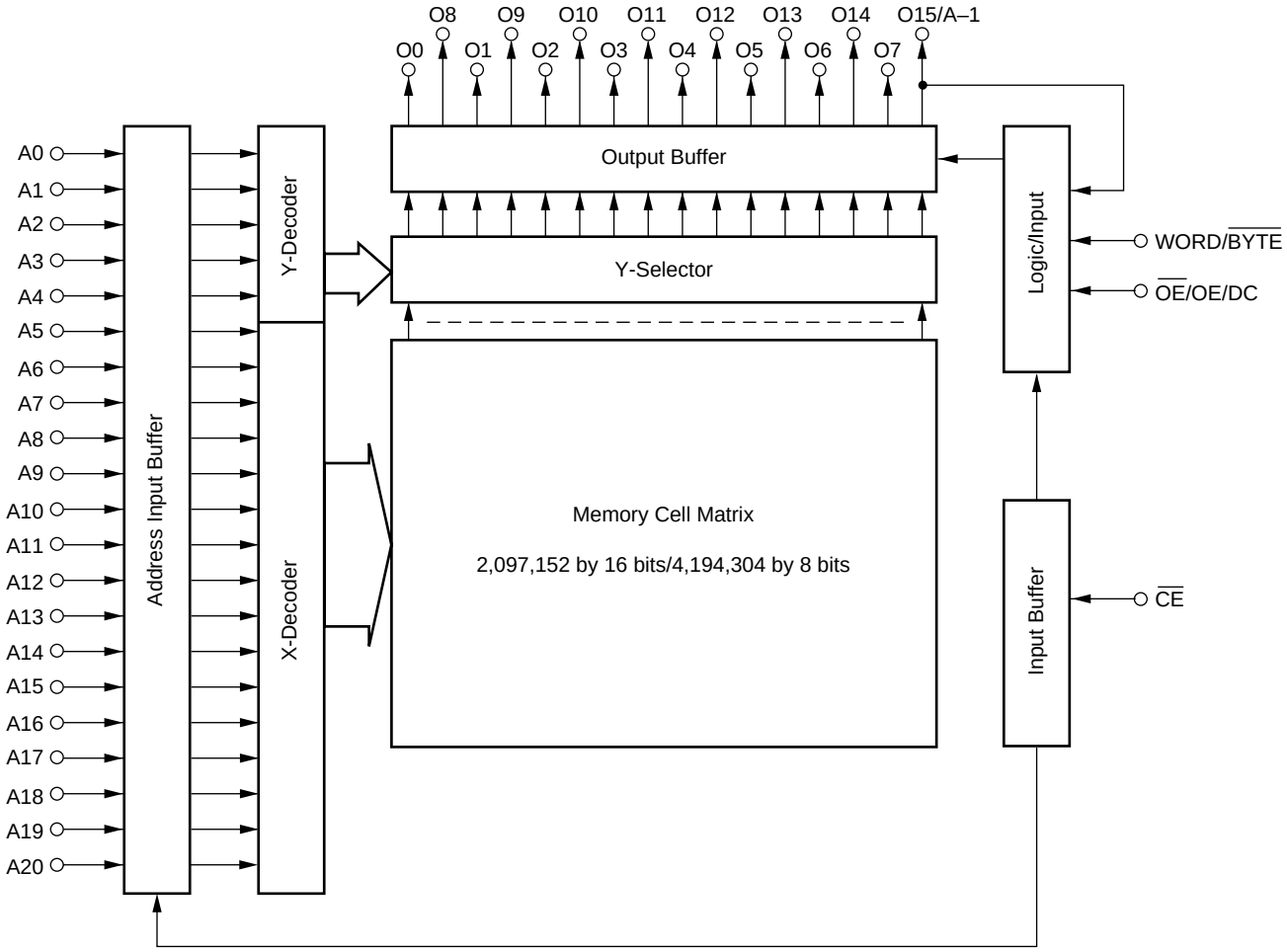
**[μPD23C32000AG5-7JF]**



## Input/Output Pin Functions

| Pin name | Input/ Output | Function |
|---|---|---|
| WORD/$\overline{BYTE}$ | Input | The pin for switching word mode and byte mode.<br>High level ····· Word mode (2M-word by 16 bits)<br>Low level ····· Byte mode (4M-word by 8 bits) |
| A0 to A20<br>(Address input) | | Address bus. A0 to A20 are used differently in the word mode (2M-word by 16 bits) and the byte mode (4M-word by 8 bits).<br>Word mode ····· A0 to A20 are used as 21 bits address signals.<br>Byte mode ····· A0 to A20 are used as the upper 21 bits of total 22 bits of address signal. (The least significant bit (A–1) is combined to O15.) |
| O0 to O7, O8 to O14<br>(Data output) | Output | Output data bus. O0 to O7, O8 to O14 are used differently in the word (2M-word by 16 bits) and the byte mode (4M-word by 8 bits).<br>Word mode ····· The lower 15 bits of 16 bits data outputs to O0 to O14. (The most significant bit (O15) combined to A–1.)<br>Byte mode ····· 8 bits data outputs to O0 to O7 and also O8 to O14 is high impedance. |
| O15/A–1<br>(Data output 15)/<br>(LSB Address input) | Output/ Input | O15/A–1 are used differently in the word (2M-word by 16 bits) and the byte mode (4M-word by 8 bits).<br>Word mode ····· The most significant output data bus (O15).<br>Byte mode ····· The least significant address bus (A–1). |
| $\overline{CE}$<br>(Chip Enable) | Input | Chip activating signal.<br>When the OE is active, output states are following.<br>High level ····· High impedance<br>Low level ····· Data out |
| $\overline{OE}$/OE/DC<br>(Output Enable/Don't care) | | Output enable signal. The active level of OE is mask option. The active level of OE can be selected from high active, low active and Don't care at order. |
| $V_{CC}$ | — | Supply voltage |
| GND | — | Ground |
| NC | — | Not internally connected. (The signal can be connected.) |
| IC | — | Internally connected. (Leave this pin unconnected or connect to GND.) |

## Block Diagram



## Mask Option

The active levels of output enable pin ($\overline{OE}$/OE/DC) are mask programmable and optional, and can be selected from among “0” “1” “×” shown in the table below.

| Option | $\overline{OE}$/OE/DC | OE active level |
|---|---|---|
| 0 | $\overline{OE}$ | L |
| 1 | OE | H |
| × | DC | Don’t care |

Operation modes for each option are shown in the tables below.

Operation mode (Option: 0)

| $\overline{CE}$ | $\overline{OE}$ | Mode | Output state |
|---|---|---|---|
| L | L | Active | Data out |
| | H | | High impedance |
| H | H or L | Standby | High impedance |

Operation mode (Option: 1)

| $\overline{CE}$ | OE | Mode | Output state |
|---|---|---|---|
| L | L | Active | High impedance |
| | H | | Data out |
| H | H or L | Standby | High impedance |

Operation mode (Option: ×)

| $\overline{CE}$ | DC | Mode | Output state |
|---|---|---|---|
| L | H or L | Active | Data out |
| H | H or L | Standby | High impedance |

**Remark** L: Low level input
H: High level input

## Electrical Specifications

### Absolute Maximum Ratings

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | | –0.3 to +7.0 | V |
| Input voltage | $V_I$ | | –0.3 to $V_{CC}$ +0.3 | V |
| Output voltage | $V_O$ | | –0.3 to $V_{CC}$ +0.3 | V |
| Operating ambient temperature | $T_A$ | | –10 to +70 | ˚C |
| Storage temperature | $T_{stg}$ | | –65 to +150 | ˚C |

**Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.**

### Capacitance ($T_A$ = 25 ˚C)

| Parameter | Symbol | Test conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Input capacitance | $C_I$ | f = 1 MHz | | | 10 | pF |
| Output capacitance | $C_O$ | | | | 12 | pF |

### DC Characteristics ($T_A$ = –10 to +70 ˚C, $V_{CC}$ = 5.0 V ± 10 %)

| Parameter | Symbol | Test conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| High level input voltage | $V_{IH}$ | | 2.2 | | $V_{CC}$ +0.3 | V |
| Low level input voltage | $V_{IL}$ | | –0.3 | | +0.8 | V |
| High level output voltage | $V_{OH1}$ | $I_{OH}$ = –400 μA | 2.4 | | | V |
| | $V_{OH2}$ | $I_{OH}$ = –100 μA | $V_{CC}$ –0.5 | | | |
| Low level output voltage | $V_{OL}$ | $I_{OL}$ = 2.1 mA | | | 0.4 | V |
| Input leakage current | $I_{LI}$ | $V_I$ = 0 to $V_{CC}$ | –10 | | +10 | μA |
| Output leakage current | $I_{LO}$ | $V_O$ = 0 to $V_{CC}$, Chip deselected | –10 | | +10 | μA |
| Power supply current | $I_{CC1}$ | $\overline{CE}$ = $V_{IL}$ (Active mode), $I_O$ = 0 mA | | | 70 | mA |
| Standby current | $I_{CC2}$ | $\overline{CE}$ = $V_{IH}$ (Standby mode) | | | 1.5 | mA |
| | $I_{CC3}$ | $\overline{CE}$ = $V_{CC}$ –0.2 V (Standby mode) | | | 100 | μA |

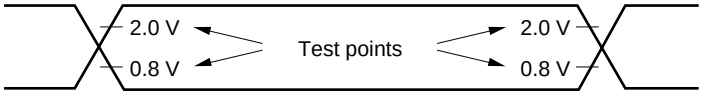
**AC Characteristics ($T_A$ = –10 to +70 °C, $V_{CC}$ = 5.0 V ±10 %)**

| Parameter | Symbol | Test conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Address access time | $t_{ACC}$ | | | | 120 | ns |
| Chip enable access time | $t_{CE}$ | | | | 120 | ns |
| Output enable access time | $t_{OE}$ | | | | 50 | ns |
| Output hold time | $t_{OH}$ | | 0 | | | ns |
| Output disable time | $t_{DF}$ | | 0 | | 25 | ns |
| WORD/$\overline{BYTE}$ access time | $t_{WB}$ | | | | 120 | ns |

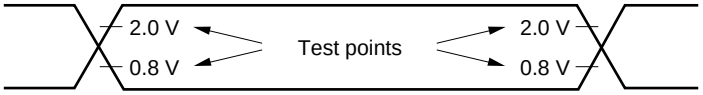
**Remark** $t_{DF}$ is the time from inactivation of $\overline{CE}$ or $\overline{OE}$/OE to high-impedance state output.

**AC Test Conditions**

Input waveform (Rise/Fall time ≤ 5 ns)



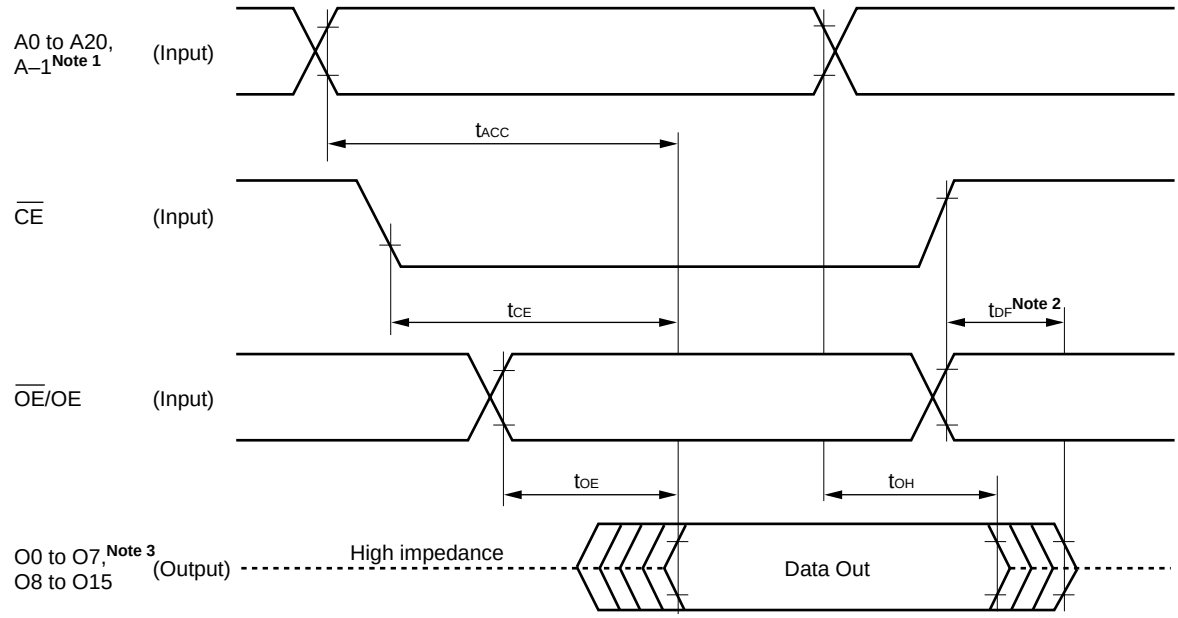

Output waveform




Output load

1TTL + 100 pF

**Read Cycle Timing Chart**

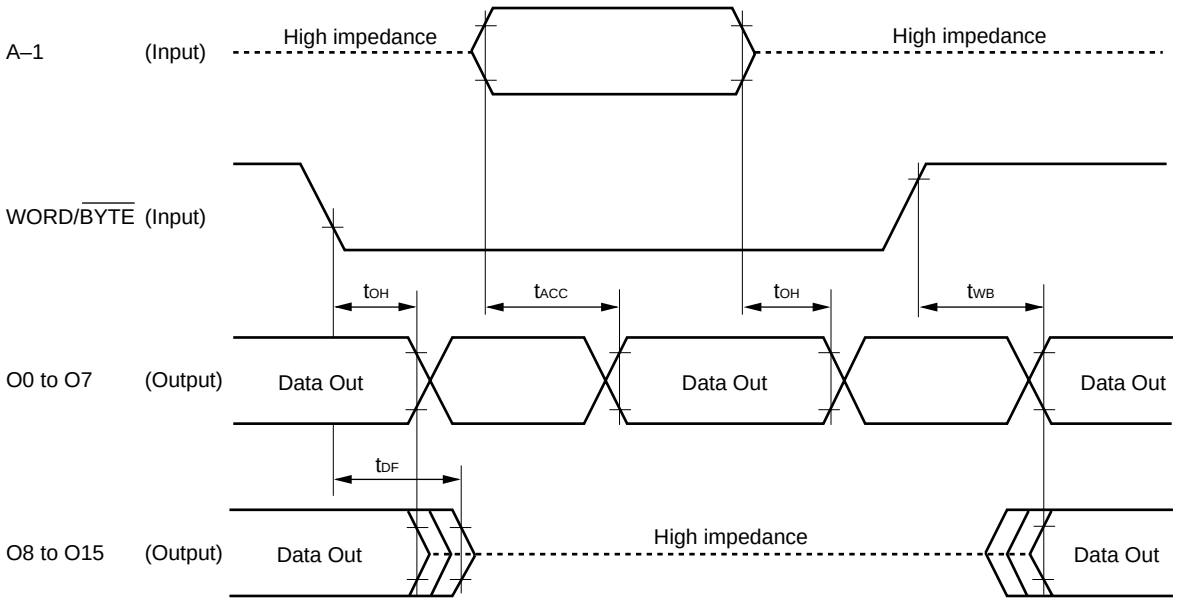



**Notes 1.** During WORD mode, A–1 is O15.

**2.** $t_{DF}$ is specified when the one of $\overline{CE}$, $\overline{OE}$ or OE is inactivated.

**3.** During BYTE mode, O8 to O14 are high impedance and O15 is A–1.

**WORD/$\overline{BYTE}$ Switch Timing Chart**



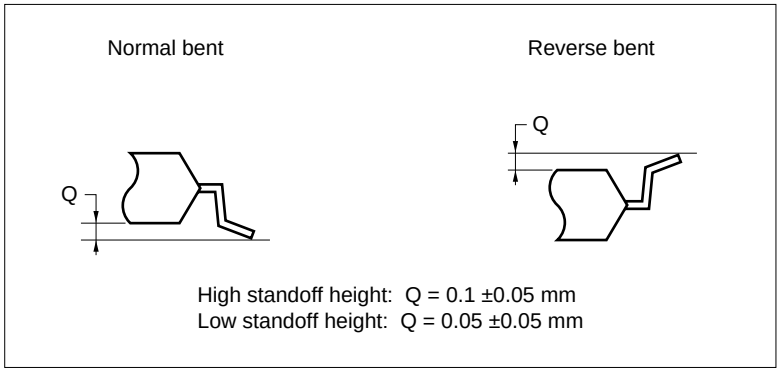

**Remark** $\overline{OE}$/OE, $\overline{CE}$: Active.

★ **Notice of change in 48-pin TSOP (I) standoff height**

We are changing the 48-pin TSOP (I) standoff height 0.05 ±0.05 mm (low standoff height) to 0.1 ±0.05 mm (high standoff height). Each lot version is identified by the fifth character of the lot number.

**Difference between high standoff height and low standoff height**

**Detail of lead end**

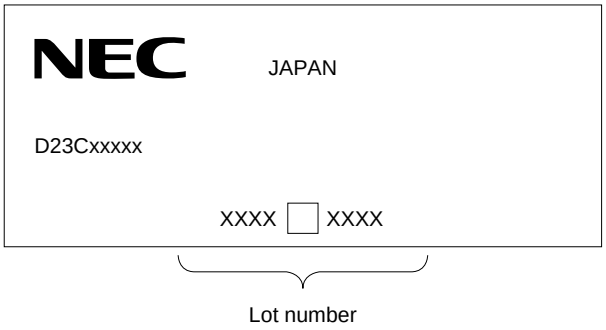



**Identification of each lot version**

Each lot version is identified by the fifth character of the lot number.

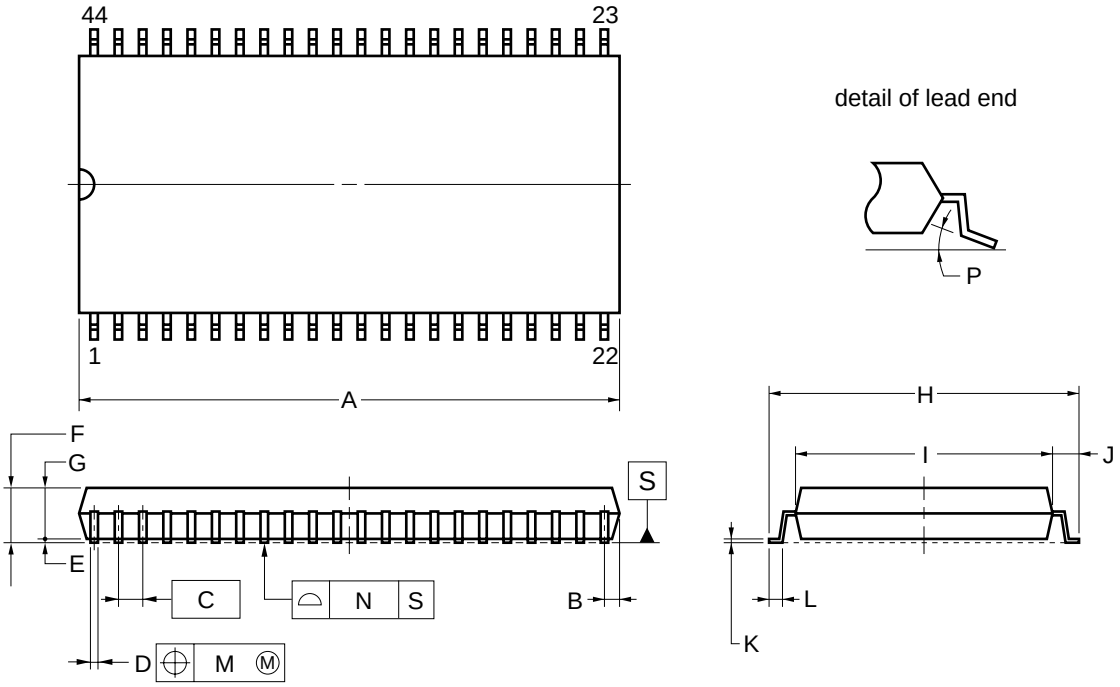
| Fifth character of the lot number | Lot version | Standoff height |
|---|---|---|
| L | L version | 0.1 ±0.05 mm (High standoff height) |
| K | K version | 0.05 ±0.05 mm (Low standoff height) |

**Marking Example**



★ **Package Drawings**

## 44 PIN PLASTIC SOP (600 mil)




**NOTE**

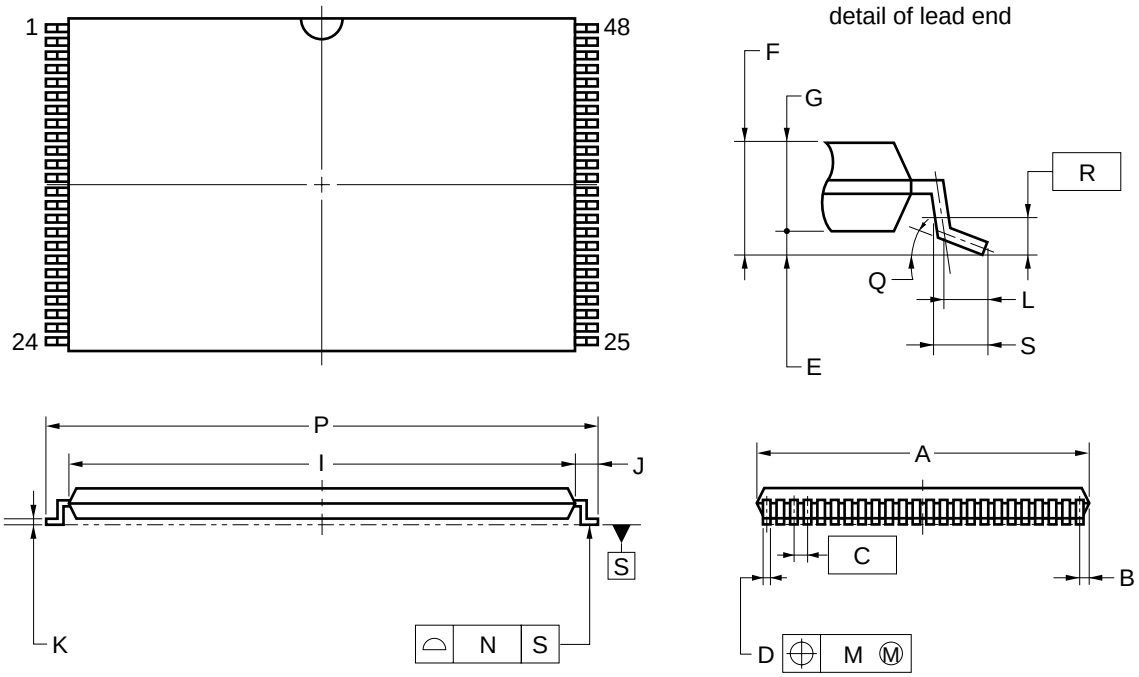
1. Controlling dimension —— millimeter.
2. Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | $27.83^{+0.4}_{-0.05}$ | $1.096^{+0.016}_{-0.003}$ |
| B | 0.78 MAX. | 0.031 MAX. |
| C | 1.27 (T.P.) | 0.050 (T.P.) |
| D | $0.42^{+0.08}_{-0.07}$ | $0.017^{+0.003}_{-0.004}$ |
| E | 0.15±0.1 | 0.006±0.004 |
| F | 3.0 MAX. | 0.119 MAX. |
| G | 2.7±0.05 | $0.106^{+0.003}_{-0.002}$ |
| H | 16.04±0.3 | $0.631^{+0.013}_{-0.012}$ |
| I | 13.24±0.1 | $0.521^{+0.005}_{-0.004}$ |
| J | 1.4±0.2 | 0.055±0.008 |
| K | $0.22^{+0.08}_{-0.07}$ | $0.009^{+0.003}_{-0.004}$ |
| L | 0.8±0.2 | $0.031^{+0.009}_{-0.008}$ |
| M | 0.12 | 0.005 |
| N | 0.10 | 0.004 |
| P | $3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$ | $3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$ |

**P44GX-50-600A-3**

**L Version: High standoff height**

## 48 PIN PLASTIC TSOP (I) (12×18)




**NOTES**

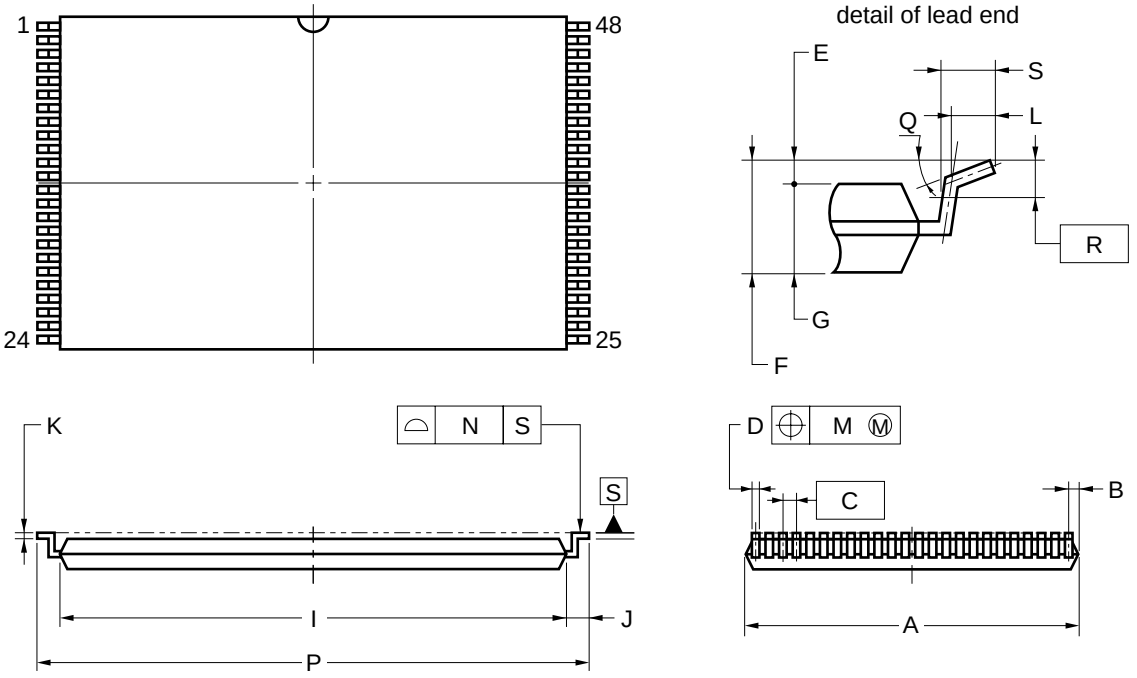
1. Controlling dimension — Millimeter.
2. Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.
3. "A" excludes mold flash. (Includes mold flash : 12.4 mm MAX. <0.489 inch MAX.>)

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | 12.0±0.1 | $0.472^{+0.005}_{-0.004}$ |
| B | 0.45 MAX. | 0.018 MAX. |
| C | 0.5 (T.P.) | 0.020 (T.P.) |
| D | 0.22±0.05 | $0.009^{+0.002}_{-0.003}$ |
| E | 0.1±0.05 | 0.004±0.002 |
| F | 1.2 MAX. | 0.048 MAX. |
| G | 1.0±0.05 | $0.039^{+0.003}_{-0.002}$ |
| I | 16.4±0.1 | $0.646^{+0.004}_{-0.005}$ |
| J | 0.8±0.2 | $0.031^{+0.009}_{-0.008}$ |
| K | 0.145±0.05 | $0.006^{+0.002}_{-0.003}$ |
| L | 0.5 | 0.020 |
| M | 0.10 | 0.004 |
| N | 0.10 | 0.004 |
| P | 18.0±0.2 | $0.709^{+0.008}_{-0.009}$ |
| Q | $3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$ | $3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$ |
| R | 0.25 | 0.010 |
| S | 0.60±0.15 | $0.024^{+0.006}_{-0.007}$ |

**S48GY-50-MJH1**

**L Version: High standoff height**

## 48 PIN PLASTIC TSOP (I) (12×18)




**NOTES**

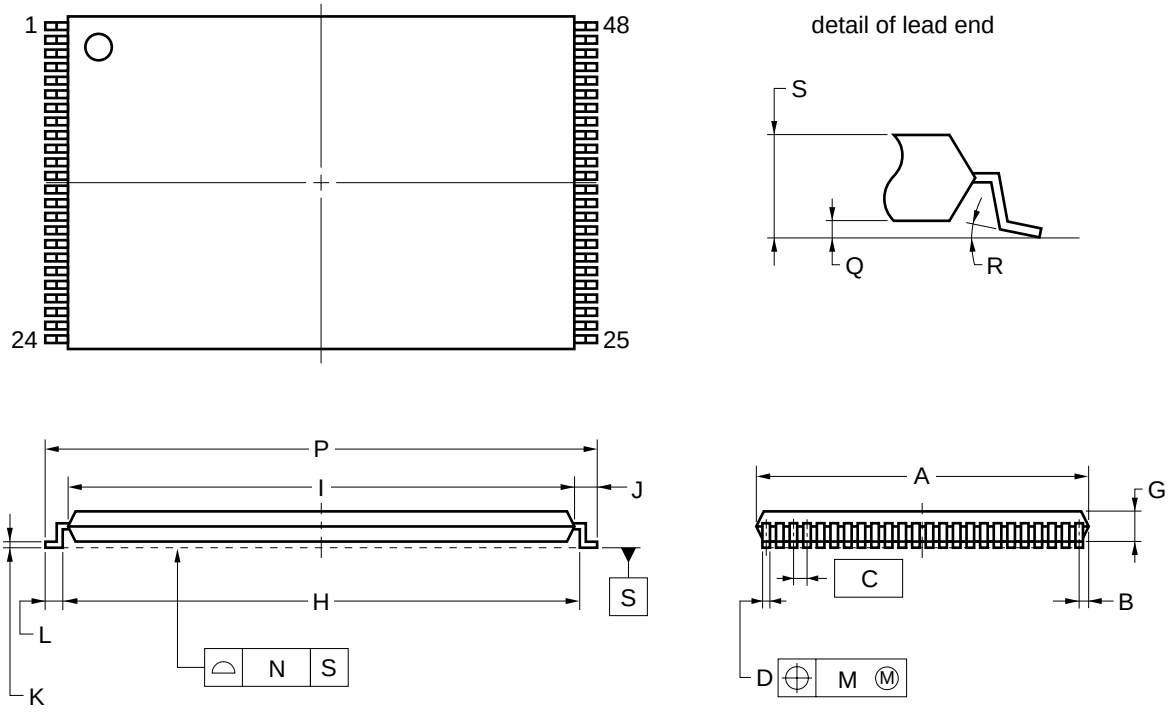
1. Controlling dimension —— Millimeter.
2. Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.
3. "A" excludes mold flash. (Includes mold flash : 12.4 mm MAX. <0.489 inch MAX.>)

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | 12.0±0.1 | $0.472^{+0.005}_{-0.004}$ |
| B | 0.45 MAX. | 0.018 MAX. |
| C | 0.5 (T.P.) | 0.020 (T.P.) |
| D | 0.22±0.05 | $0.009^{+0.002}_{-0.003}$ |
| E | 0.1±0.05 | 0.004±0.002 |
| F | 1.2 MAX. | 0.048 MAX. |
| G | 1.0±0.05 | $0.039^{+0.003}_{-0.002}$ |
| I | 16.4±0.1 | $0.646^{+0.004}_{-0.005}$ |
| J | 0.8±0.2 | $0.031^{+0.009}_{-0.008}$ |
| K | 0.145±0.05 | $0.006^{+0.002}_{-0.003}$ |
| L | 0.5 | 0.020 |
| M | 0.10 | 0.004 |
| N | 0.10 | 0.004 |
| P | 18.0±0.2 | $0.709^{+0.008}_{-0.009}$ |
| Q | $3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$ | $3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$ |
| R | 0.25 | 0.010 |
| S | 0.60±0.15 | $0.024^{+0.006}_{-0.007}$ |

**S48GY-50-MKH1**

**K Version: Low standoff height**

## 48 PIN PLASTIC TSOP (I) (12x18)




**NOTES**

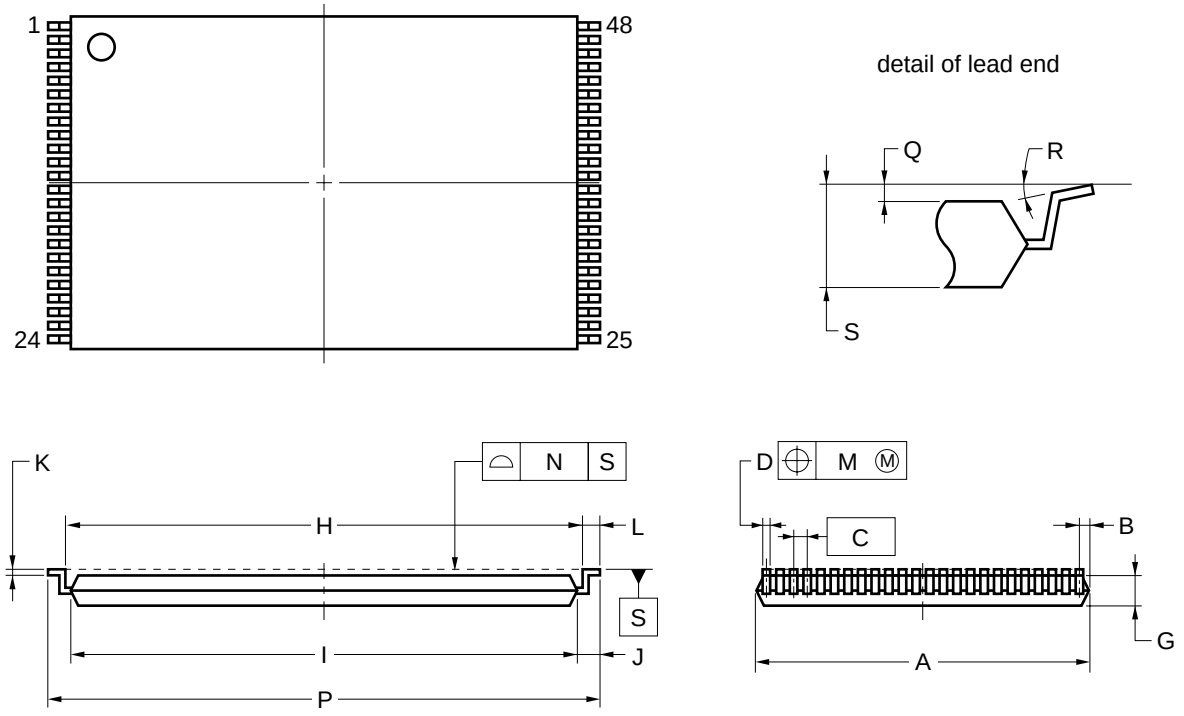
1. Controlling dimension —— millimeter.
2. Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.
3. "A" excludes mold flash. (Includes mold flash : 12.4 mm MAX. <0.489 inch MAX.>)

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | 12.0±0.1 | $0.472^{+0.005}_{-0.004}$ |
| B | 0.45 MAX. | 0.018 MAX. |
| C | 0.5 (T.P.) | 0.020 (T.P.) |
| D | $0.22^{+0.08}_{-0.07}$ | $0.009^{+0.003}_{-0.004}$ |
| G | 0.97 | 0.038 |
| H | 17.0±0.2 | $0.669^{+0.009}_{-0.008}$ |
| I | 16.4±0.1 | $0.646^{+0.004}_{-0.005}$ |
| J | 0.8±0.2 | $0.031^{+0.009}_{-0.008}$ |
| K | $0.145^{+0.03}_{-0.055}$ | $0.006^{+0.001}_{-0.003}$ |
| L | 0.5±0.1 | $0.020^{+0.004}_{-0.005}$ |
| M | 0.08 | 0.003 |
| N | 0.10 | 0.004 |
| P | 18.0±0.2 | $0.709^{+0.008}_{-0.009}$ |
| Q | 0.05±0.05 | 0.002±0.002 |
| R | $2^{\circ}{}^{+4^{\circ}}_{-2^{\circ}}$ | $2^{\circ}{}^{+4^{\circ}}_{-2^{\circ}}$ |
| S | 1.02±0.08 | $0.040^{+0.004}_{-0.003}$ |

**S48GY-50-MJH-3**

**K Version: Low standoff height**

## 48 PIN PLASTIC TSOP (I) (12x18)



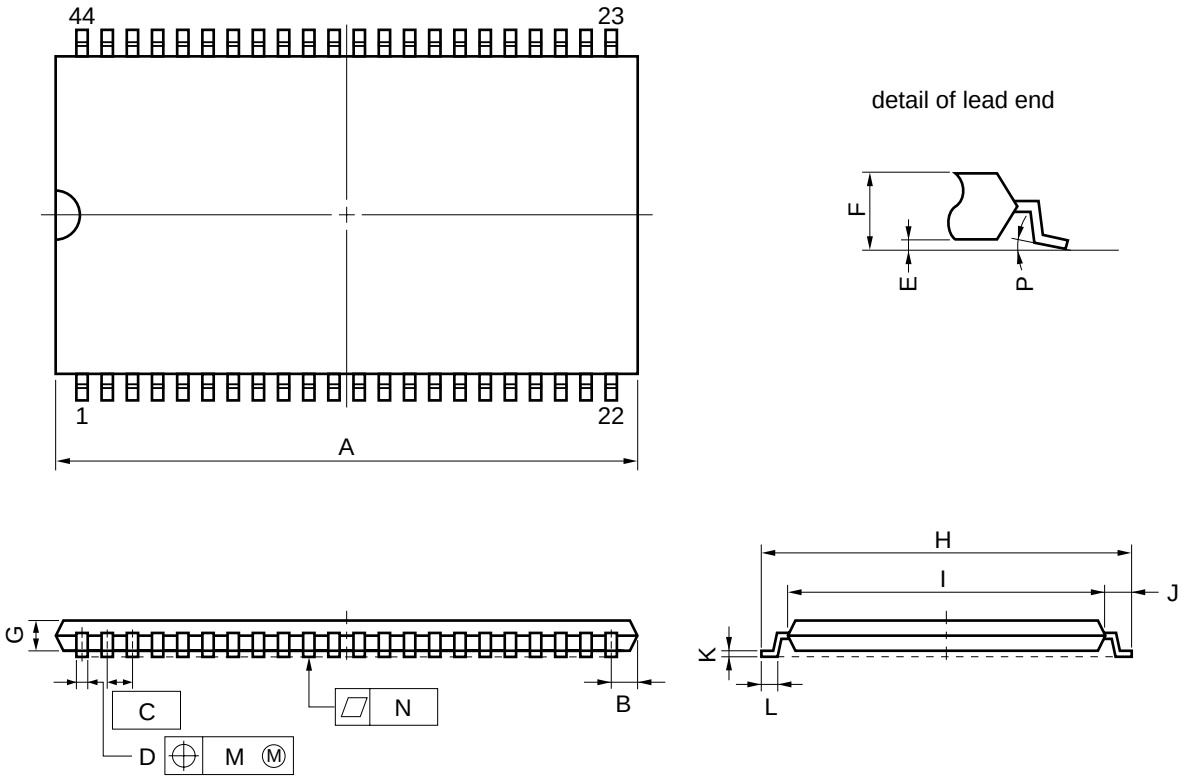

**NOTES**

1. Controlling dimension —— millimeter.
2. Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.
3. "A" excludes mold flash. (Includes mold flash : 12.4 mm MAX. <0.489 inch MAX.>)

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | 12.0±0.1 | $0.472^{+0.005}_{-0.004}$ |
| B | 0.45 MAX. | 0.018 MAX. |
| C | 0.5 (T.P.) | 0.020 (T.P.) |
| D | $0.22^{+0.08}_{-0.07}$ | $0.009^{+0.003}_{-0.004}$ |
| G | 0.97 | 0.038 |
| H | 17.0±0.2 | $0.669^{+0.009}_{-0.008}$ |
| I | 16.4±0.1 | $0.646^{+0.004}_{-0.005}$ |
| J | 0.8±0.2 | $0.031^{+0.009}_{-0.008}$ |
| K | $0.145^{+0.03}_{-0.055}$ | $0.006^{+0.001}_{-0.003}$ |
| L | 0.5±0.1 | $0.020^{+0.004}_{-0.005}$ |
| M | 0.08 | 0.003 |
| N | 0.10 | 0.004 |
| P | 18.0±0.2 | $0.709^{+0.008}_{-0.009}$ |
| Q | 0.05±0.05 | 0.002±0.002 |
| R | $2^{\circ}{}^{+4^{\circ}}_{-2^{\circ}}$ | $2^{\circ}{}^{+4^{\circ}}_{-2^{\circ}}$ |
| S | 1.02±0.08 | $0.040^{+0.004}_{-0.003}$ |

**S48GY-50-MKH-3**

## 44 PIN PLASTIC TSOP(II) (400 mil)




**NOTE**

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | 18.63 MAX. | 0.734 MAX. |
| B | 0.93 MAX. | 0.037 MAX. |
| C | 0.8 (T.P.) | 0.031 (T.P.) |
| D | $0.32^{+0.08}_{-0.07}$ | 0.013±0.003 |
| E | 0.1±0.05 | 0.004±0.002 |
| F | 1.2 MAX. | 0.048 MAX. |
| G | 0.97 | 0.038 |
| H | 11.76±0.2 | 0.463±0.008 |
| I | 10.16±0.1 | 0.400±0.004 |
| J | $0.8\pm0.2$ | $0.031^{+0.009}_{-0.008}$ |
| K | $0.145^{+0.025}_{-0.015}$ | 0.006±0.001 |
| L | 0.5±0.1 | $0.020^{+0.004}_{-0.005}$ |
| M | 0.13 | 0.005 |
| N | 0.10 | 0.004 |
| P | $3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$ | $3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$ |

**S44G5-80-7JF5**

## Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD23C32000A.

**Types of Surface Mount Device**

μPD23C32000AGX : 44-pin Plastic SOP (600 mil)
μPD23C32000AGY-MJH : 48-pin Plastic TSOP (I) (12 × 18 mm) (Normal bent)
μPD23C32000AGY-MKH : 48-pin Plastic TSOP (I) (12 × 18 mm) (Reverse bent)
μPD23C32000AG5-7JF : 44-pin Plastic TSOP (II) (400 mil) (Normal bent)

## NOTES FOR CMOS DEVICES

### ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

**Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.**

### ② HANDLING OF UNUSED INPUT PINS FOR CMOS

**Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to $V_{DD}$ or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.**

### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

**Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.**

**[MEMO]**

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