Features

- **All-in-one Design**
  - **MIDI Control Processor**
  - **Synthesis**
  - **Compatible Effects: Reverb and Chorus**
  - **Microphone Echo Processing (Two Channels)**
  - **Programmable Spatializer or Four-channel Surround**
  - **4-band Stereo Equalizer**
- **High-quality Synthesis**
  - **Maximum 48-voice Polyphony and Reverb/Chorus (34 if all features on)**
  - **24 dB Resonant Filter per Voice**
  - **16-bit Samples**
  - **Alternate Loop**
  - **Internal Computations on 28 Bits**
- **Crisp MIDI Response: Built-in 16-bit Processor Runs at 38.4 MHz**
- **High-quality Sound Post-processing**
  - **13 Delay Lines for Stereo Reverb**
  - **Programmable Stereo Echo for Microphone**
  - **Spatializer/Surround Allows Wide Stereo Image for Strong Sound Presence**
- **Top Technology**
  - **Synthesizer Chip Set: SAM9703 + 32-Mbit ROM + 32K x 8 RAM + DAC or Codec**
  - **Single 9.6 MHz Crystal with Built-in PLL**
  - **100-lead TQFP Space Saver Package**
- **Standard Firmware includes Top-quality CleanWave® Sound Set and Other Sample Sets under Special Conditions**
- **Typical Applications: Karaokes, Musical instruments, Battery-operated Instruments**
- **Pin- and Function-compatible with SAM9503, with Additional Features:**
  - **Lower Consumption**
  - **3.3V Core Supply, 3V to 5.5V Periphery Supply**
  - **Up to 8 Channels Audio-in**

Note: Pin-to-pin replacement for SAM9503 requires 3.3V core supply V_{C3}.

Description

The highly-integrated architecture of the SAM9703 device combines a specialized high-performance RISC digital signal processor and a general-purpose 16-bit CISC control processor on a single chip. An on-chip memory management unit allows the digital signal processor and the control processor to share external ROM and RAM devices. The ROM bus width should be 16 bits, while the SRAM can be selected to be 8 or 16 bits wide. When using an 8-bit SRAM, fast type (static cache) should be selected as two SRAM cycles will be done in one ROM cycle duration.

Running at 300 million operations per second (MOPS), the digital signal processor supports high-quality PCM synthesis as well as most important functions like reverb, chorus, surround effect and equalizer. By adding an additional stereo DAC, four-channel audio surround can be obtained as well.

Computer karaoke manufacturers will enjoy the built-in high-quality dual-microphone echo processing.

Dream® licenses a 32-Mbit jumper-configurable firmware ROM, CleanWave32®, which includes high-quality General MIDI-compliant synthesis with many additional sounds and drumsets. Please refer to the corresponding CleanWave32® datasheet. Other sample sets are available under special conditions.

More information, including licensing, can be obtained from any Atmel sales office.

Smaller capacity firmwares are also available for more cost-sensitive or portable applications.

Professional Integrated Synthesizer

SAM9703

Rev. 1710A–10/00

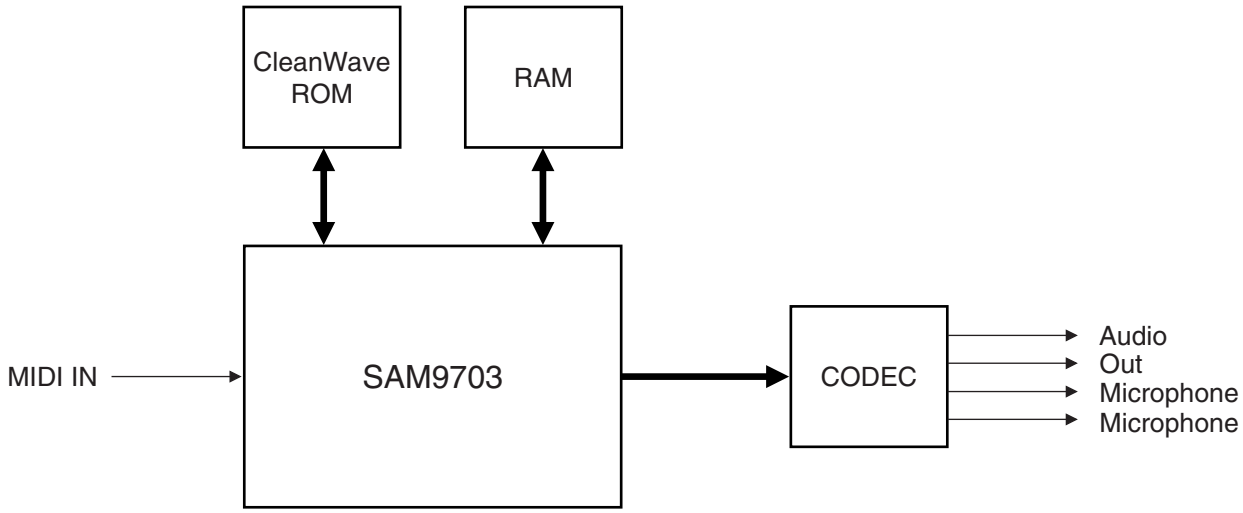
The firmware can also be modified to fit customer specifications. A SAM9703-based development/prototyping board is available and includes the SAM9703, 32 Mbits of EPROM memory, 32K words of SRAM, a codec and one DAC, providing four channels of audio out and a stereo line input (ref. 9703DVB).

The SAM9703 internal sound definition format is compatible with the SAM9407 sound studio IC. Therefore it is possible to develop specific sounds for the SAM9703 by using the development tools of the SAM9407.

The SAM9703 operates from a “low” frequency 9.6 MHz typical crystal. A built-in PLL raises this frequency to a 38.4 MHz internal clock which controls the two processors. Care has been taken that output pin signals change only when necessary. This minimizes RFI (radio frequency interferences) and power consumption. Minimizing RFI is mostly important in order to comply with standards such as FCC, CSA and CE.

The core power supply for the SAM9703 should be 3.3V ± 10%, while the periphery supports supply from 3V to 5.5V (5V ± 10% for TTL-compatible applications). Therefore, by selecting 3.3V ROM, SRAM and DAC, it is possible to develop low-power/low-voltage portable applications.

Figure 1. Typical Hardware Configuration



Pin Description

Pins by Function

Table 1. Power Supply Group

Pin Name	Pin Number	Type	Function
GND	2, 6, 8, 16, 20, 22, 26, 28, 38, 46, 49, 53, 59, 71, 75, 82, 83, 94	PWR	Digital Ground All pins should be connected to a ground plane.
VCC	1, 7, 15, 21, 27, 37, 48, 52, 58, 70, 74, 81, 95	PWR	Power Supply, 3V to 5.5V All pins should be connected to a VCC plane.
VC3	9, 19, 24, 77	PWR	Core Power Supply, 3.3V ± 10 %. All pins should be connected to +3.3V. If 3.3V is not available, then it can be derived from 5V by two 1N41418 diodes in series.

Table 2. Serial MIDI

Pin Name	Pin Number	Type	Function
MIDI IN	17	IN	Serial TTL MIDI IN. All controls are received by this pin.

Table 3. External ROM/RAM Group

Pin Name	Pin Number	Type	Function
WA0_WA24	47, 50, 51, 54 - 57, 60 - 69, 72, 73, 76, 78 - 80, 84, 85	OUT	External ROM/RAM address for up to 32M words (64 MB) of memory. ROM memory holds firmware and PCM data. RAM memory holds working variables and effect delay lines.
WD0_WD15	86 - 93, 96 -100, 3 - 5	I/O	External ROM/RAM data. Holds read data from ROM or RAM when $\overline{WOE}$ is low, write data to RAM when $\overline{WWE}$ is low.
$\overline{WCS0}$	34	OUT	External ROM chip select, active low.
$\overline{WCS1}$	35	OUT	External RAM chip select, active low.
$\overline{WOE}$	36	OUT	External ROM/RAM output enable, active low.
$\overline{WWE}$	33	OUT	External RAM write, active low
RBS	25	OUT	RAM byte select. Used as lower address from RAM when 8-bit wide RAM is connected.

Table 4. Digital Audio Group

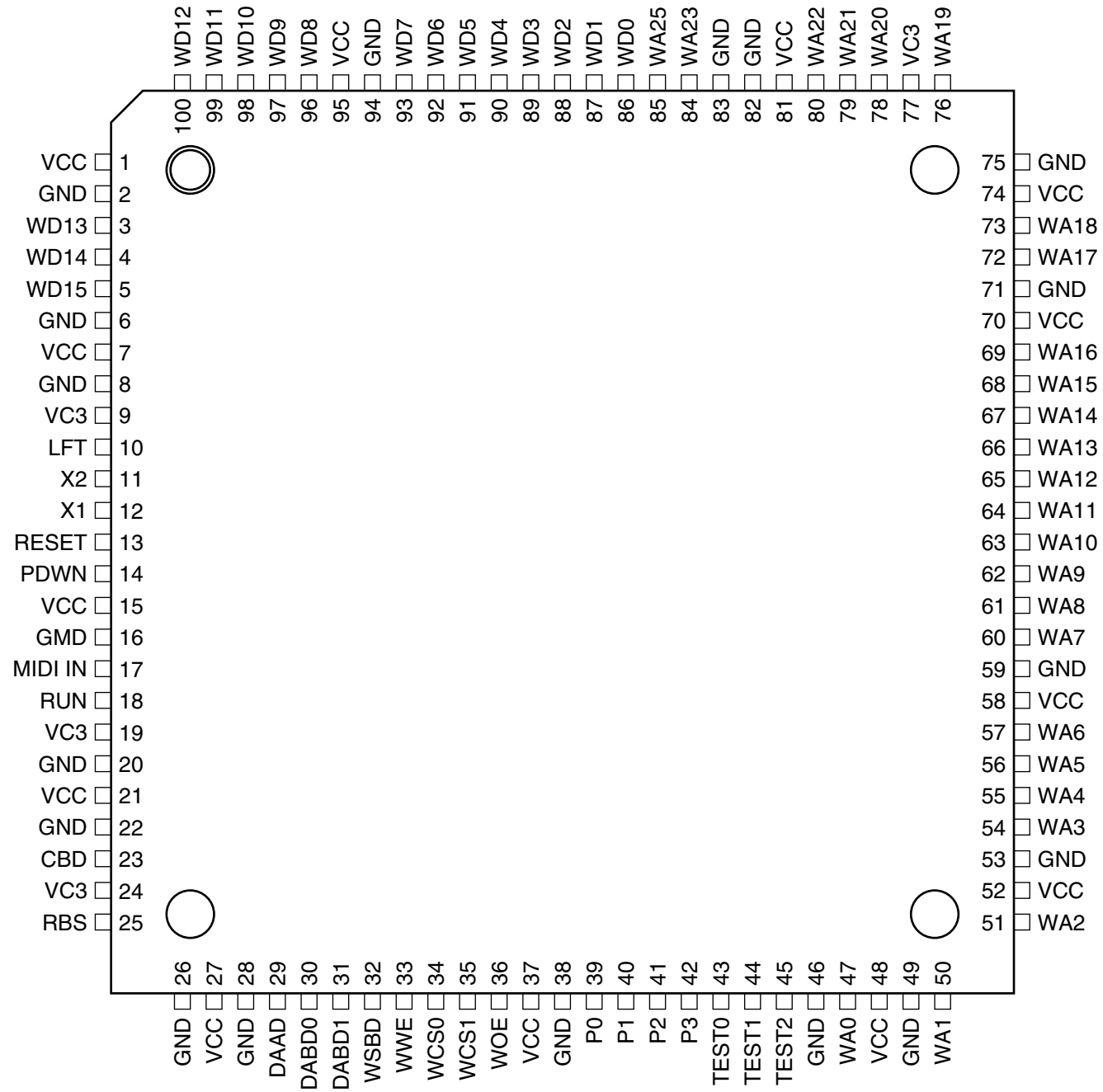
Pin Name	Pin Number	Type	Function
CLBD	23	OUT	Digital audio bit clock
WSBD	32	OUT	Digital audio left/right select
DABD0	30	OUT	Digital audio main stereo output
DABD1	31	OUT	Auxiliary digital stereo output. Reserved for surround effects.
DAAD	29	IN	Digital audio two channels input. Up to eight channels of audio can be input to the chip by using pins P1 to P3 alternate function.

Table 5. Miscellaneous Group

Pin Name	Pin Number	Type	Function
X1-X2	12, 11	–	9.6 MHz crystal connection. An external 9.6 MHz clock can also be used on X1 (3.3V input). X2 cannot be used to drive external circuits.
LFT	10	–	PLL external RC network.
$\overline{\text{RESET}}$	13	IN	Reset input, active low. This is a Schmidt trigger input, allowing direct connection of an RC network.
$\overline{\text{PDWN}}$	14	IN	Power down, active low. When power down is active, then all output pins will be floated. The crystal oscillator will be stopped. To exit from power down, $\overline{\text{PDWN}}$ should be high and $\overline{\text{RESET}}$ applied.
TEST0-TEST2	43, 44, 45	IN	Test pins. Should be grounded.
P0-P3	39, 40, 41, 42	I/O	General-purpose I/O pins. As inputs, can be used to configure the software. P1 to P3 can also be used as three additional stereo serial inputs (six audio channels).
RUN	18	OUT	When high, indicates that the synthesizer is up and running. May be used as a $\overline{\text{RESET}}$ input for an external DAC.

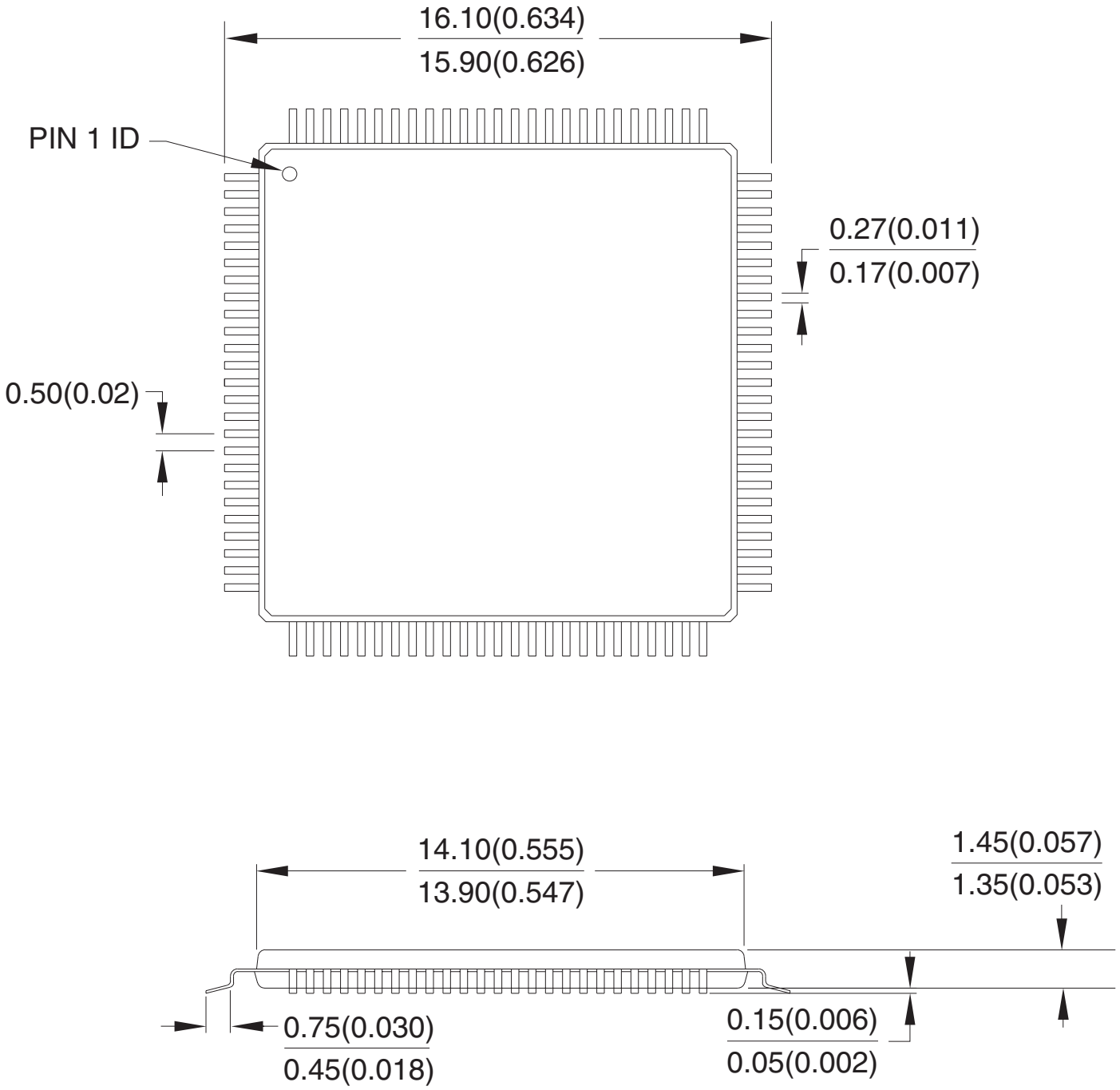
Pinout

Figure 2. SAM9703 Pinout in 100-lead TQFP Package



Mechanical Dimensions

Figure 3. 100-lead Thin Plastic Quad Flat Pack



Absolute Maximum Ratings

Table 6. Absolute Maximum Ratings

Symbol	Parameter/Condition	Min	Typ	Max	Unit
	Ambient Temperature (Power applied)	-40		+85	°C
	Storage Temperature	-6.5		+150	°C
	Voltage on any pin (except X1)	-0.5		V_{CC} + 0.5	V
	Supply Voltage	-0.5		6.5	V
V_{C3}	Supply Voltage	-0.5		4.5	V
	Maximum IOL per I/O pin			10	mA

Note: All voltages with respect to 0V, GND = 0V)

Recommended Operating Conditions

Table 7. Recommended Operating Conditions

Symbol	Parameter/Condition	Min	Typ	Max	Unit
V_{CC}	Supply Voltage[1]	3	3.3/5.0	5.5	V
V_{C3}	Supply Voltage	3	3.3	3.6	V
T_A	Operating Ambient Temperature	0		70	°C

Note: 1. When using 3.3V supply in a 5V environment, care must be taken that pin voltage does not exceed V_{CC} + 0.5V.

DC Characteristics

Table 8. DC Characteristics (T_A = 25°C, V_{C3} = 3.3V ± 10%)

Symbol	Parameter/Condition	VCC	Min	Typ	Max	Unit
V_{IL}	Low Level Input Voltage	3.3 5.0	-0.5 -0.5		1.0 1.7	V V
V_{IH}	High Level Input Voltage	3.3 5.0	2.3 3.3		VCC + 0.5 VCC + 0.5	V V
V_{OL}	Low Level Output Voltage (I_{OL} = -3.2 mA)	3.3 5.0			0.45 0.45	V V
V_{OH}	High Level Output Voltage (I_{OH} = 0.8 mA)	3.3 5.0	2.8 4.5			V V
I_{CC}	Power Supply Current (Crystal Freq. = 9.6 MHz)	3.3 5.0		70 25	90 35	mA mA
	Power Down Supply Current			70	100	µA

Timings

All timing conditions: T_A = 25°C, V_{CC} = 5V, V_C = 3.3V, all outputs exept X2 and LFT load capacitance = 30 pF, crystal frequency or external clock at X1 = 9.6 MHz.

External ROM Timing

Figure 4. ROM Read Cycle

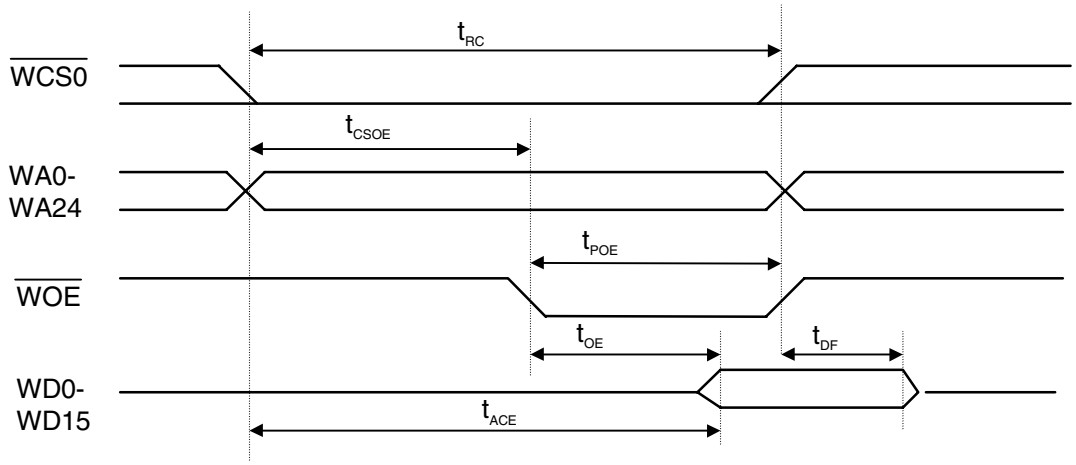


Table 9. Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_{RC}	Read Cycle Time	130			ns
t_{CSOE}	Chip Select Low/Address Valid to $\overline{WOE}$ low	45		80	ns
t_{POE}	Output Enable Pulse Width		78		ns
t_{ACE}	Chip Select/Address Access Time	125			ns
t_{OE}	Output Enable Access Time	70			ns
t_{DF}	Chip select or $\overline{WOE}$ High to Input Data High-Z	0		50	ns

External RAM Timing

Figure 5. 16-bit SRAM Read Cycle

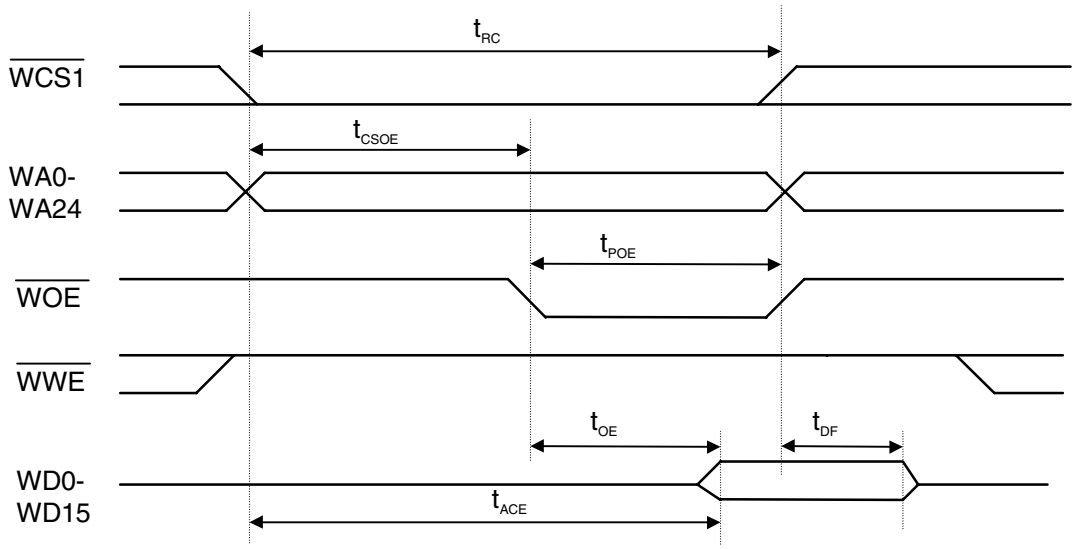


Figure 6. 16-bit SRAM Write Cycle

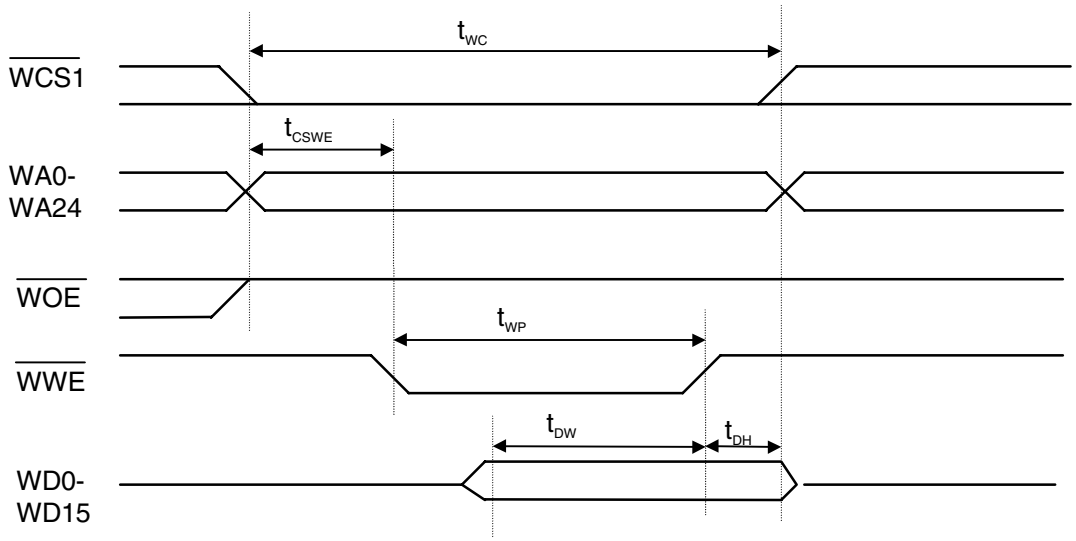


Table 10. Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_{RC}	Read Cycle Time	130			ns
t_{CSOE}	Chip Select Low/Address Valid to $\overline{WOE}$ Low	45		80	ns
t_{POE}	Output Enable Pulse Width		78		ns
t_{ACE}	Chip Select/Address Access Time	125			ns
t_{OE}	Output Enable Access Time	70			ns

Table 10. Timing Parameters (Continued)

Symbol	Parameter	Min	Typ	Max	Unit
t_{DF}	Chip Select or $\overline{WOE}$ High to Input Data High-Z	0		50	ns
t_{WC}	Write Cycle Time	130			ns
t_{CSWE}	Write enable Low from $\overline{CS}$ or Address or $\overline{WOE}$	40			ns
t_{WP}	Write Pulse Width		104		ns
t_{DW}	Data Out Setup Time	95			ns
t_{DH}	Data Out Hold Time	10			ns

Figure 7. 8-bit SRAM Read Cycle

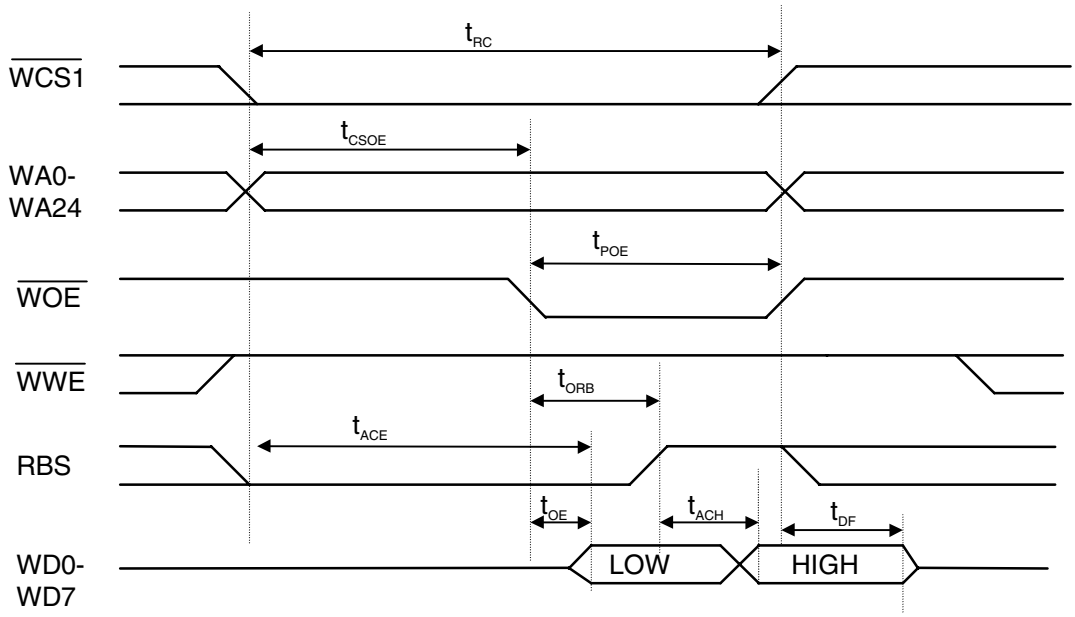


Figure 8. 8-bit SRAM Write Cycle

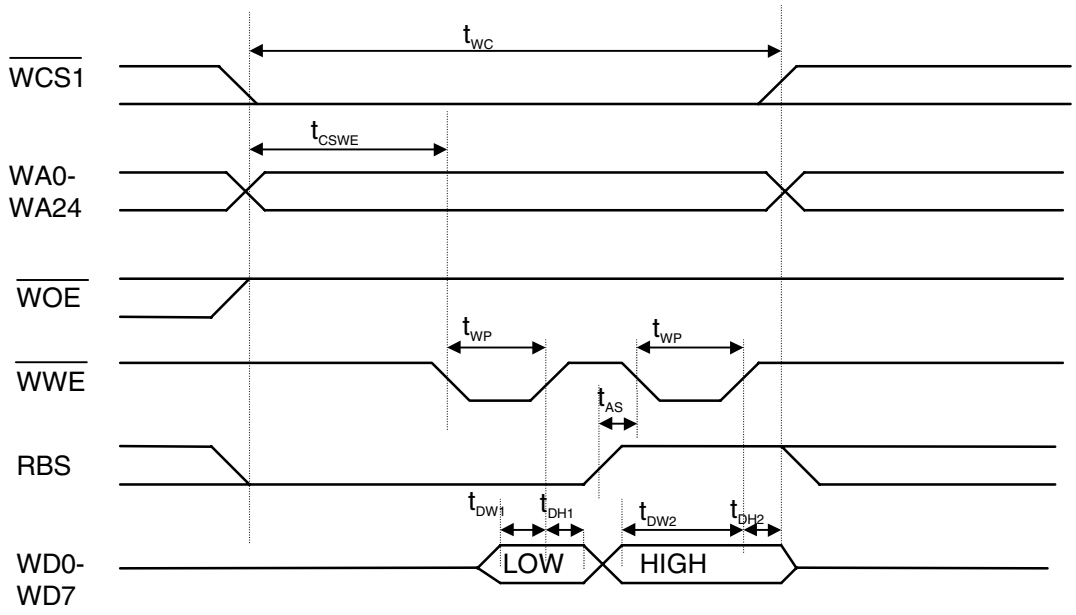


Table 11. Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_{RC}	Word Read Cycle Time	130			ns
t_{CSOE}	Chip Select Low/Address Valid to $\overline{WOE}$ Low	45		80	ns
t_{POE}	Output Enable Pulse Width		78		ns
t_{ACE}	Chip Select/Address Low Byte Access Time	70			ns
t_{OE}	Output Enable Low Byte Access Time	20			ns
t_{ORB}	Output Enable Low Byte Select High		26		ns
t_{ACH}	Byte Select High Byte access Time	45			ns
t_{DF}	Chip select or $\overline{WOE}$ High to Input High-Z	0		50	ns
t_{WC}	Word Write Cycle Time	130			ns
t_{CSWE}	1st $\overline{WWE}$ Low from $\overline{CS}$ or Address or $\overline{WOE}$	40			ns
t_{WP}	Write (Low and High Byte) Pulse Width	20			ns
t_{DW1}	Data Out Low Byte Setup Time	25			ns
t_{DH1}	Data Out Low Byte Hold Time	20			ns
t_{AS}	RBS High to Second Write Pulse	8			ns
t_{DW}	Data Out High Byte Setup Time	40			ns
t_{DH2}	Data Out High Byte Hold Time	10			ns

Digital Audio

Figure 9. Digital Audio Timing

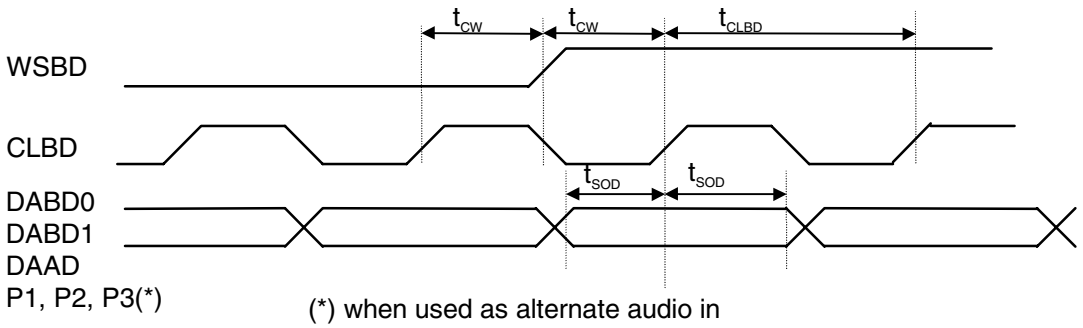
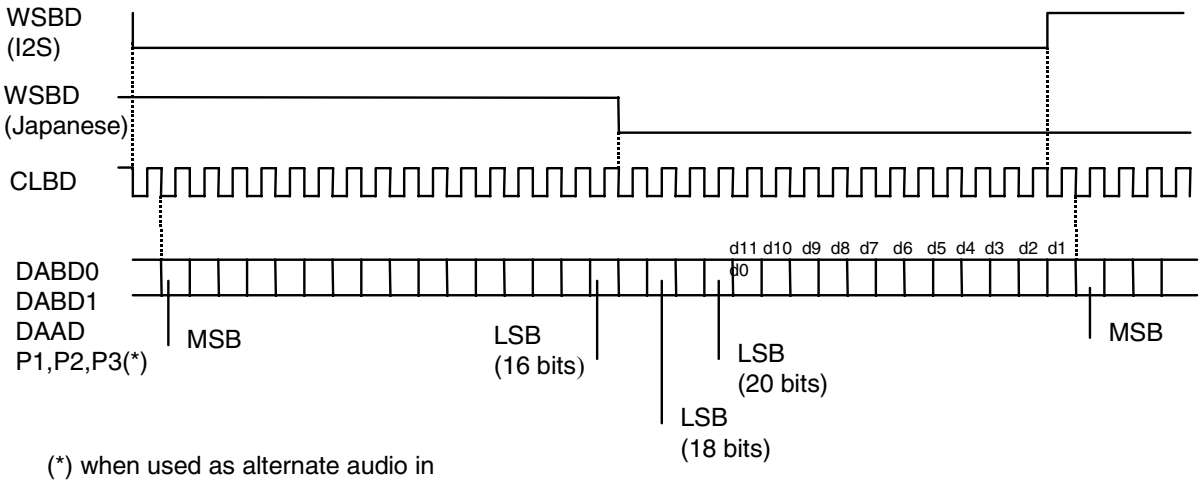


Table 12. Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_{CW}	CLBD Rising to WSBD Change	200			ns
t_{SOD}	DABD Valid Prior/After CLBD Rising	200			ns
t_{CLBD}	CLBD Cycle Time		416.67		ns

Digital Audio Frame

Figure 10. Digital Audio Frame Format



Notes: 1. Selection between I2S and Japanese format is a firmware option.

2. DAAD, P1, P2, P3 are 16 bits only.

3. When connected to codecs such as CS4216 or CS4218, D0 - D11 can be used to hold independent auxiliary information on left and right words. Refer to the corresponding codec data sheets for details. Auxiliary information is available on DABD0 and DAAD.

Reset and Power-down

During power-up, the $\overline{\text{RESET}}$ input should be held low until the crystal oscillator and PLL are stabilized, which can take about 20 ms. A typical RC/diode power-up network can be used.

After the low-to-high transition of $\overline{\text{RESET}}$, the following occurs:

- The synthesis enters an idle state.
- The RUN output is set to zero.
- Firmware execution starts from address 0100H in ROM space ($\overline{\text{WCS0}}$ low).

If $\overline{\text{PDWN}}$ is asserted low, then all I/Os and outputs will be floated and the crystal oscillator and PLL will be stopped. The chip enters a deep power-down sleep mode. To exit power-down, $\overline{\text{PDWN}}$ has to be asserted high, then $\overline{\text{RESET}}$ applied.

Recommended Board Layout

As for all HCMOS high-integration ICs, some rules of board layout should be followed for reliable operation:

- GND, V_{CC}, V_{C3} distribution, decouplings

All GND, V_{CC}, V_{C3} pins should be connected. GND + V_{CC} planes are strongly recommended below the SAM9703. The board GND + V_{CC} distribution should be in grid form. For 5V V_{CC} operation, if 3.3V is not available, then V_{C3} can be connected to V_{CC} by two 1N4148 diodes in serial. This guarantees a minimum voltage drop of 1.2V.

Recommended V_{CC} decoupling is 0.1 µF at each corner of the IC with an additional 10 µF decoupling close to the crystal. V_{C3} requires a single 0.1 µF decoupling close to the IC.

- Crystal, LFT

The paths between the crystal, the crystal compensation capacitors, the LFT filter R-C-R and the SAM9703 should be short and shielded. The ground return from the compensation capacitors and LFT filter should be the GND plane from SAM9703.

- Analog Section

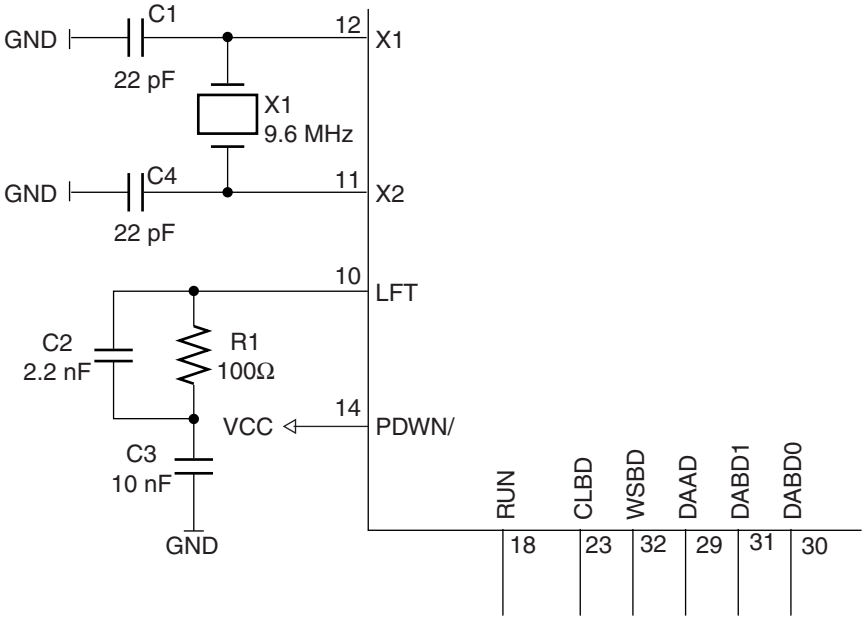
A specific AGND ground plane should be provided, which connects by a single trace to the GND ground. No digital signals should cross the AGND plane. Refer to the codec vendor recommended layout for correct implementation of the analog section.

- Unused Inputs

Unused inputs should always be connected. A floating input can cause internal oscillation inside the IC, which can destroy the device by dramatically increasing the power consumption. If the power-down feature is to be used, care should be taken that no pin is left floating during power down. Usually, a 1 MΩ ground return is sufficient.

Recommended Crystal Compensation and LFT Filter

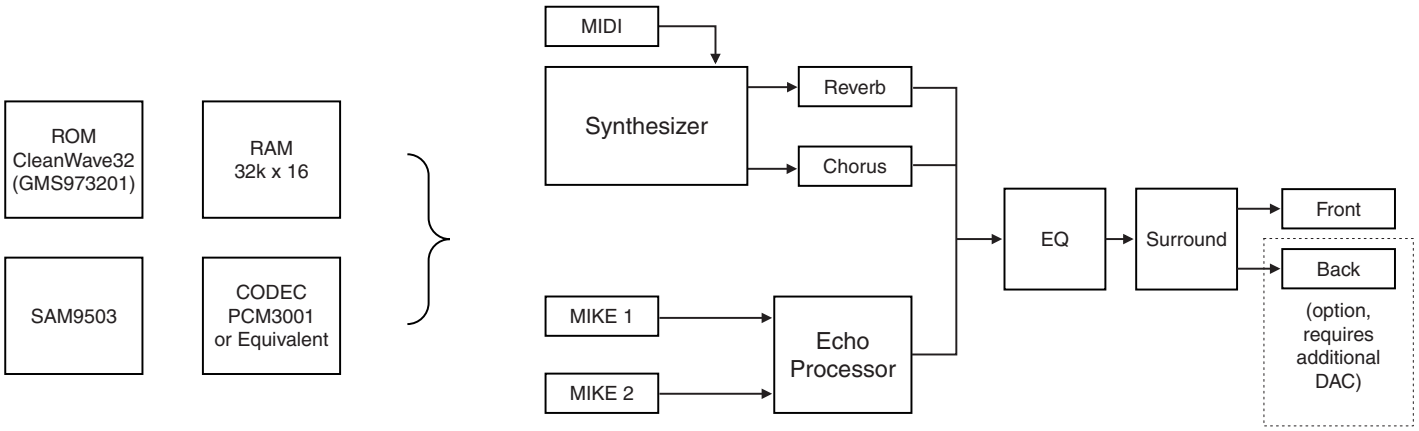
Figure 11. Crystal Compensation and LFT Filter



Note: The X2 output cannot be used to drive another circuit.

CleanWave32™ ROM Firmware (Ref. GMS973201)

- **ROM includes Firmware and PCM Data**
- **Full GM implementation with Top-quality Additional Sounds**
  - **128 General MIDI Sounds**
  - **189 Variation Sounds including Sound Effects**
  - **9 Drum Sets + 1 SFX Set**
- **Powerful MIDI implementation**
- **Built-in Compatible Reverb and Chorus**
- **Built-in Four-band Parametric Equalizer, Fully Controllable by MIDI**
- **Built-in Spatializer Effect with MIDI Control**
- **Microphone Echo Processing**



For detailed information about sound list and MIDI implementation, please request the CleanWave32 user's manual.

Reference Design: 9703DVB

SAM9703 + 2 x 16-Mbit EPROMs + 2 x 32k x 8 SRAMs + Codec + DAC

9703DVB can be used for CleanWave32 evaluation or other specific applications requiring not more than 4 Mb of PCM data.

Atmel Headquarters

Corporate Headquarters
2325 Orchard Parkway
San Jose, CA 95131
TEL (408) 441-0311
FAX (408) 487-2600

Europe
Atmel SarL
Route des Arsenaux 41
Casa Postale 80
CH-1705 Fribourg
Switzerland
TEL (41) 26-426-5555
FAX (41) 26-426-5500

Asia
Atmel Asia, Ltd.
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan
Atmel Japan K.K.
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Atmel Colorado Springs
1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL (719) 576-3300
FAX (719) 540-1759

Atmel Rousset
Zone Industrielle
13106 Rousset Cedex
France
TEL (33) 4-4253-6000
FAX (33) 4-4253-6001

Atmel Smart Card ICs
Scottish Enterprise Technology Park
East Kilbride, Scotland G75 0QR
TEL (44) 1355-803-000
FAX (44) 1355-242-743

Atmel Grenoble
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex
France
TEL (33) 4-7658-3243
FAX (33) 4-7658-3320

Fax-on-Demand
North America:
1-(800) 292-8635
International:
1-(408) 441-0732

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

BBS
1-(408) 436-4309

1710A–10/00/0M