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### PS21255-E



#### INTEGRATED POWER FUNCTIONS

4th generation (planar) IGBT inverter bridge for 3 phase DC-to-AC power conversion.

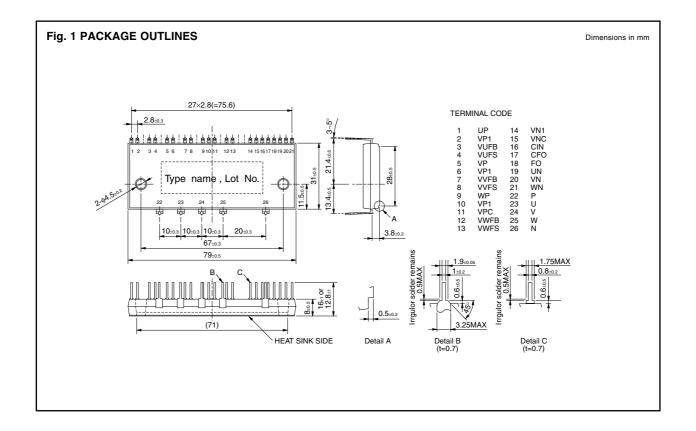
### INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

- For upper-leg IGBTs: Drive circuit, High voltage isolated high-speed level shifting, Control circuit under-voltage (UV) protection.

  Note: Bootstrap supply scheme can be applied.
- For lower-leg IGBTs: Drive circuit, Control circuit under-voltage protection (UV), Short circuit protection (SC).
- Fault signaling: Corresponding to a SC fault (Low-side IGBT) or a UV fault (Low-side supply).
- Input interface: 5V line CMOS/TTL compatible, Schmitt Trigger receiver circuit.

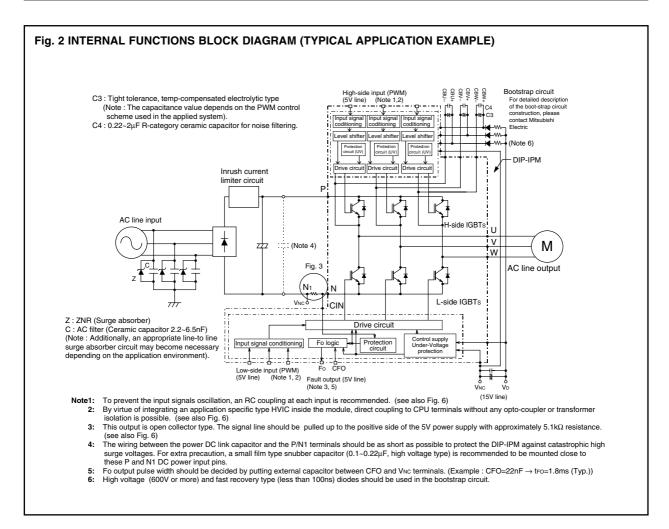
# **APPLICATION**

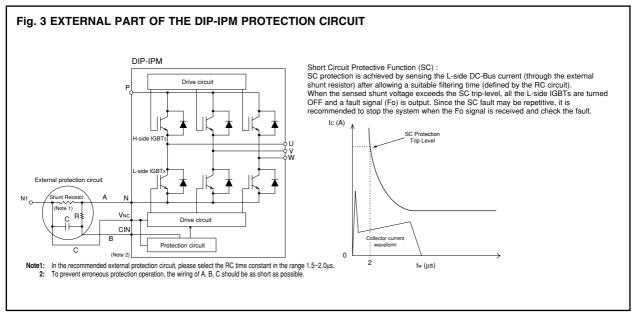
AC100V~200V three-phase inverter drive for small power motor control.





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# **MAXIMUM RATINGS** (Tj = $25^{\circ}$ C, unless otherwise noted)

### **INVERTER PART**

Symbol	Parameter	Condition	Ratings	Unit
Vcc	Supply voltage	Applied between P-N	450	V
VCC(surge)	Supply voltage (surge)	Applied between P-N	500	V
VCES	Collector-emitter voltage		600	V
±lc	Each IGBT collector current	Tc = 25°C	20	Α
±ICP	Each IGBT collector current (peak)	Tc = 25°C, instantaneous value (pulse)	40	Α
Pc	Collector dissipation	Tc = 25°C, per 1 chip	56	W
Tj	Junction temperature	(Note 1)	-20~+150	°C

Note 1 : The maximum junction temperature rating of the power chips integrated within the DIP-IPM is  $150^{\circ}$ C (@ Tc  $\leq 100^{\circ}$ C) however, to ensure safe operation of the DIP-IPM, the average junction temperature should be limited to Tj(ave)  $\leq 125^{\circ}$ C (@ Tc  $\leq 100^{\circ}$ C).

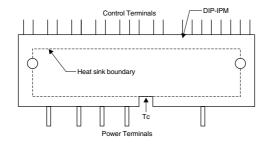
# **CONTROL (PROTECTION) PART**

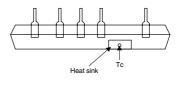
Symbol	Parameter	Condition	Ratings	Unit
VD	Control supply voltage	Applied between VP1-VPC, VN1-VNC	20	V
VDB	Control supply voltage	Applied between Vufb-Vufs, Vvfb-Vvfs, Vwfb-Vwfs	20	٧
VCIN	Input voltage	Applied between UP, VP, WP-VPC, UN, VN, WN-VNC	-0.5~+5.5	٧
VFO	Fault output supply voltage	Applied between Fo-VNC	-0.5~VD+0.5	V
IFO	Fault output current	Sink current at Fo terminal	15	mA
Vsc	Current sensing input voltage	Applied between CIN-VNC	-0.5~VD+0.5	V

### **TOTAL SYSTEM**

Symbol	Parameter	Condition	Ratings	Unit
VCC(PROT)	Self protection supply voltage limit (short circuit protection capability)	$VD = 13.5 \sim 16.5 V$ , Inverter part $T_j = 125 °C$ , non-repetitive, less than 2 μs	400	V
Tc	Module case operation temperature	(Note 2)	<b>−20~+100</b>	°C
Tstg	Storage temperature		<b>−</b> 40~+125	°C
Viso	Isolation voltage	60Hz, Sinusoidal, AC 1 minute, connection pins to heat-sink plate	1500	Vrms

### Note 2:Tc MEASUREMENT POINT







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### THERMAL RESISTANCE

Symbol Parameter	Dawara atau	O and distant	Limits			Unit
	Condition		Тур.	Max.		
Rth(j-c)Q	Junction to case thermal	Inverter IGBT part (per 1/6 module)	_	_	2.2	°C/W
Rth(j-c)F	resistance	Inverter FWD part (per 1/6 module)	_	_	4.5	°C/W
Rth(c-f)	Contact thermal resistance	Case to fin, (per 1 module) thermal grease applied	_	_	0.067	°C/W

# **ELECTRICAL CHARACTERISTICS** ( $T_j = 25^{\circ}C$ , unless otherwise noted)

### **INVERTER PART**

0	Dt	Dovernmentory Constitutes		Limits			Unit
Symbol	Parameter		Condition		Тур.	Max.	Unit
VCE(sat)	Collector-emitter saturation	VD = VDB = 15V	IC = 20A, Tj = 25°C	_	1.80	2.45	V
	voltage	VCIN = 0V	Ic = 20A, Tj = 125°C	_	1.90	2.60	\ \ \
VEC	FWD forward voltage	Tj = 25°C, -IC = 20A, VCIN = 5V		_	2.20	3.00	V
ton				0.10	0.80	1.30	μs
trr		$\begin{tabular}{ll} VCC = 300V, VD = VDB = 15V \\ IC = 20A, T_j = 125^{\circ}C, VCIN = 5V \leftrightarrow 0V \\ \end{tabular}$		_	0.10	_	μs
tc(on)	Switching times			_	0.50	0.90	μs
toff		Inductive load (upper-lov	Inductive load (upper-lower arm)		0.80	1.90	μs
tc(off)				_	0.40	1.30	μs
ICES	Collector-emitter cut-off	VCE = VCES	Tj = 25°C	_	_	1	mA
	current	VCE = VCES	Tj = 125°C	_	_	10	111/

# **CONTROL (PROTECTION) PART**

0	Danamatan		O and distant		Limits		
Symbol	Parameter	Condition		Min.	Тур.	Max.	Unit
VD	Control supply voltage	Applied between	/P1-VPC, VN1-VNC	13.5	15.0	16.5	V
VDB	Control supply voltage	Applied between	/UFB-VUFS, VVFB-VVFS, VWFB-VWFS	13.5	15.0	16.5	V
lp	Circuit current	VD = VDB = 15V,	Total of VP1-VPC, VN1-VNC	_	_	8.50	mA
וט	Circuit current	VCIN= 5V	VUFB-VUFS, VVFB-VVFS, VWFB-VWFS	_	_	1.00	IIIA
VFOH		Vsc = 0V, Fo = 10	)kΩ 5V pull-up	4.9	_	_	V
VFOL	Fault output voltage	Vsc = 1V, Fo = 10	Vsc = 1V, Fo = $10k\Omega$ 5V pull-up		— 0.8	1.2	V
VFOsat	1	Vsc = 1V, IFO = 1	VSC = 1V, IFO = 15mA		1.2	1.8	V
tdead	Arm shoot-through blocking time	Relates to corresponding input signal for blocking arm shoot-through. $-20^{\circ}\text{C} \le \text{Tc} \le 100^{\circ}\text{C}$		2.5	_	_	μs
VSC(ref)	Short circuit trip level	$T_j = 25^{\circ}C, V_D = 15V$ (Note 3)		0.45	0.5	0.55	V
UVDBt			Trip level	10.0	_	12.0	V
UVDBr	Supply circuit under-voltage	T <sub>i</sub> ≤ 125°C	Reset level	10.5	_	12.5	V
UVDt	protection	1] \( \) 125 C	Trip level	10.3	_	12.5	V
UVDr	1		Reset level	10.8	_	13.0	V
tFO	Fault output pulse width	CFO = 22nF (Note 4)		1.0	1.8	_	ms
Vth(on)	ON threshold voltage	Applied between	UP, VP, WP-VPC, UN, VN, WN-VNC	0.8	1.4	2.0	V
Vth(off)	OFF threshold voltage	Applied between .	OF, VF, VVF-VFC, ON, VN, VVN-VNC	2.5	3.0	4.0	V

Note 3: Short circuit protection is functioning only at the low-arms. Please select the value of the external shunt resistor such that the SC trip-level is less than 34 A.



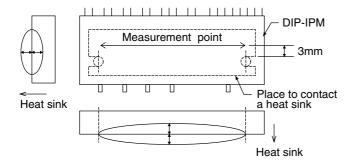
<sup>4:</sup> Fault signal is output when the low-arms short circuit or control supply under-voltage protective functions operate. The fault output pulsewidth tFO depends on the capacitance value of CFO according to the following approximate equation: CFO = 12.2 × 10<sup>-6</sup> × tFO [F].

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# **MECHANICAL CHARACTERISTICS AND RATINGS**

Parameter	Condition		Limits			Unit
Parameter	Condition		Min.	Тур.	Max.	Offit
Mounting torque	Mounting screw : M4	_	0.98	1.18	1.47	N⋅m
Terminal pulling strength	Weight 19.6N	EIAJ-ED-4701	10	_	_	S
Bending strength	Weight 9.8N. 90deg bend	EIAJ-ED-4701	2		_	times
Weight		_		54	_	g
Heat-sink flatness	(Note 5)	_	-50		100	μm

### Note 5: Measurement point of heat-sink flatness



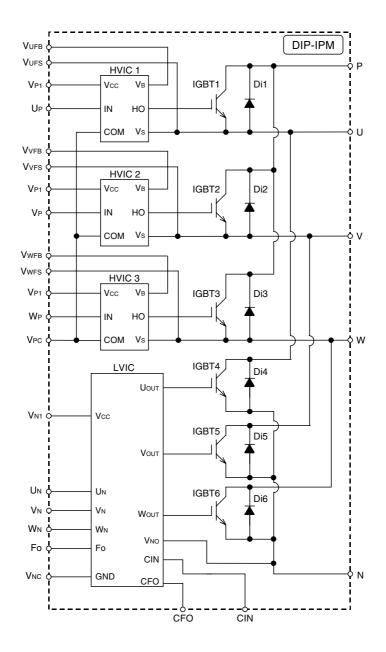
### RECOMMENDED OPERATION CONDITIONS

Symbol	Davamatar Condition		Limits			Unit
	Parameter	Condition	Min.	Тур.	Max.	Offit
Vcc	Supply voltage	Applied between P-N	0	300	400	V
<b>V</b> D	Control supply voltage	Applied between VP1-VPC, VN1-VNC	13.5	15.0	16.5	V
VDB	Control supply voltage	Applied between Vufb-Vufs, Vvfb-Vvfs, Vwfb-Vwfs	13.5	15.0	16.5	V
$\Delta V$ D, $\Delta V$ DB	Control supply variation		-1	_	1	V/μs
tdead	Arm shoot-through blocking time	Relates to corresponding input signal for blocking arm shoot-through	2.5	_	_	μs
fPWM	PWM input frequency	Tc ≤ 100°C, Tj ≤ 125°C	_	15	-	kHz
VCIN(ON)	Input ON threshold voltage	Applied between UP, VP, WP-VPC 0~0.65			V	
VCIN(OFF)	Input OFF threshold voltage	Applied between Un, Vn, Wn-Vnc 4.0~5.5			V	



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Fig. 4 THE DIP-IPM INTERNAL CIRCUIT





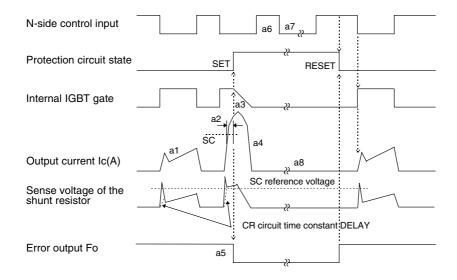
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### Fig. 5 TIMING CHARTS OF THE DIP-IPM PROTECTIVE FUNCTIONS

### [A] Short-Circuit Protection (N-side only)

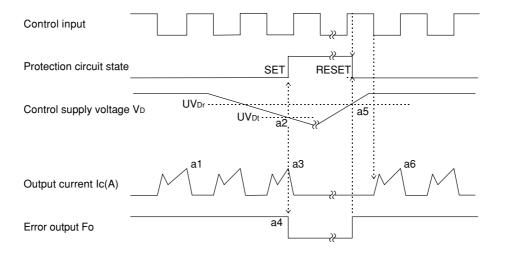
(For the external shunt resistor and CR connection.)

- a1. Normal operation: IGBT ON and carrying current.
- a2. Short circuit current detection (SC trigger).
- a3. Hard IGBT gate interrupt.
- a4. IGBT turns OFF.
- a5. Fo timer operation starts: The pulse width of the Fo signal is set by the external capacitor CFo.
- a6. Input "H": IGBT OFF state.
- a7. Input "L" : IGBT ON state.
- a8. IGBT OFF state.



# [B] Under-Voltage Protection (N-side, UVD)

- a1. Normal operation: IGBT ON and carrying current.
- a2. Under voltage trip (UVDt).a3. IGBT OFF in spite of control input condition.
- a4. Fo timer operation starts.
- a5. Under voltage reset (UVDr)
- a6. Normal operation: IGBT ON and carrying current.





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### [C] Under-Voltage Protection (P-side, UVDB)

- a1. Control supply voltage rises: After the voltage level reachs UVDBr, the circuits start to operate when the next input is applied. a2. Normal operation: IGBT ON and carrying current. a3. Under voltage trip (UVDBt).

- a4. IGBT OFF in spite of control input condition, but there is no Fo signal output.
- a5. Under-voltage reset (UVDBr).
- a6. Normal operation: IGBT ON and carrying current.

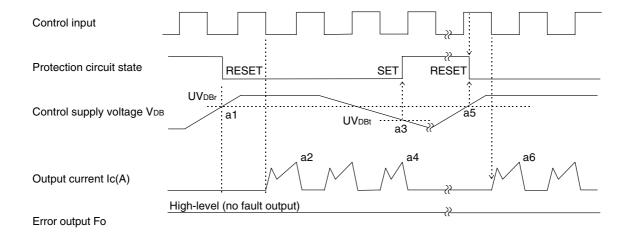
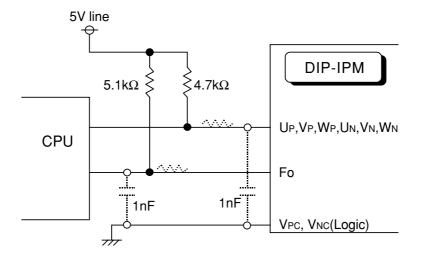


Fig. 6 RECOMMENDED CPU I/O INTERFACE CIRCUIT



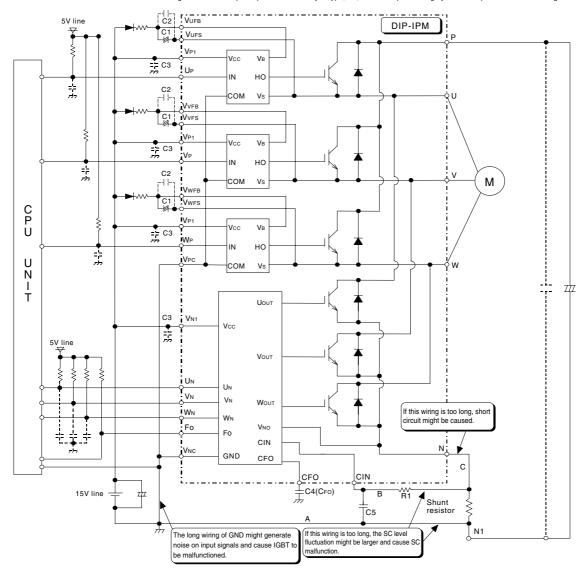
Note: RC coupling at each input (parts shown dotted) may change depending on the PWM control scheme used in the application and on the wiring impedances of the application's printed circuit board.



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### Fig. 7 TYPICAL DIP-IPM APPLICATION CIRCUIT EXAMPLE

C1: Tight tolerance temp-compensated electrolytic type; C2,C3: 0.22~2  $\mu$  F R-category ceramic capacitor for noise filtering



- Note 1: To prevent the input signals oscillation, an RC coupling at each input is recommended, and the wiring of each input should be as short as possible. (Less than 2cm)
  - 2: By virtue of integrating an application specific type HVIC inside the module, direct coupling to CPU terminals without any opto-coupler or transformer isolation is possible.
  - 3: Fo output is open collector type. This signal line should be pulled up to the positive side of the 5V power supply with approximately 5 1kO resistance
  - 4: FO output pulse width should be decided by connecting an external capacitor between CFO and VNc terminals (CFo). (Example: CFO
  - = 22 nF  $\rightarrow$  tFO = 1.8 ms (typ.)) 5: Each input signal line should be pulled up to the 5V power supply with approximately 4.7k $\Omega$  resistance (other RC coupling circuits at each input may be needed depending on the PWM control scheme used and on the wiring impedances of the system's printed circuit board). Approximately a 0.22~2µF by-pass capacitor should be used across each power supply connection terminals.
  - 6: To prevent errors of the protection function, the wiring of A, B, C should be as short as possible.
  - 7: In the recommended protection circuit, please select the R1C5 time constant in the range  $1.5 \sim 2 \mu s$ .
  - 8: Each capacitor should be put as nearby the pins of the DIP-IPM as possible.
  - 9: To prevent surge destruction, the wiring between the smoothing capacitor and the P&N1 pins should be as short as possible. Approximately a  $0.1 \sim 0.22 \mu F$  snubber capacitor between the P&N1 pins is recommended.

