MT90401

SONET/SDH System Synchronizer

Data Sheet

Features

- Meets requirements of GR-253-CORE for SONET Stratum 3 and SONET minimum clock
- Meets requirements of GR-1244-CORE Stratum 3
- Meets requirements of G.813 Option 1 and Option 2 for SDH Equipment Clocks (SEC) with external jitter attenuator
- Provides OC-3/STM-1, DS3, E3, 19.44MHz, DS2, E1, T1, 8kHz and ST-BUS clock outputs
- Accepts reference inputs from two independent sources
- Selectable 1.544MHz, 2.048MHz, 19.44MHz or 8kHz input reference frequencies
- Holdover accuracy of 0.02 ppm
- Adjustable output clock phase supporting master-slave arrangements
- Hardware or microprocessor control (8 bit microprocessor interface)
- 3.3V supply
- JTAG boundary scan

Applications

- SONET/SDH Add/Drop multiplexers
- SONET/SDH uplinks
- Integrated access devices
- ATM edge switches

Ordering Information

MT90401AB   80 Pin LQFP

-40 to +85°C

Description

The MT90401 is a digital phase locked loop (DPLL) that is designed to synchronize SDH (Synchronous Digital Hierarchy) and SONET (Synchronous Optical Network) networking equipment. The MT90401 is used to ensure that the timing of outgoing signals remains within the limits specified by Telcordia, ANSI and the ITU during normal operation and in the presence of disturbances on the incoming synchronization signals.

The MT90401 can operate in free-run, locked or holdover mode. The loop filter corner frequency can be selected to suit SONET applications or to suit SDH applications. The MT90401 uses an external 20MHz oscillator as its master clock and it does not require external loop filter components.

In Hardware Mode, the MT90401 can be controlled and monitored via external pins. In Microport Mode, a microprocessor can be used for more comprehensive control and monitoring.
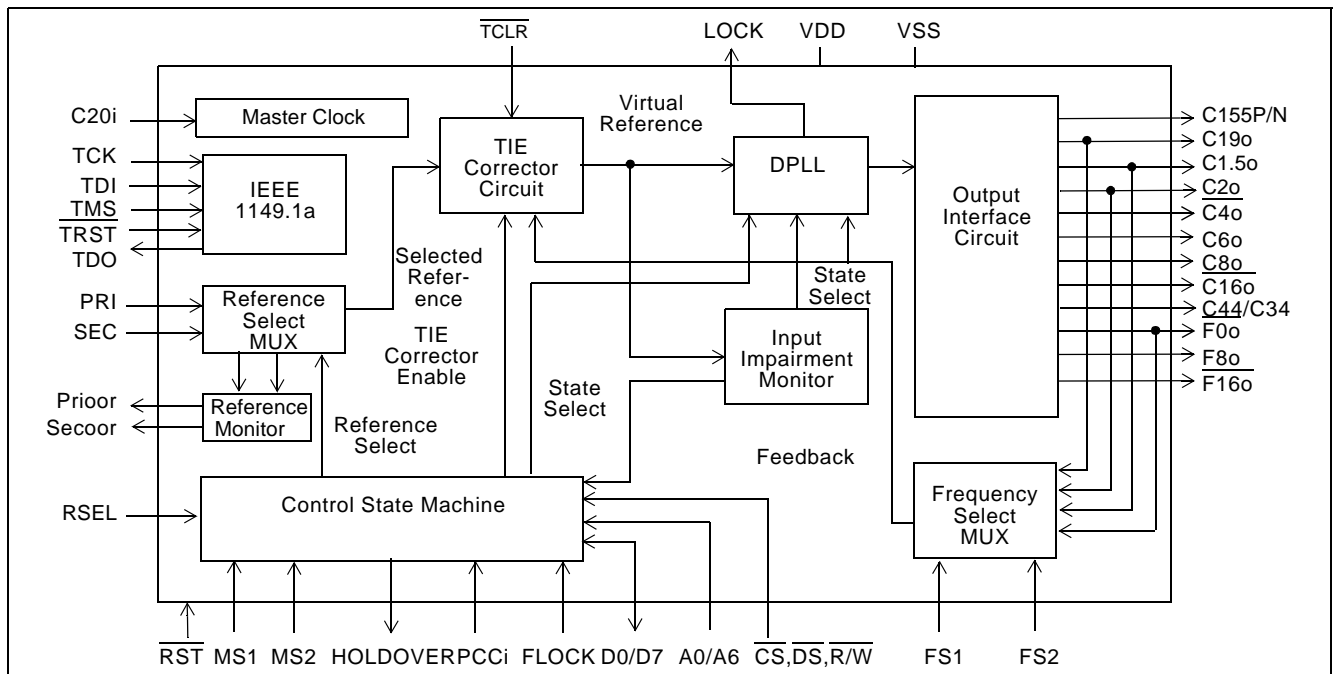

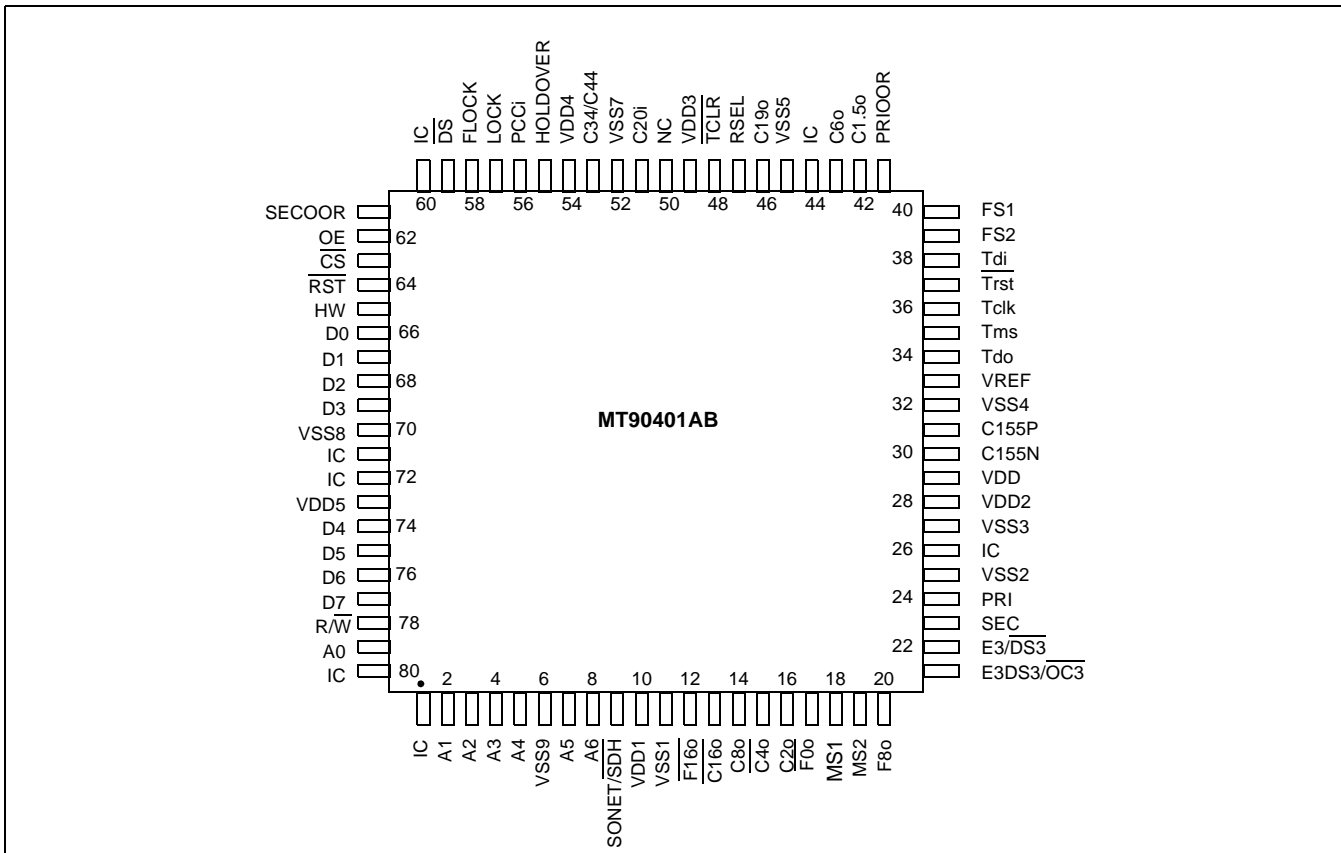**Figure 1 - Functional Block Diagram**

Figure pin labels (80 Pin LQFP MT90401AB):

Top: IC, DS, FLOCK, LOCK, PCCi, HOLDOVER, VDD4, C34/C44, VSS7, C20i, NC, VDD3, TCLR, RSEL, C19o, VSS5, IC, C6o, C1.5o, PRIOOR

Left: SECOOR, OE, CS, RST, HW, D0, D1, D2, D3, VSS8, IC, IC, VDD5, D4, D5, D6, D7, R/W, A0, IC

Right: FS1, FS2, Tdi, Trst, Tclk, Tms, Tdo, VREF, VSS4, C155P, C155N, VDD, VDD2, VSS3, IC, VSS2, PRI, SEC, E3/DS3, E3DS3/OC3

Bottom: IC, A1, A2, A3, A4, VSS9, A5, A6, SONET/SDH, VDD1, VSS1, F16o, C16o, C8o, C4o, C2o, F0o, MS1, MS2, F8o

Figure 2 - Pin Connections 80 Pin LQFP for MT90401

Pin Description

Pin #	Name	Description
1	IC	**Internal Connection**. Leave unconnected.
2-5	A1 - A4	**Address 1 to 4 (5V tolerant Inputs).** Address inputs for the parallel processor interface.
6	V_{SS9}	**Digital ground.** 0 Volts
7, 8	A5, A6	**Address 5, to 6 (5V tolerant Input).** Address inputs for the parallel processor interface.
9	SONET/ SDH	**SONET/SDH (Input).** In hardware mode set this pin high to have a loop filter corner frequency of 70 millihertz and limit the phase slope to 885 ns per second. Set this pin low to have a corner frequency of approximately 1.1 hertz and limit the phase slope to 53 ns per 1.326 ms. This pin performs no function if the device is not in hardware mode.
10	V_{DD1}	**Positive Power Supply.** Digital supply.
11	V_{SS1}	**Digital ground.** 0 Volts
12	F16o	**Frame Pulse ST-BUS 8.192 Mb/s (CMOS Output).** This is an 8kHz 61ns active low framing pulse, which marks the beginning of an ST-BUS frame. This is typically used for ST-BUS operation at 8.192 Mb/s.
13	C16o	**Clock 16.384MHz (CMOS Output).** This output is used for ST-BUS operation with a 16.384MHz clock.
14	C8o	**Clock 8.192MHz (CMOS Output).** This output is used for ST-BUS operation at 8.192Mb/s.
15	C4o	**Clock 4.096MHz (CMOS Output).** This output is used for ST-BUS operation at 2.048Mb/s and 4.096Mb/s.

Pin Description (continued)

Pin #	Name	Description
16	C2o	**Clock 2.048MHz (CMOS Output).** This output is used for ST-BUS operation at 2.048Mb/s.
17	F0o	**Frame Pulse ST-BUS 2.048Mb/s (CMOS Output).** This is an 8kHz 244ns active low framing pulse, which marks the beginning of an ST-BUS frame. This is typically used for ST-BUS operation at 2.048Mb/s and 4.096Mb/s.
18	MS1	**Mode/Control Select 1 (Input).** This input, together with MS2, determines the state (Normal, Holdover, or Freerun) of operation. See Table 3 on page 10. The logic level at this input is gated in by the rising edge of F8o. This pin performs no function if the device is not in hardware mode.
19	MS2	**Mode/Control Select 2 (Input).** This input, together with MS1, determines the state (Normal, Holdover or Freerun) of operation. See Table 3 on page 10. The logic level at this input is gated in by the rising edge of F8o. This pin performs no function if the device is not in hardware mode.
20	F8o	**Frame Pulse Generic (CMOS Output).** This is an 8kHz 122ns active high framing pulse, which marks the beginning of a TDM frame. This is typically used for TDM streams operating at 8.192 Mb/s.
21	E3DS3/OC3	**E3DS3 or OC-3 Selection (Input).** In Hardware Mode a low on this pin enables the differential 155.52MHz output clock on the C155N/C155P pins; this will also cause the C34/C44 pin to output its nominal clock frequency divided by 4. In Hardware Mode, a high on this pin disables the differential 155.52MHz output clock on the C155N/C155P pins; this will also cause the C34/C44 pin to output its nominal clock frequency. This pin performs no function if the device is not in Hardware Mode.
22	E3/DS3	**E3 or DS3 Selection (Input).** In Hardware Mode a low on this pin selects a clock rate of 44.736MHz for the C34/C44 pin, while a high selects a clock rate of 34.368MHz. This pin performs no function if the device is not in hardware mode.
23	SEC	**Secondary Reference (Input).** This is one of two (PRI & SEC) input reference sources (falling edge) used for synchronization. One of four possible frequencies (8kHz, 1.544MHz, 2.048MHz or 19.44MHz) may be used. In hardware mode the selection of the input reference is based upon the MS1, MS2 and RSEL control inputs.
24	PRI	**Primary Reference (Input).** This is one of two (PRI & SEC) input reference sources (falling edge) used for synchronization. One of four possible frequencies (8kHz, 1.544MHz, 2.048MHz or 19.44MHz) may be used. In hardware mode the selection of the input reference is based upon the MS1, MS2 and RSEL control inputs.
25	V$_{SS2}$	**Digital ground.** 0 Volts
26	IC	**Internal Connection.** Leave unconnected
27	V$_{SS3}$	**Analog ground.** 0 Volts
28	V$_{DD2}$	**Positive Analog Power Supply.** Analog supply.
29	V$_{DD}$	**Positive Power Supply.** Digital supply.
30 31	C155N, C155P	**LVDS 155.52 MHz (Output)).** Differential outputs generating a 155.52MHz clock
32	V$_{SS4}$	**Digital ground.** 0 Volts
33	VREF	**LVDS Reference Voltage (Input).**
34	Tdo	**IEEE 1149.1a Test Data Output (Output).** If not used, this pin should be left unconnected.
35	Tms	**IEEE 1149.1a Test Mode Selection (Input)**. If not used, this pin should be pulled high.
36	Tclk	**IEEE 1149.1a Test Clock Signal (Input)**. If not used, this pin should be pulled high.

Pin Description (continued)

Pin #	Name	Description
37	$\overline{Trst}$	**IEEE 1149.1a Reset Signal (Input).** If not used, this pin should be held low.
38	Tdi	**IEEE 1149.1a Test Data Input (Input).** If not used, this pin should be pulled high.
39	FS2	**Frequency Select 2 (Input).** This input, in conjunction with FS1, selects which of four possible frequencies (8kHz, 1.544MHz, 2.048MHz or 19.44MHz) may be input to the PRI and SEC inputs. See Table 1 on page 6.
40	FS1	**Frequency Select 1 (Input).** This input, in conjunction with FS2, selects which of four possible frequencies (8kHz, 1.544MHz, 2.048MHz or 19.44MHz) may be input to the PRI and SEC inputs. See Table 1 on page 6.
41	PRIOOR	**Primary Reference Out Of Range (CMOS Output).** A logic high at this pin indicates that the primary reference is off the PLL center frequency by more than 12 ppm. The measurement is done on a 1 second basis using a signal derived from the 20MHz clock input on C20i. When the accuracy of the 20MHz clock is $\pm$ 4.6ppm, the effective out of range limits of the PRIOOR signal will be +16.6ppm to -7.4ppm or +7.4ppm to -16.6ppm.
42	C1.5o	**Clock 1.544MHz (CMOS Output).** This output is used in T1 applications.
43	C6	**Clock 6.312MHz (CMOS Output).** This output is used for DS2 or J2 applications.
44	IC	**Internal Connection.** Tie low for normal operation.
45	V_{SS5}	**Digital ground.** 0 Volts
46	C19o	**Clock 19.44MHz (CMOS Output).** This output is used in OC-N and STM-N applications.
47	RSEL	**Reference Source Select (Input).** A logic low selects the PRI (primary) reference source as the input reference signal and a logic high selects the SEC (secondary) input. The logic level at this input is gated in by the rising edge of F8o.
48	$\overline{TCLR}$	**TIE Circuit Clear (Input).** A logic low at this input clears the Time Interval Error (TIE) correction circuit resulting in a realignment of output phase with input phase. The $\overline{TCLR}$ pin should be held low for a minimum of 300ns. When this pin is held low, the time interval error correction circuit is disabled.
49	V_{DD3}	**Positive Power Supply. Digital supply**.
50	NC	**No Connection.**
51	C20i	**20 MHz Clock Input (5V tolerant Input).** This pin is the input for the master 20MHz clock.
52	V_{SS7}	**Digital ground.** 0Volts
53	C34/C44	**Controlled Clock 34.368MHz / Clock 44.736MHz (CMOS Output).** This output clock is programmable to be either 34.368MHz (for E3 applications) or 44.736MHz (for DS3 applications). The output clock is controlled via control pins in Hardware Mode or control bits when the device is in Microport Mode. If the E3DS3/$\overline{OC3}$ control pin or control bit is high, the C34/C44 pin will output its nominal frequency. If the E3DS3/$\overline{OC3}$ control pin or bit is low, the C34/C44 pin will output its nominal frequency divided by 4. (C8.5o/C11o)
54	V_{DD4}	**Positive Power Supply.** Digital supply.
55	HOLDOVER	**Holdover (CMOS Output).** This output goes high when the device is in holdover mode.
56	PCCi	**Phase Continuity Control Input (3V Input).** The signal at this pin affects the state changes between Primary Holdover Mode and Primary Normal Mode and Primary Holdover Mode and Secondary Normal Mode. The logic level at this input is gated by the rising edge of F8o. See "Figure 12 - Control State Diagram" on page 13 for details.

Pin Description (continued)

Pin #	Name	Description
57	LOCK	**Lock Indicator (CMOS Output).** This output goes high when the PLL is in frequency lock to the input reference.
58	FLOCK	**Fast Lock Mode (Input).** In hardware mode, hold this pin high to lock faster than normal to the input reference. This pin performs no function if the device is not in hardware mode. In Fast Lock Mode, the wander generation of the PLL is, of necessity, compromised.
59	$\overline{DS}$	**Data Strobe (5V tolerant Input)**. This input is the active low data strobe of the Motorola processor interface.
60	IC	**Internal Connection.** Tie low for normal operation.
61	SECOOR	**Secondary Reference Out Of Capture Range (CMOS Output).** A logic high at this pin indicates that the secondary reference is off the PLL center frequency by more than 12 ppm. The measurement is done on a 1 second basis using a signal derived from the 20MHz clock input on the C20i pin. When the accuracy of the 20MHz clock is $\pm$ 4.6ppm the effective out of range limits of the SECOOR signal will be +16.6ppm to -7.4ppm or +7.4ppm to -16.6ppm.
62	OE	**Output Enable (Input).** Tie high for normal operation. Tie low to force output clocks pins F16, F8, C16, C8, C4, C2 to a high impedance state.
63	$\overline{CS}$	**Chip Select (5V tolerant Input)**. This active low input enables the non-multiplexed Motorola parallel microprocessor interface of the MT90401. When $\overline{CS}$ is set to high, the microprocessor interface is idle and all bus I/O pins will be in a high impedance state.
64	$\overline{RST}$	**RESET (5V tolerant Input).** This active low input puts the MT90401 in a reset condition. $\overline{RST}$ should be set to high for normal operation. The MT90401 should be reset after power-up and after the selected reference frequency is changed. The $\overline{RST}$ pin must be held low for a minimum of 1μsec. to reset the device properly.
65	HW	**Hardware Mode (Input)**. If this pin is tied low, the device is in microport mode and is controlled via the microport. If it is tied high, the device is in hardware mode and is controlled via the control pins MS1, MS2, FS1, FS2, FLOCK and SONET/SDH.
66-69	D0 - D3	**Data 0 to Data 3 (5V tolerant Three-state I/O)**. These signals combined with D4-D7 form the bidirectional data bus of the parallel processor interface (D0 is the least significant bit).
70	V_{SS8}	**Digital ground.** 0 Volts.
71	IC	**Internal Connection.** Tie low for normal operation.
72	IC	**Internal Connection.** Tie low for normal operation.
73	V_{DD5}	**Positive Power Supply.** Digital supply.
74-77	D4 - D7	**Data 4 to Data 7 (5V tolerant Three-state I/O).** These signals combined with D0-D7 form the bidirectional data bus of the parallel processor interface (D7 is the most significant bit).
78	R/$\overline{W}$	**Read/Write Select (5V tolerant Input).** This input controls the direction of the data bus D[0:7] during a microprocessor access. When R/$\overline{W}$ is high, the parallel processor is reading data from the MT90401. When low, the parallel processor is writing data to the MT90401.
79	A0	**Address 0 (5V tolerant Input).** Address input for the parallel processor interface. A0 is the least significant input.
80	IC	**Internal Connection.** Tie low for normal operation.

MT90401

Functional Description

The MT90401 is a SONET/SDH System Synchronizer, providing timing (clock) and synchronization (frame) signals to interface circuits for Digital Telecommunications Transmission links. Figure 1 is a functional block diagram which is described in the following sections.

Reference Select MUX Circuit

The MT90401 accepts two simultaneous reference input signals and operates on their falling edges. Either the primary reference (PRI) signal or the secondary reference (SEC) signal can be selected as input to the TIE Corrector Circuit. The selection is based on the Control, Mode and Reference Selection of the device. See Table 1 and Table 4.

Frequency Select MUX Circuit

The MT90401 operates with one of four possible input reference frequencies (8kHz, 1.544MHz, 2.048MHz or 19.44MHz). The frequency select inputs, FS1 and FS2, which come from pins in hardware mode and control bits in microport mode determine which of the four frequencies may be used at the reference inputs (PRI and SEC). Both inputs must have the same frequency applied to them. A reset (RST) must be performed after every frequency select input change. See Table 1 - Input Frequency Selection.

FS2	FS1	Input Frequency
0	0	19.44MHz
0	1	8kHz
1	0	1.544MHz
1	1	2.048MHz

Table 1. Frequency Selection

Time Interval Error (TIE) Corrector Circuit

The TIE corrector circuit, when enabled, prevents a step change in phase on the input reference signals (PRI or SEC) from causing a step change in phase at the input of the DPLL block of Figure 1.

During reference input rearrangement, such as during a switch from the primary reference (PRI) to the secondary reference (SEC), a step change in phase on the input signals will occur. A phase step at the input of the DPLL would lead to unacceptable phase changes in the output signal.

As shown in Figure 3, the TIE Corrector Circuit receives one of the two reference (PRI or SEC) signals, passes the signal through a programmable delay line, and uses this delayed signal as an internal virtual reference, which is input to the DPLL. Therefore, the virtual reference is a delayed version of the selected reference. During a switch from one reference to the other, the State Machine first changes the mode of the device from Normal to Holdover. In Holdover Mode, the DPLL no longer uses the virtual reference signal, but generates an
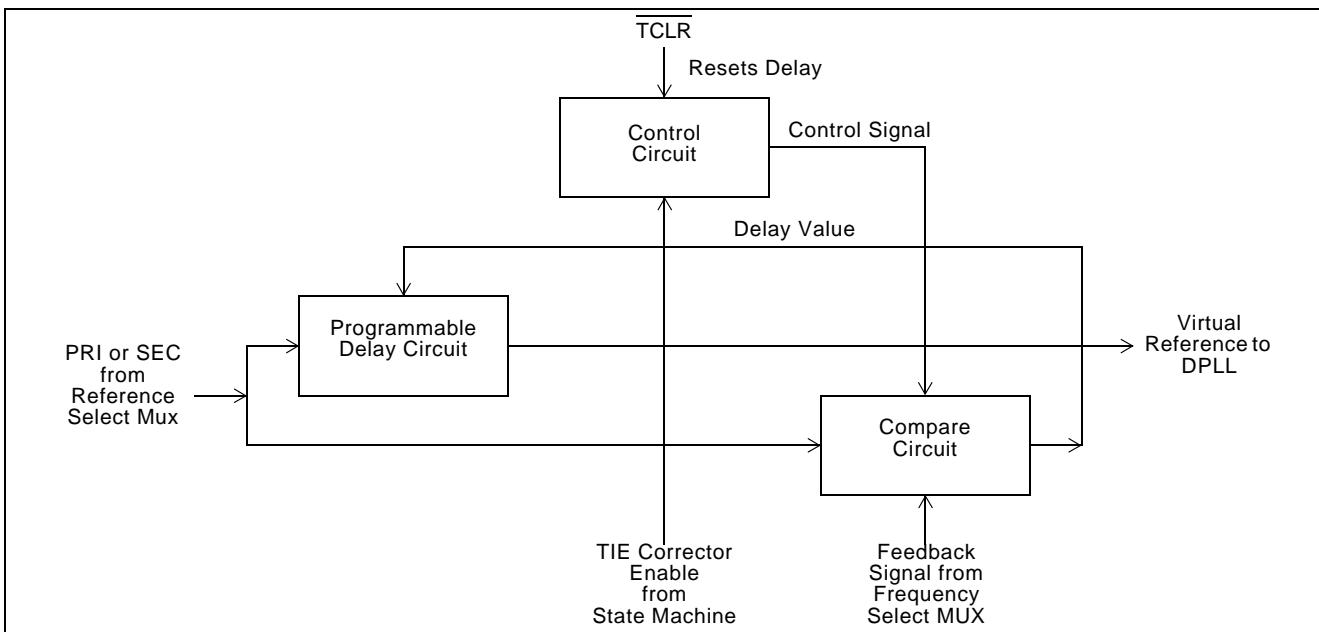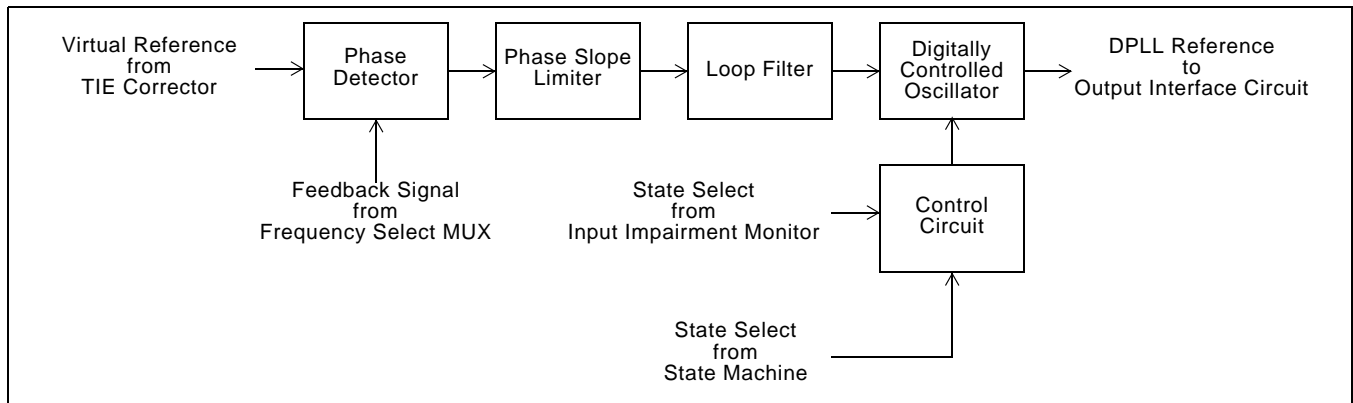

Figure 3 - TIE Corrector Circuit

Figure 4 - DPLL Block Diagram

accurate clock signal using storage techniques. The Compare Circuit then measures the phase delay between the current phase (feedback signal) and the phase of the new reference signal. This delay value is passed to the Programmable Delay Circuit (See Figure 3). The new virtual reference signal is now at the same phase position as the previous reference signal would have been if the reference switch had not taken place.   The State Machine then returns the device to Normal Mode.

The DPLL now uses the new virtual reference signal, and since no phase step took place at the input of the DPLL, no phase step occurs at the output of the DPLL. In other words, reference switching will not create a phase change at the input of the DPLL, or at the output of the DPLL.

Since internal delay circuitry maintains the alignment between the old virtual reference and the new virtual reference, a phase error may exist between the selected input reference signal and the output signal of the DPLL. This phase error is a function of the difference in phase between the two input reference signals during reference rearrangements. Each time a reference switch is made, the delay between input signal and output signal will change. The value of this delay is the accumulation of the error measured during each reference switch.

The programmable delay circuit can be reset to zero by applying a logic low pulse to the TIE Circuit Clear (TCLR) pin. A minimum reset pulse width is 300ns. This results in a phase realignment between the input reference signal and the output signal as shown in Figure 16. The speed of the phase alignment correction is limited to 885 ns/s in SONET mode and 53ns per 1.326 ms in SDH mode, convergence is in the direction of least phase travel.

The state diagram of Figure 7 indicates the state changes for which the TIE Corrector Circuit is activated.

Digital Phase Lock Loop (DPLL)

As shown in Figure 4, the DPLL of the MT90401 consists of a Phase Detector, Phase Slope Limiter, Loop Filter, Digitally Controlled Oscillator, and a Control Circuit.

Phase Detector - the Phase Detector compares the virtual reference signal from the TIE Corrector circuit with the feedback signal from the Frequency Select MUX circuit, and provides an error signal corresponding to the phase difference between the two. This error signal is passed to the Phase Slope Limiter circuit. The Frequency Select MUX allows the proper feedback signal to be externally selected (e.g., 8kHz, 1.544MHz, 2.048MHz or 19.44MHz).

Phase Slope Limiter - the Phase Slope Limiter receives the error signal from the Phase Detector and ensures that the DPLL responds to all input transient conditions with a limited output phase slope. In SONET Mode the maximum output phase slope is limited to 885ns/s as per Telcordia GR-253-CORE. In SDH Mode the maximum output phase slope is 53ns per 1.326ms.

Loop Filter - the Loop Filter is a low pass filter, that defines the network jitter and wander transfer requirements for all input reference frequencies (8kHz, 1.544MHz, 2.048MHz, or 19.44MHz). In SONET mode the loop filter has a cut-off frequency of 70mHz to comply with Telcordia GR-253-CORE and GR-1244-CORE. In SDH mode the loop filter has a cut-off frequency of 1.1Hz to comply with ITU-T G.813 Option 1 and GR-1244-CORE.

Control Circuit - the Control Circuit uses status and control information from the State Machine and the Input Impairment Circuit to set the mode of the DPLL. The three possible modes are Normal, Holdover and Freerun.

Digitally Controlled Oscillator (DCO) - the DCO receives the limited and filtered signal from the Loop Filter, and based on its value, generates a corresponding digital output signal. The synchronization method of the DCO is dependent on the state of the MT90401.

In Normal Mode, the DCO provides an output signal which is frequency and phase locked to the selected input reference signal.

In Holdover Mode, the DCO is free running at a frequency equal to the last locked frequency the DCO was generating while in Normal Mode. In order to improve accuracy of the Holdover Mode the actual frequency sample is taken 30-60ms before switching into holdover.

In Freerun Mode, the DCO is free running with an accuracy equal to the accuracy of the C20i 20MHz source.

Telcordia GR-253-CORE requires that, during recovery from holdover, SONET clocks not change their output frequency at a rate faster than 2.9ppm per second. In SONET Mode the MT90401 limits the rate of change of its output frequency (frequency slope) to less than 1.9ppm per second; this limit remains in place when the PLL is in Fast Lock Mode.

Lock Indicator - If the PLL is in frequency lock (frequency lock means the center frequency of the PLL is identical to the line frequency), and the input phase offset is small enough such that no phase slope limiting is exhibited, then the lock signal will be set high.

Output Interface Circuit

The output of the DCO (DPLL) is used by the Output Interface Circuit to provide the output signals shown in Figure 5. The Output Interface Circuit uses five Tapped Delay Lines in MT90401 followed by a T1 Divider Circuit, an E1 Divider Circuit, a DS2 Divider Circuit, and a x4/x8 PLL, to generate the required output signals.

Five tapped delay lines are used to generate 8.592MHz, 11.184MHz, 16.384MHz, 12.352MHz, 12.624MHz and 19.44 MHz signals.

The E1 Divider Circuit uses the 16.384MHz signal to generate four clock outputs and three frame pulse outputs. The C8o, C4o and C2o clocks are generated by simply dividing the C16o clock by two, four and eight respectively. These outputs have a nominal 50% duty cycle. The frame pulse outputs (F0o, F8o, and F16o) are generated directly from the C16 clock.

The T1 Divider Circuit uses the 12.352MHz signal to generate C1.5o. This output has a nominal 50% duty cycle. The DS2 Divider Circuit uses the 12.624 MHz signal to generate the clock output C6o. This output has a nominal 50% duty cycle.

The 19.44MHz signal is output on the C19o pin and it is multiplied by an internal PLL to generate the 155.52MHz clock output on the C155P/N pins. The C155P/N clock has a nominal 50% duty cycle.

The 8.592MHz and 11.184 MHz signals are multiplied by an internal PLL to generate the 34.368MHz or 44.736MHz clock output on the C34/C44 pin. If the internal PLL is dedicated to the C155P/N clock then the C34/C44 pin will output the 8.592MHz or 11.184 MHz clocks. The 34.368Mhz and 44.736MHz clocks have a nominal 50% duty cycle. The duty cycles of the 8.592MHz and 11.184MHz signals are dependent on the duty cycle of the 20MHz clock input to the C20i pin.
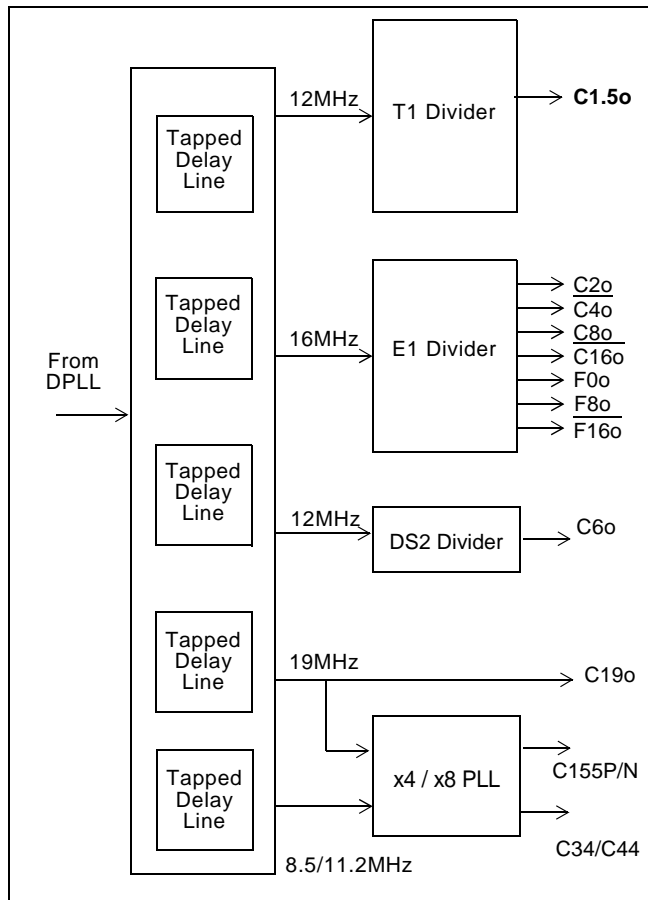
Figure 5 - Output Interface Circuit Block Diagram

The T1 and E1 signals are generated from a common DPLL signal. Consequently, all frame pulses and clock outputs are locked to one another for all operating states, and are also locked to the selected input reference in Normal Mode. See Figure 18.

All frame pulses and clock outputs have limited driving capability, and should be buffered when driving capacitive loads exceeding 30pF.

Input Impairment Monitor

This circuit monitors the input signal to the DPLL and automatically enables the Auto-Holdover when the frequency of the incoming signal is outside the Auto-Holdover capture range. (See Performance Characteristics - Mode Switching). This includes a complete loss of incoming signal, or a large frequency shift in the incoming signal. When the incoming signal returns to normal, the DPLL is returned to Normal Mode with the output signal locked to the input signal. The holdover output signal in the MT90401 is based on the incoming signal 30ms minimum to 60ms prior to entering the

Holdover Mode. The amount of phase drift while in holdover is negligible because the Holdover Mode is very accurate (i.e., 0.02ppm). Consequently, the phase delay between the input and output after switching back to Normal Mode is preserved.

State Machine Control

An internal state machine can be enabled to control the TIE Corrector Circuit as shown in Figure 1. In hardware mode, control is based on the logic levels at the control inputs RSEL, MS1, MS2 and PCCi (See Figure 6). In Microport mode, control is based on the state of control bits RSEL, MS1 and MS2 and the PCCi pin. When switching from Primary Holdover to Primary Normal, the TIE Corrector Circuit is enabled when PCCi = 1, and disabled when PCCi = 0.

All state machine changes occur synchronously on the rising edge of F8o. See the Control and Mode of Operation section for full details.
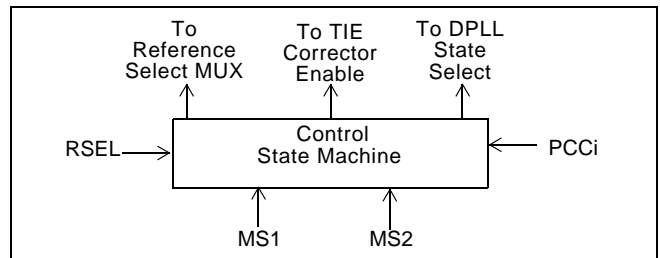

Figure 6 - Control State Machine Block Diagram Master Clock

The MT90401 uses an external oscillator as the master timing source. For recommended master timing circuits, see the Applications - Master Clock section.

Control and Mode of Operation

The MT90401 has three possible modes of operation, Normal, Holdover and Freerun.

In hardware mode the Mode/Control Select pins MS2 and MS1 select the mode and method of control as shown in Table 3.

RSEL	Input Reference
0	PRI
1	SEC

Table 2. Input Reference Selection

MS2	MS1	Mode
0	0	NORMAL
0	1	HOLDOVER
1	0	FREERUN
1	1	Reserved

Table 3. Operating Modes and States

The active reference input (PRI or SEC) is selected by the RSEL pin as shown in Table 2. Refer to Table 4 and Figure 12 for details of the state change sequences.

Normal Mode

Normal Mode is typically used when a slave clock source, synchronized to the network is required.

In Normal Mode, the MT90401 provides timing and frame synchronization signals, which are synchronized to one of two reference inputs (PRI or SEC). The input reference signal may have a nominal frequency of 8kHz, 1.544MHz, 2.048MHz or 19.44MHz.

The selection of input references is control dependent as shown in state table 4. The reference frequencies are selected by the frequency control pins/bits FS2 and FS1 as shown in Table 1.

Holdover Mode

Holdover Mode is typically used when network synchronization is temporarily disrupted.

In Holdover Mode, the MT90401 provides timing and synchronization signals, which are not locked to an external reference signal, but are based on storage techniques. The storage value is determined while the device is in Normal Mode and locked to an external reference signal

When in Normal Mode, and locked to the input reference signal, a numerical value corresponding to the MT90401 output reference frequency is stored alternately in two memory locations every 30ms. When the device is switched into Holdover Mode, the value in memory from between 30ms and 60ms is used to set the output frequency of the device.

The frequency accuracy of Holdover Mode is ±0.02ppm, which translates to a worst case 14 frame (125us) slips in 24 hours. This is better than the Telcordia GR-1244-CORE Stratum 3 requirement of ±0.37ppm (255 frame slips per 24 hours).

Two factors affect the accuracy of Holdover Mode. One is drift on the Master Clock and the other is jitter on the reference signal. The drift on the Master Clock oscillator propagates unattenuated and causes the same drift on the output clocks. This drift can only be reduced by selecting more stable Master Clock oscillator. For example, a ±4.6ppm temperature compensated clock oscillator may have a temperature coefficient of 0.03ppm per degree C. The 10 degc change while in Holdover Mode, will result in an additional offset in frequency accuracy equal to 0.3ppm which is much greater than the internal holdover accuracy of the MT90401 (0.02ppm).

The other factor affecting accuracy is large jitter on the reference input prior (30ms to 60ms) to the mode switch. For instance, jitter of 7.5UI at 700Hz may reduce the Holdover Mode accuracy from 0.02ppm to 0.10ppm.

Freerun Mode

Freerun Mode is typically used when a master clock source is required, or immediately following system power-up before network synchronization is achieved.

In Freerun Mode, the MT90401 provides timing and synchronization signals which are based on the master clock frequency (C20i) only, and are not synchronized to the reference signals (PRI and SEC).

The accuracy of the output clock is equal to the accuracy of the master clock (C20i). So if a ±20ppm output clock is required, the master clock must also be ±20ppm. See Applications - Master Clock section.

Fast Lock Mode

Fast Lock Mode is a submode of Normal Mode, it is used to allow the MT90401 to lock to a reference eight times more quickly than normal. Fast Lock Mode necessarily compromises the wander generation characteristics of the MT90401. When the MT90401 is in Fast Lock Mode and SONET Mode at the same time, the PLL frequency slope is limited to less than 1.9ppm per second.

Transitions from Freerun Mode or Holdover Mode to Normal Mode

Telcordia GR-253-CORE requires SONET Internal Clocks to settle within 100s after transitioning from Freerun Mode or Holdover Mode to Normal Mode. During such a transition, the wander filtering requirements for a SONET Internal Clock are relaxed to make a 100s settling time possible.

To meet the GR-253-CORE 100s settling time requirement at power-up and during a transition from Freerun Mode to Normal Mode the MT90401 should be placed in its SDH Mode until lock is achieved. When the PLL indicates lock the MT90401 should be placed in SONET Mode.

During a transition from Holdover Mode to Normal Mode, GR-253-CORE requires a SONET Internal Clock to limit the frequency slope to less than 2.9ppm per second. To meet the 100s settling time during such a transition it is necessary to keep the MT90401 in SONET Mode and Fast Lock Mode until lock is achieved. When the PLL indicates lock the MT90401 can be taken out of its Fast Lock Mode.

A transition from Holdover Mode to Normal Mode can result in a large initial frequency offset, for example 4.6ppm, between the clock's reference and its output. The 2.9ppm per second frequency slope limit required by GR-253-CORE places a lower limit on the time it takes for a SONET Internal Clock to acquire a new frequency. While the clock is acquiring the new frequency a phase error will accumulate which could cause the clock's settling time to be longer than 100s. GR-1244-CORE and GR-253-CORE allow a clock to ignore some of the phase error accumulated during the transition from Holdover Mode to Normal Mode.

During a transition from Holdover Mode to Normal Mode, if the MT90401 has not achieved lock within 16 seconds, it is recommended that the PLL be put briefly into its Holdover Mode and then returned to Normal Mode by toggling the MS1 pin or the MS1 control bit. Toggling the PLL into and out of Holdover will clear any accumulated phase error and reduce the settling time.

MT90401 Measures of Performance

The following are some synchronizer performance indicators and their corresponding definitions.

Jitter Generation

Jitter generation is the amount of jitter produced by a PLL and is measured at its output. It is measured by applying a reference signal with no jitter to the input of the device, and measuring its output jitter. Jitter generation may also be measured when the device is in a non-synchronizing mode, such as free running or holdover, by measuring the output jitter of the device. Jitter generation is usually measured with various band-limiting filters depending on the applicable standards.

Jitter Tolerance

Jitter tolerance is a measure of the ability of a PLL to operate properly (i.e., remain in lock and or regain lock in the presence of large jitter magnitudes at various jitter frequencies) when jitter is applied to its reference. The applied jitter magnitude and jitter frequency depends on the applicable standards (see Figures 7, 8 and 9).
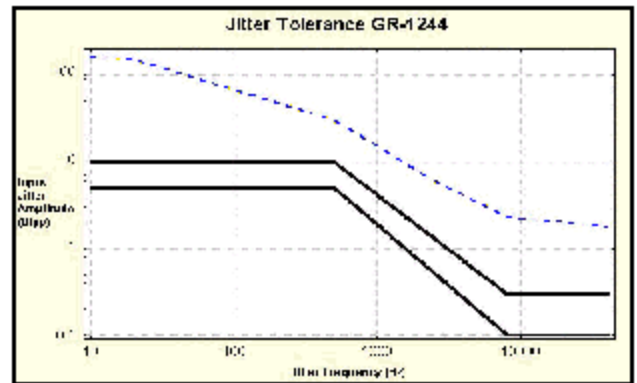

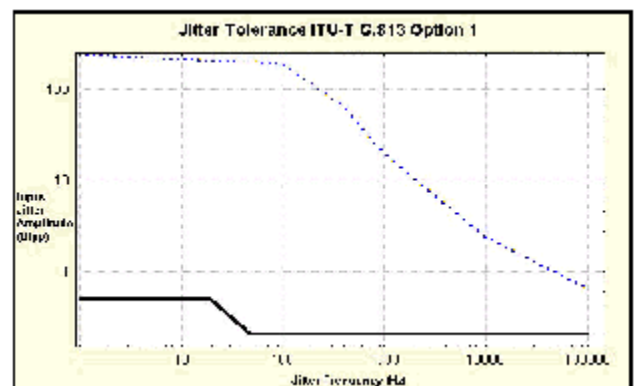**Figure 7 - Jitter Tolerance GR-1244 1.544MHz Reference**

Figure 8 - Jitter Tolerance ITU-T G.813 Option 1

Figure 9 - Jitter Tolerance SONET Category II (OC1) 19.44 MHz Input Reference

Jitter Transfer

Jitter transfer or jitter attenuation refers to the magnitude of jitter at the output of a device for a given amount of jitter at the input of the device. Input jitter is applied at various amplitudes and frequencies, and output jitter is measured with various filters depending on the applicable standards.

For the MT90401, two internal elements determine the jitter attenuation. This includes the low pass loop filter and the phase slope limiter. Both of these parameters have different settings depending on whether the device is in SONET or SDH mode. For SONET mode the loop filter has a corner frequency of 70 millihertz and the output phase slope is limited to 885ns per second. For SDH mode the loop filter has a corner frequency of 1.1 Hertz and a maximum phase slope of 53ns per 1.326 milliseconds. If the input signal exceeds this rate, such as for very large amplitude low frequency input jitter, the maximum output phase slope will be limited.

The MT90401 has ten outputs that can be locked to four possible input frequencies for a total of 40 possible jitter transfer functions. Since all outputs are derived from the same internal signal, the jitter transfer values for the four cases, 8kHz to 8kHz, 1.544MHz to 1.544MHz, 2.048MHz to 2.048MHz 19.44 MHz to 19.44 MHz can be applied to all outputs.
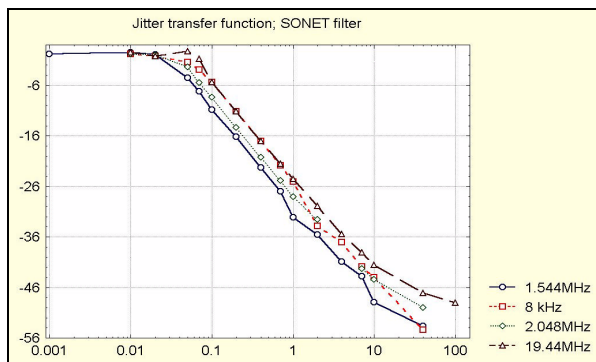

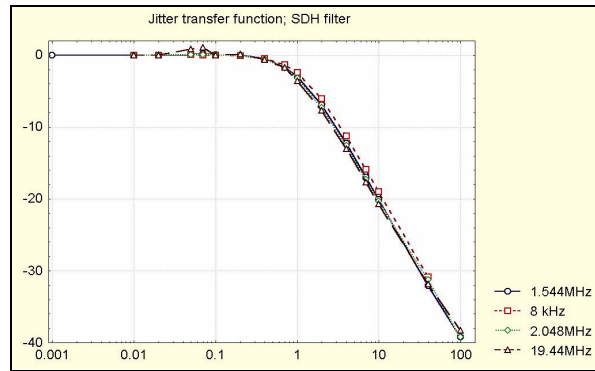**Figure 10 - Jitter and Wander Transfer with SONET filter**

Figure 11 - Jitter and Wander Transfer with SDH Filter

It should be noted that 1UI at 1.544MHz is 648ns, which is not equal to 1UI at 2.048MHz, which is 488ns. Consequently, a transfer value using different input and output frequencies must be calculated in common units (e.g., seconds) as shown in the following example.

Example: *What is the T1 and E1 output jitter when the T1 input jitter is 20UI (T1 UI Units) and the T1 to T1 jitter attenuation is 18dB?*

$$OutputT1 = InputT1 \times 10^{\left(\frac{-A}{20}\right)}$$

$$OutputT1 = 20 \times 10^{\left(\frac{-18}{20}\right)} = 2.5UI(T1)$$

$$OutputE1 = OutputT1 \times \frac{(1UIT1)}{(1UIE1)}$$

$$OutputE1 = OutputT1 \times \frac{(644ns)}{(488ns)} = 3.3UI(T1)$$

Using the above method, the jitter attenuation can be calculated for all combinations of inputs and outputs based on the four jitter transfer functions provided.

Since intrinsic jitter generation is always present, jitter attenuation will appear to be lower for small input jitter signals than for large ones. Consequently, accurate jitter transfer function measurements are usually made with large input jitter signals (e.g., 75% of the specified maximum jitter tolerance).

| Description				State				
Input Controls				**Freerun**	**Normal (PRI)**	**Normal (SEC)**	**Holdover (PRI)**	**Holdover (SEC)**
MS2	**MS1**	**RSEL**	**PCCi**	**S0**	**S1**	**S2**	**S1H**	**S2H**
0	0	0	0	S1	-	S1 MTIE	S1	S1 MTIE
0	0	0	1	S1	-	S1 MTIE	S1 MTIE	S1 MTIE
0	0	1	X	S2	S2 MTIE	-	S2 MTIE	S2 MTIE
0	1	0	X	/	S1H	/		/
0	1	1	X	/	S2H	S2H	/	-
1	0	X	X	-	S0	S0	S0	S0
Legend: - No Change / Not Valid MTIE State change occurs with TIE Corrector Circuit Refer to Control State Diagram for state changes to and from Auto-Holdover State								

Table 4. Control State Table
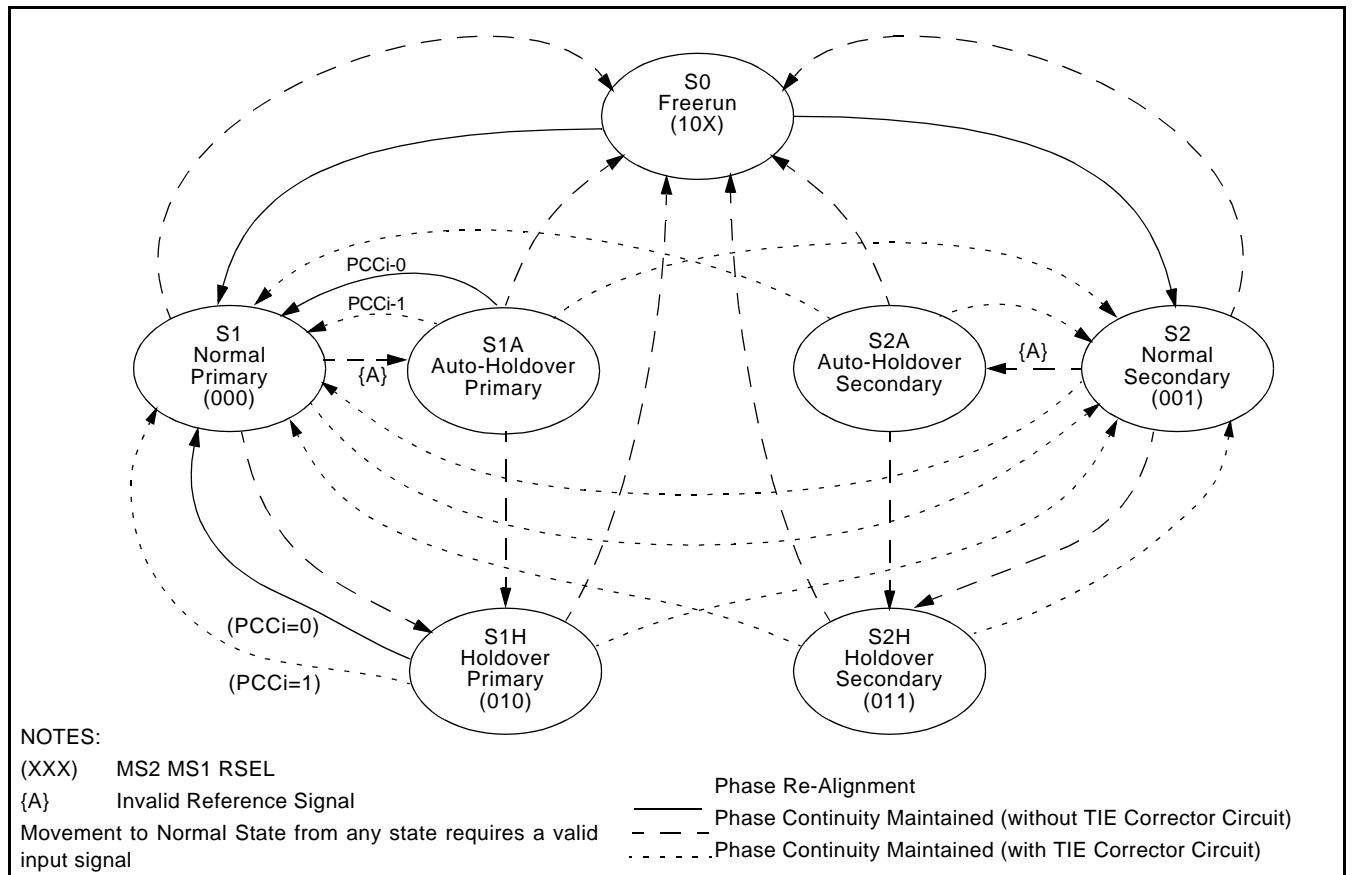
Figure 12 - Control State Diagram

Frequency Accuracy

Frequency accuracy is defined as the absolute tolerance of an output clock signal when it is not locked to an external reference, but is operating in a free running mode. For the MT90401, the Freerun accuracy is equal to the Master Clock (C20i) accuracy.

Holdover Accuracy

Holdover accuracy is defined as the absolute tolerance of an output clock signal, when it is not locked to an external reference signal, but is operating using storage techniques. For the MT90401, the storage value is determined while the device is in Normal Mode and locked to an external reference signal. The initial frequency offset of the MT90401 in Holdover Mode is $\pm20 \times 10^{-9}$. This is more accurate than Telcordia's GR-1244-CORE stratum 3 requirements of $\pm50 \times 10^{-9}$. Once the MT90401 has transitioned into Holdover Mode, holdover stability is determined by the stability of the 20MHz Master Clock Oscillator.

The absolute Master Clock (C20i) accuracy of the MT90401 does not affect Holdover accuracy, but the change in C20i accuracy while in Holdover Mode does.

Capture Range

Also referred to as pull-in range. This is the input frequency range over which the synchronizer must be able to pull into synchronization. The MT90401 capture range is equal to ±52 ppm minus the accuracy of the master clock (C20i). For example, a ±32 ppm master clock results in a capture range of ±20 ppm.

In Telcordia GR-1244-CORE, it is a conditional requirement that the PLL should be able to reject references that are off the nominal frequency by more than 17ppm. MT90401 provides two pins and two bits, PRIOOR and SECOOR, to indicate whether the primary and secondary reference are within the 17ppm of the nominal frequency. When the accuracy of the 20MHz oscillator is 4.6ppm the effective out of range limits of the PRIOOR and SECOOR pins will be +16.6ppm to -7.4ppm or +7.4ppm to -16.6ppm. Both references are monitored at the same time. PRIOOR and SECOOR are updated every 1.0 to 1.5 seconds.

Lock Range

This is the input frequency range over which the synchronizer must be able to maintain synchronization. The lock range is equal to the capture range for the MT90401.

Phase Slope

Phase slope is measured in seconds per second and is the rate at which a given signal changes phase with respect to an ideal signal. The given signal is typically the output signal. An ideal signal is one that is at exactly the nominal frequency and is completely free of jitter and wander.

Frequency Slope

Frequency slope is measured in ppm per second and is the rate at which the fractional frequency offset of a given signal changes. The fractional frequency offset is calculated with respect to an ideal signal. The given signal is typically the output signal. An ideal signal is one that is at exactly the nominal frequency and is completely free of jitter and wander.

Time Interval Error (TIE)

TIE is the time delay between a given timing signal and an ideal timing signal.

Maximum Time Interval Error (MTIE)

MTIE is the maximum peak to peak delay between a given timing signal and an ideal timing signal within a particular observation period.

$$MTIE(S) = TIEmax(t) - TIEmin(t)$$

Phase Continuity

Phase continuity is the phase difference between a given timing signal and an ideal timing signal at the end of a particular observation period. Usually, the given timing signal and the ideal timing signal are of the same frequency. Phase continuity applies to the output of the synchronizer after a signal disturbance due to a reference switch or a mode change.

Phase Lock Time

This is the time it takes the synchronizer to phase lock to the input signal. Phase lock occurs when the input signal and output signal are not changing in phase with respect to each other (not including jitter).

Lock time is very difficult to determine because it is affected by many factors which include:

i) initial input to output phase difference

ii) initial input to output frequency difference

iii) synchronizer loop filter

iv) synchronizer limiter

Although a short lock time is desirable, it is not always possible to achieve due to other synchronizer requirements. For instance, better jitter transfer performance is achieved with a lower frequency loop filter which increases lock time. And better (smaller) phase slope performance (limiter) results in longer lock times. The MT90401 loop filter and limiter were optimized to meet the GR-253-CORE, GR-1244-CORE, and G-813 jitter transfer and phase slope requirements.

MT90401 and Network Specifications

The MT90401 meets all applicable PLL requirements for the following specifications.

1. Telcordia GR-1244-CORE December 2000 for Stratum 3, SONET Minimum Clock (SMC), Stratum 4 Enhanced and Stratum 4

2. Telcordia GR-253-CORE September 2000 for SONET Internal Clocks

3. ANSI T1.101 (DS1) February 1994 for Stratum 3, Stratum 4 Enhanced and Stratum 4

4. ANSI T1.105.09-1996 for SONET Minimum Clocks (SMCs)

5. ITU-T G.813 August 1996 for Option1 and Option 2 clocks (with external jitter attenuator)

Applications

This section contains MT90401 application specific details for Master clock operation, LVDS output drivers setup, microport functionality and output clock phase adjustment.

Master Clock

In Freerun Mode, the frequency tolerance at the clock outputs is identical to the frequency tolerance of the source at the C20i input pin.

Another consideration in determining the accuracy of the master timing source is the desired capture range. The sum of the accuracy of the master timing source and the capture range of the MT90401 will always equal 52ppm. For example, if the master

timing source is ± 20 ppm, then the capture range will be ± 32 ppm.

TIE Correction (using PCCi)

When Primary Holdover Mode is entered for short time periods, TIE correction should not be enabled. This will prevent unwanted accumulated phase change between the input and output.

For example, we can estimate phase accumulation for a case when ten Normal to Holdover to Normal sequential mode changes occur, with each Holdover entered for 2s with <u>TIE enabled</u>. Each mode change could account for a phase shift as large as 250ns. Thus, the accumulated phase could be as large as 2.9us, and, the overall MTIE could be as large as 2.9us.

$$Phase_{hold} = 0.02ppm \times 2s = 40ns$$

$$Phase_{state} = 50ns + 200ns = 250ns$$

$$Phase_{10} = 10 \times (250ns + 40ns) = 2.9us$$

- *0.02ppm is the accuracy of Holdover Mode*
- *50ns is the maximum phase continuity of the MT90401 from Normal Mode to Holdover Mode*
- *200ns is the maximum phase continuity of the MT90401 from Holdover Mode to Normal Mode (with or without TIE Corrector Circuit)*

When the same ten Normal to Holdover to Normal mode changes occur with <u>TIE disabled</u>, the overall MTIE will only be 250ns. There would be no accumulated phase change, since the input to output phase is re-aligned after every Holdover to Normal state change.

C155 clock generation and LVDS output drivers

The MT90401 provides a 155.52MHz clock that is frequency locked to the internally generated 19.44MHz clock. The locking of both clocks is achieved by the internal analog PLL that multiplies the 19.44MHz clock eight times. This C155 clock is output on pins C155P and C155N in LVDS format. The LVDS offset voltage Vos is set by applying an external 1.25V reference voltage to the Vref input (pin 33). This pin can be connected to a common 1.25V voltage reference that may exist on the customer board or alternatively can be generated by a simple voltage divider as it is shown in Figure 13 - LVDS Voltage Offset Vos Generation Circuit. To ensure proper operation of LVDS drivers, the decoupling capacitor must be placed very close to the MT90401 package.
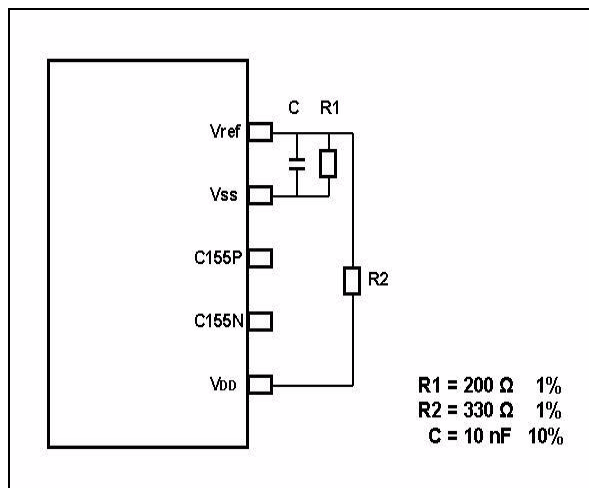

Figure 13 - LVDS Voltage Offset Vos Generation Circuit

Microport

If the HW pin is tied low, an 8 bit Motorola microprocessor may be used to control the PLL and report on the device status. In this case the control pins SONET/SDH, RSEL, MS1, MS2, FS1, FS2, and FLOCK are unused and they are replaced by the control bits SONET/SDH, RSEL, MS1, MS2, FS1, FS2, FLOCK. The input pin PCCi remains in use. The output pins LOCK, HOLDOVER, SECOOR, PRIOOR function whether the device is in microprocessor mode or hardware mode, but these signals are also available in Status Register 1. The microport provides additional functionality not available in hardware.

Output Phase Adjustment

Two control registers are available to program the output phase offset of the generated clocks. All 16.384 MHz derived outputs clocks, F16o, F80, F0o, C16o, C8o, C4o and C2o can be collectively shifted up to 125 microseconds with a step size of 60 nS with respect to the input reference by programming the Set Delay Word 1 and Set Delay Word 2 registers.

Control and Status Registers

Address ($A_6A_5A_4A_3A_2A_1A_0$)	Register	Read/ Write	Function
00H (Table 6)	Control Register 1	Read/ Write	RSEL, $\overline{FS2}$, FS1, MS2, MS1, SONET/$\overline{SDH}$ FLOCK, $\overline{TCLR}$
01H (Table 7)	Status Register 1	Read Only	PRIOOR, SECOOR, LOCK, HOLDOVER, RSV, FLim, RSV, RSV
02H	Reserved	Read Only	
03H	Reserved	Read Only	
04H (Table 8)	Control Register 2	Read/ Write	E3/DS3/$\overline{OC3}$, E3/$\overline{DS3}$, RSV=0, RSV=0, RSV=0, RSV=0, RSV=0, RSV=0.
05H	Reserved	Read / Write	Set all bits to zero.
06H (Table 9)	Set Delay Word 2	Read/ Write	RSV=0, RSV=0, RSV=0, RSV=0, OffEn, C16OCNT10,C16OCNT9, C16OCNT8
07H (Table 10)	Set Delay Word 1	Read/ Write	C16OCNT7-0
08H	Reserved	Read/ Write	Set all bits to zero.
09H	Reserved	Read Only	
0AH	Reserved	Read Only	
0BH	Reserved	Read Only	
0CH	Reserved	Read Only	
0DH	Reserved	Read Only	
0EH	Reserved	Read Only	
0FH (Table 11)	Identification Word	Read Only	ID7-0
10H	Reserved	Read/ Write	Set all bits to zero.

Table 5. Register Map

Bit	Name	Functional Description
7	RSEL	**Reference Select**. A zero selects the PRI (primary) reference source as the input reference signal and a one selects the SEC (secondary) reference.
6 - 5	FS2-1	**Frequency Select 2 - 1**. These bits select which of four possible frequencies (8kHz, 1.544MHz, 2.048MHz or 19.44MHz) may be input to the PRI and SEC inputs. FS2 - 0, FS1 - 0 = 19.44 MHz FS2 - 0, FS1 - 1 = 8 kHz. FS2 - 1, FS1 - 0 = 1.544 MHz. FS2 - 1, FS1 - 1 = 2.048 MHz.
4 - 3	MS2-1	**Mode Select 2 - 1**: These bits select the PLL state of operation. MS2 - 0, MS1 - 0 = Normal. MS2 - 0, MS1 - 1 = Holdover. MS2 - 1, MS1 - 0 = Freerun. MS2 - 1, MS1 - 1 = Reserved.
2	SONET/$\overline{\text{SDH}}$	**SONET / SDH**. Set to one to move the loop filter corner frequency to 70 millihertz and limit the phase slope to 885 ns per second as per SONET requirements. Set to zero to move the corner frequency to 1.1 Hz and limit the phase slope to 53ns per 1.326ms.
1	FLOCK	**Fast Lock**. Set to one to allow the PLL to lock faster than normal to the input reference. During the time that FLOCK is one, the wander generation of the PLL is, of necessity, compromised. Set to zero for normal operation.
0	$\overline{\text{TCLR}}$	**TIE Clear**. Set to zero to clear the Time Interval Error correction circuit resulting in a realignment of output phase with input phase. When this bit is zero, the Time Interval Error correction circuit is disabled. When this bit is one, the Time Interval Error correction circuit will function normally.

Table 6. Control Register 1 (Address 00H - Read/Write)

Bit	Name	Functional Description
7	PRIOOR	**Primary Out Of Range**. A one indicates that the primary reference is off the PLL center frequency by more than 12 ppm. The measurement is done on a 1 second basis using a signal derived from the 20MHz clock input on C20i. When the accuracy of the 20MHz clock is $\pm$ 4.6ppm, the effective out of range limits of the PRIOOR signal will be +16.6ppm to -7.4ppm or +7.4ppm to -16.6ppm.
6	SECOOR	**Secondary Out of Range**. A one indicates that the secondary reference is off the PLL center frequency by more than 12 ppm. The measurement is done on a 1 second basis using a signal derived from the 20MHz clock input on C20i. When the accuracy of the 20MHz clock is $\pm$ 4.6ppm, the effective out of range limits of the PRIOOR signal will be +16.6ppm to -7.4ppm or +7.4ppm to -16.6ppm.
5	LOCK	**Lock**. This bit goes high when the PLL is in frequency lock to the input reference.
4	HOLDOVER	**Holdover**. This bit goes high whenever the device is in Holdover mode.
3	RSV	**Reserved.**
2	FLim	**Frequency Limit**. This bit goes high whenever the reference frequency hits the input frequency offset tolerance of the PLL. This bit can flicker high in the event of large excursions of still tolerable input jitter.
1-0	RSV	**Reserved.**

Table 7. Status Register 1 (Address 01H - Read Only)

Bit	Name	Functional Description
7	E3DS3/$\overline{OC3}$	**E3DS3/$\overline{OC3}$ Selection.** Set this bit to zero to enable the differential 155.52 MHz output clock on the C155N/C155P pins and cause the C34/C44 pin to output its nominal clock frequency divided by 4. Set this bit to one to disable the differential 155.52 MHz output clock on the C155N/C155P pins and cause the C34/C44 pin to output its nominal clock frequency.
6	E3/$\overline{DS3}$	**E3/$\overline{DS3}$.** Set this bit low to select a clock rate of 44.736 MHz for the C34/C44 pin. Set high to select a clock rate of 34.368 MHz for the C34/C44 pins.
5-0	RSV	**Reserved**. Set to zero for normal operation.

Table 8. Control Register 2 (Address 04H - Read/Write)

Bit	Name	Functional Description
7-4	RSV	**Reserved.** Set to zero.
3	OffEn	**Offset Enable.** Set high to enable a programmed phase shift between the input reference and the generated clocks.
2 - 0	C16OCNT10-8	**C16 Offset Count.** The three most significant bits of the offset delay word. These bits program the offset all clocks derived from 16.384 MHz with respect to the input reference in step sizes of 60 nS.

Table 9. Set Delay Word 2 (Address 06H - Read/Write)

Bit	Name	Functional Description
7 - 0	C16OCNT 7-0	**C16 Offset Count**. The eight least significant bits of the offset delay word. These bits program the offset of all clocks derived from 16.384 MHz with respect to the input reference in step sizes of 60 nS.

Table 10. Set Delay Word 1 (Address 07H - Read/Write)

Bit	Name	Functional Description
7- 0	ID7-0	**Identification Word 7-0**. These bits contain the revision number of the part.

Table 11. Identification Word (Address 0FH - Read Only)

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	Supply voltage	V_{DDR}	-0.3	7.0	V
2	Voltage on any pin	V_{PIN}	-0.3	V_{DD}+0.3	V
3	Current on any pin	I_{PIN}		30	mA
4	Storage temperature	T_{ST}	-55	125	°C
5	80 LQFP package power dissipation	P_{PD}		1000	mW

* Voltages are with respect to ground (V_{SS}) unless otherwise stated.
* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions*

	Characteristics	Sym	Min	Typ	Max	Units
1	Supply voltage	V_{DD}	3.0	3.3	3.6	V
2	Operating temperature	T_A	-40	25	+85	$^o{}^0C$

* Voltages are with respect to ground (V_{SS}) unless otherwise stated.

DC Electrical Characteristics*

	Characteristics	Sym	Min	Max	Units	Conditions/Notes
1	Supply current with C20i = 0V	I_{DDS}		2	mA	Outputs unloaded
2	Supply current with C20i = 20MHz	I_{DD}		150	mA	Outputs unloaded
3	CMOS high-level input voltage	V_{CIH}	$0.7V_{DD}$		V	
4	CMOS low-level input voltage	V_{CIL}		$0.3V_{DD}$	V	
5	Input leakage current	I_{IL}		15	μA	$V_I = V_{DD}$ or 0V
6	High-level output voltage	V_{OH}	2.4		V	I_{OH}= 10 mA
7	Low-level output voltage	V_{OL}		0.4	V	I_{OL}= 10 mA
8	LVDS Differential Output Voltage	V_{OD}	250	460	mV	Z_T = 100 Ω
9	LVDS Change in V_{OD} between complementary output states	dV_{OD}		40	mV	
10	LVDS Offset Voltage	V_{OS}	1.15	1.35	V	
11	LVDS Change in V_{OS} between complementary output states	dV_{OS}		40	mV	
12	LVDS Output short circuit current	I_{OS}		20	mA	V_{CI55P} = 0 or V_{C155N} = 0
13	LVDS Output Rise/Fall Times	T_{RF}	300	600	ps	Measured at 20% and 80%

* Voltages are with respect to ground (V_{SS}) unless otherwise stated.
* Supply voltage and operating temperature are as per Recommended Operating Conditions.

AC Electrical Characteristics - Timing Parameter Measurement Voltage Levels*

	Characteristics	Sym	CMOS	Units
1	Threshold Voltage	V_T	$0.5V_{DD}$	V
2	Rise and Fall Threshold Voltage High	V_{HM}	$0.7V_{DD}$	V
3	Rise and Fall Threshold Voltage Low	V_{LM}	$0.3V_{DD}$	V

* Voltages are with respect to ground (V_{SS}) unless otherwise stated.
* Supply voltage and operating temperature are as per Recommended Operating Conditions.
* Timing for input and output signals is based on the worst case
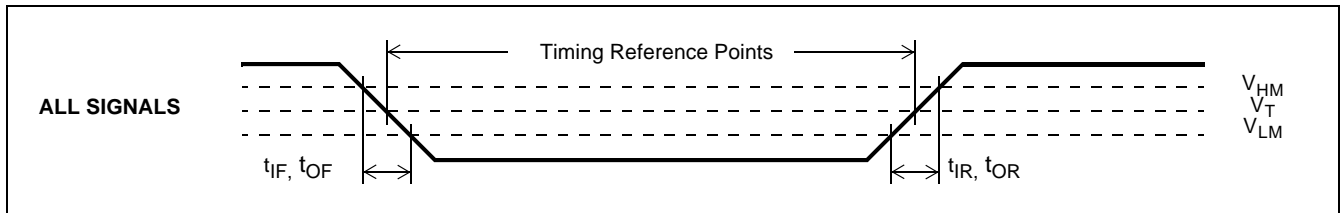
Figure 14 - Timing Parameter Measurement Voltage Levels

AC Electrical Characteristics - Microprocessor Timing*

	Characteristics	Sym	Min	Max	Units	Test Conditions
1	$\overline{DS}$ low	t_{DSL}	30		ns	
2	$\overline{DS}$ High	t_{DSH}	30		ns	
3	$\overline{CS}$ Setup	t_{CSS}	0		ns	
4	R/$\overline{W}$ Setup	t_{RWS}	18		ns	
5	Address Setup	t_{ADS}	0		ns	
6	$\overline{CS}$ Hold	t_{CSH}	0		ns	
7	R/$\overline{W}$ Hold	t_{RWH}	4		ns	
8	Address Hold	t_{ADH}	10		ns	
9	Data Delay Read	t_{DDR}		50	ns	C_L=150pF
10	Data Hold Read	t_{DHR}		30	ns	
11	Data Setup Write	t_{DSW}	0		ns	
12	Data Hold Write	t_{DHW}	10		ns	

* Supply voltage and operating temperature are as per Recommended Operating Conditions.
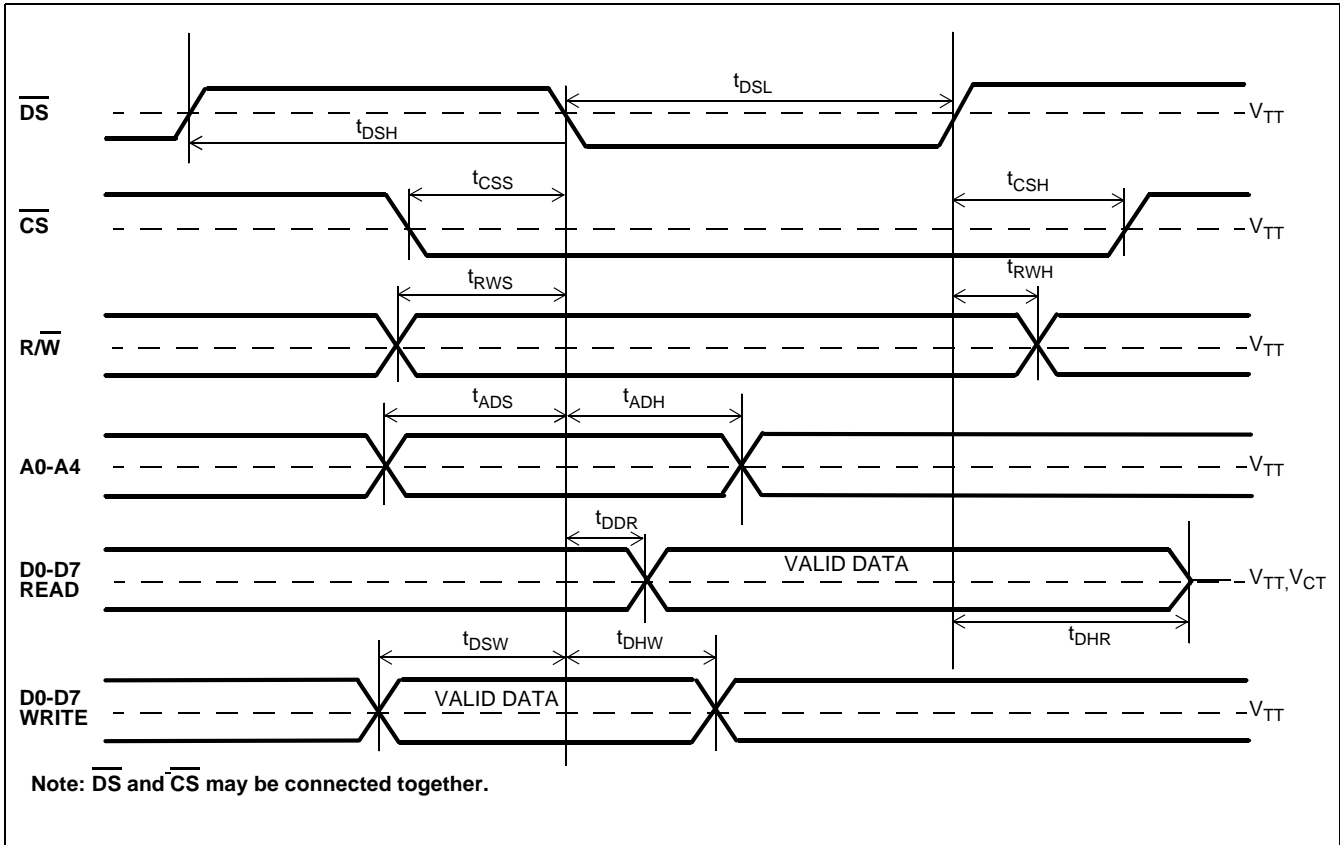
Figure 15 - Microport Timing

NOTES:

1. Input to output delay values are valid after a
$\overline{TCLR}$ or $\overline{RST}$ with no further state changes
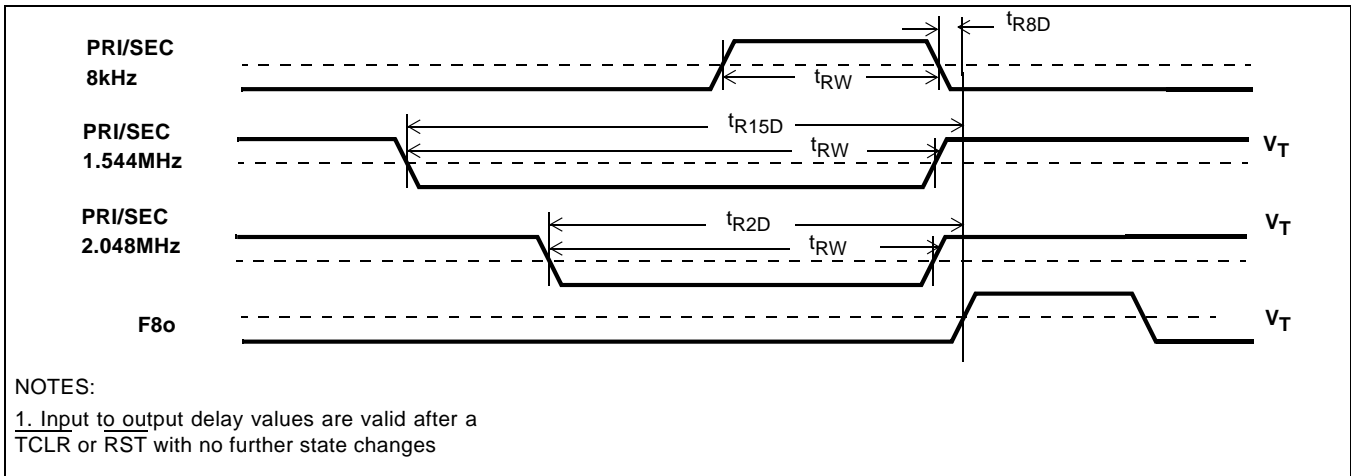
Figure 16 - Input to Output Timing for T1/E1 signals (Normal Mode)
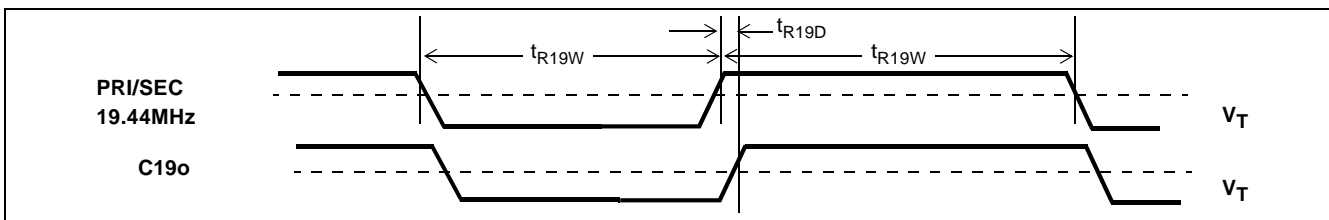
Figure 17 - Input to Output Timing for 19.44MHz Signal (Normal Mode)

AC Electrical Characteristics - Output Timing*

	Characteristics	Sym	Min	Max	Units	Conditions/Notes†
1	Reference input pulse width high or low (8KHz, 1.544MHz, 2.048MHz)	t_{RW}	100		ns	
2	Reference input pulse width high or low (19.4MHz)	t_{R19W}	10		ns	
3	Reference input rise or fall time	t_{IR}, t_{IF}		10	ns	
4	8kHz reference input to F8o delay	t_{R8D}	-85	-65	ns	
5	1.544MHz reference input to F8o delay	t_{R15D}	400	425	ns	
6	2.048MHz reference input to F8o delay	t_{R2D}	220	230	ns	
7	19.44MHz reference input to C19o delay	t_{R19D}	38	42	ns	
8	F8o to $\overline{F0o}$ delay	t_{F0D}	115	125	ns	
9	F8o to $\overline{F16o}$ delay	t_{F16D}	23	35	ns	
10	F8o to C1.5o delay	t_{C15D}	-100	-85	ns	
11	F8o to C6o delay	t_{C6D}	58	70	ns	
12	F8o to C2o delay	t_{C2D}	-6	5	ns	
13	F8o to $\overline{C4o}$ delay	t_{C4D}	-6	5	ns	
14	F8o to C8o delay	t_{C8D}	-6	5	ns	
15	F8o to $\overline{C16o}$ delay	t_{C16D}	-6	5	ns	
16	C1.5o pulse width high or low	t_{C15W}	315		ns	
17	C6o pulse width high or low	t_{C6W}	70		ns	
18	C2o pulse width high or low	t_{C2W}	235		ns	
19	$\overline{C4o}$ pulse width high or low	t_{C4W}	115		ns	
20	C8o pulse width high or low	t_{C8W}	53		ns	
21	$\overline{C16o}$ pulse width high or low	t_{C16W}	24		ns	
22	C19o pulse width high or low	t_{C19W}	9		ns	
23	C19o to c155 delay	t_{C155D}	0	6	ns	
24	$\overline{F0o}$ pulse width low	t_{F0WL}	235	250	ns	
25	F8o pulse width high	t_{F8WH}	115	130	ns	
26	$\overline{F16o}$ pulse width low	t_{F16WL}	55	63	ns	
27	Output clock and frame pulse rise or fall time	t_{OR}, t_{OF}		9	ns	
28	Input Controls Setup Time	t_S	100		ns	
29	Input Controls Hold Time	t_H	100		ns	
30	C34o Pulse width low or high	t_{C34W}	9		ns	
31	C44o Pulse width low or high	t_{C44W}	6		ns	
32	C8.5o Pulse width low	$t_{C8.5WL}$		106	ns	
33	C11o Pulse width low	t_{C11WL}		81	ns	

* Supply voltage and operating temperature are as per Recommended Operating Conditions
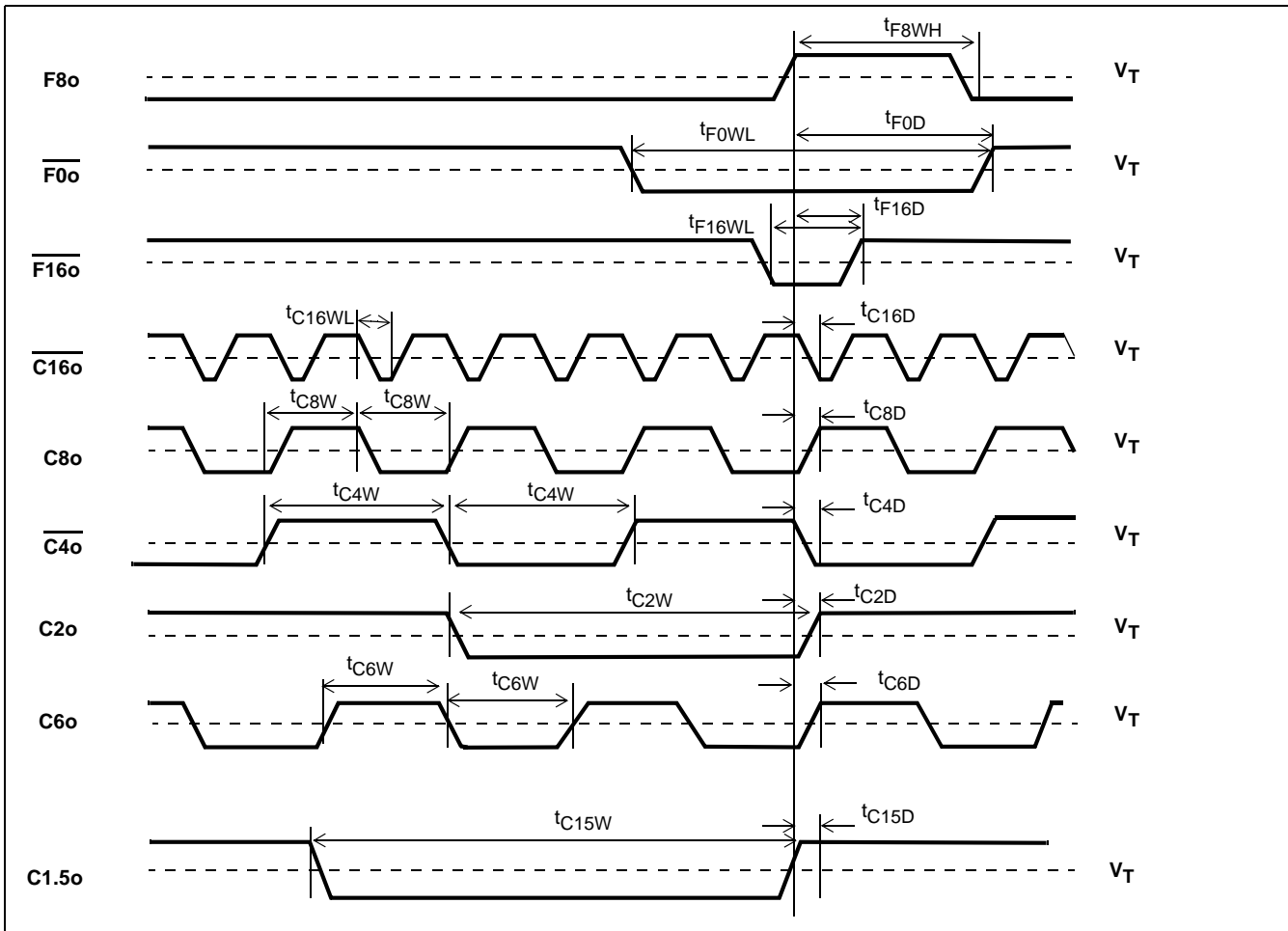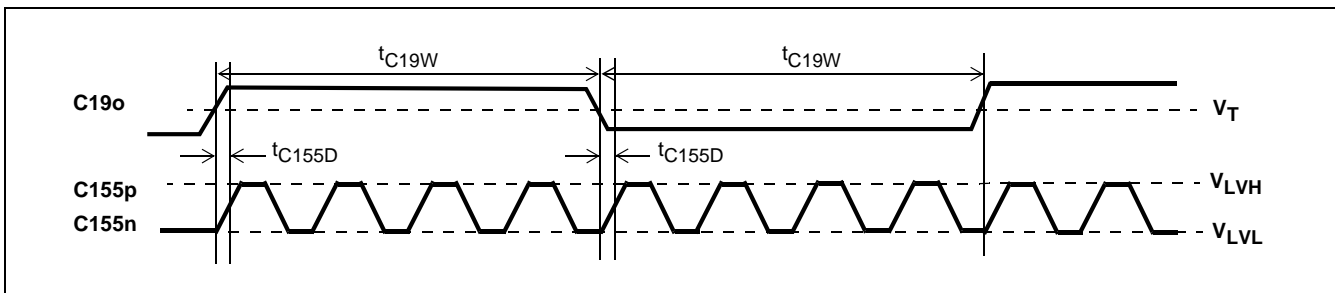
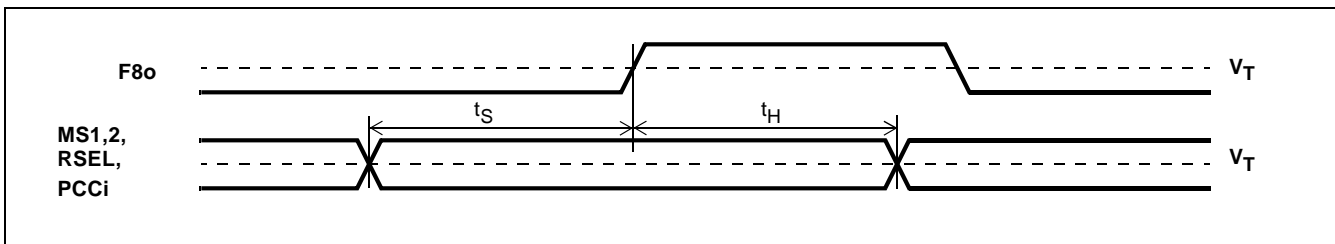**Figure 18 - Output Timing 1**

Figure 19 - Output Timing 2

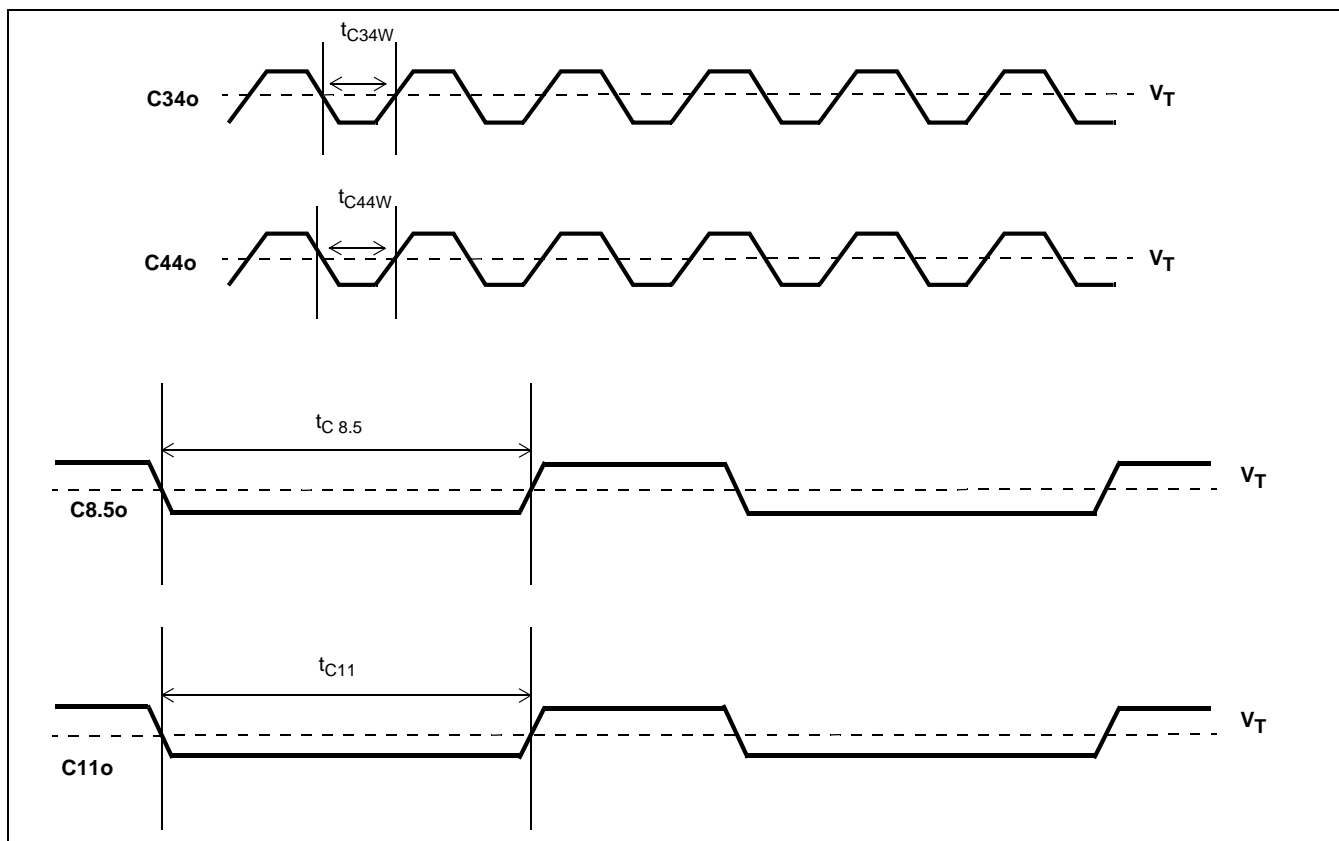**Figure 20 - Input Controls setup and Hold Timing**

Figure 21 - Output Timing 3

AC Electrical Characteristics - C20i Master Clock Input*

	Characteristics	Sym	Min	Max	Units	Conditions/Notes†
1	Duty cycle		40	60	%	
2	Rise time			10	ns	
3	Fall time			10	ns	

* Supply voltage and operating temperature are as per Recommended Operating Conditions.

Performance Characteristics: Mode Switching*

		Characteristics		Min	Typ	Max	Units	Conditions/Notes†
1	Holdover Mode accuracy with C20i at:		0ppm	-0.02		+0.02	ppm	
2			20ppm	-0.02		+0.02	ppm	
3	Capture range with C20i at:		0ppm	-52		+52	ppm	
4			20ppm	-32		+32	ppm	
5	Phase lock time				100		s	4.6ppm frequency offset
6	Output phase continuity with:	reference switch			200		ns	
7		mode switch to Normal			200		ns	
8		mode switch to Freerun			200		ns	
9		mode switch to Holdover			50		ns	
10	Output phase slope - SDH mode	- SONET mode				40 885	us/s ns/s	53ns per 1.326ms
11	Reference input for Auto-Holdover with:	8kHz		-30k		+30k	ppm	
12		1.544MHz		-30k		+30k	ppm	
13		2.048MHz		-30k		+30k	ppm	
14		19.44MHz		-30k		+30k	ppm	

* Supply voltage and operating temperature are as per Recommended Operating Conditions.

Performance Characteristics: Output Jitter Generation - Filtered

	Characteristics	MAX UIpp	MAX ns-pp	Notes
1	Intrinsic jitter at C1.5o (1.544MHz)	0.004	2.76	Filter: 10Hz - 40kHz
2	Intrinsic jitter at C2o (2.048MHz)	0.004	1.83	Filter: 20Hz - 100kHz
3	Intrinsic jitter at C19o (19.44MHz)	0.100	5.20	Filter: 500Hz - 1.3MHz OC-3
4	Intrinsic jitter at C19o (19.44MHz)	0.100	5.16	Filter: 65kHz - 1.3MHz OC-3
5	Intrinsic jitter at C34o (34.368MHz)	0.044	1.30	Filter: 100Hz - 800kHz
6	Intrinsic jitter at C34o (34.368MHz)	0.039	1.15	Filter: 10kHz - 800kHz
7	Intrinsic jitter at C44o (44.736MHz)	0.044	0.99	Filter: 10Hz - 400kHz
8	Intrinsic jitter at C44o (44.736MHz)	0.037	0.82	Filter: 30kHz - 400kHz

* Supply voltage and operating temperature are as per Recommended Operating Conditions.

Performance Characteristics: Output Jitter Generation - Filtered

(V_{DD} = 3.3V +/- 10%, T_{A} = -5°C to +85°C)

	Characteristics	MAX UIpp	MAX ns-pp	Notes
1	Intrinsic jitter at C155o (155.52MHz)	0.12	0.76	Filter: 100Hz - 400kHz OC-1
2	Intrinsic jitter at C155o (155.52MHz)	0.11	0.69	Filter: 20kHz - 400kHz OC-1
3	Intrinsic jitter at C155o (155.52MHz)	0.18	1.13	Filter: 500Hz - 1.3MHz OC-3
4	Intrinsic jitter at C155o (155.52MHz)	0.13	0.83	Filter: 65kHz - 1.3MHz OC-3

.

Performance Characteristics: Output Jitter Generation - Unfiltered*

	Characteristics	Sym	MAX : UIpp	MAX : nspp	Notes
1	Intrinsic jitter at C1.5o (1.544MHz)		0.010	6.5	
2	Intrinsic jitter at C2o (2.048MHz)		0.012	5.8	
3	Intrinsic jitter at C4o (4.096MHz)		0.027	6.5	
4	Intrinsic jitter at C6o (6.312MHz)		0.037	5.8	
5	Intrinsic jitter at C8o (8.192MHz)		0.048	5.9	
6	Intrinsic jitter at C8.5o (8.592MHz)		0.032	3.8	
7	Intrinsic jitter at C11o (11.184MHz)		0.036	3.2	
8	Intrinsic jitter at C16o (16.384MHz)		0.096	5.8	
9	Intrinsic jitter at C19o (19.44MHz)		0.11	5.6	
10	Intrinsic jitter at C34o (34.368MHz)		0.12	3.5	
11	Intrinsic jitter at C44o (44.736MHz)		0.12	2.6	
12	Intrinsic jitter at C155o (155.52MHz)		0.21	1.3	
13	Intrinsic jitter at F0o (8kHz)		NA	4.7	
14	Intrinsic jitter at F8o (8kHz)		NA	4.0	
15	Intrinsic jitter at F16o (8kHz)		NA	3.1	

* Supply voltage and operating temperature are as per Recommended Operating Conditions.
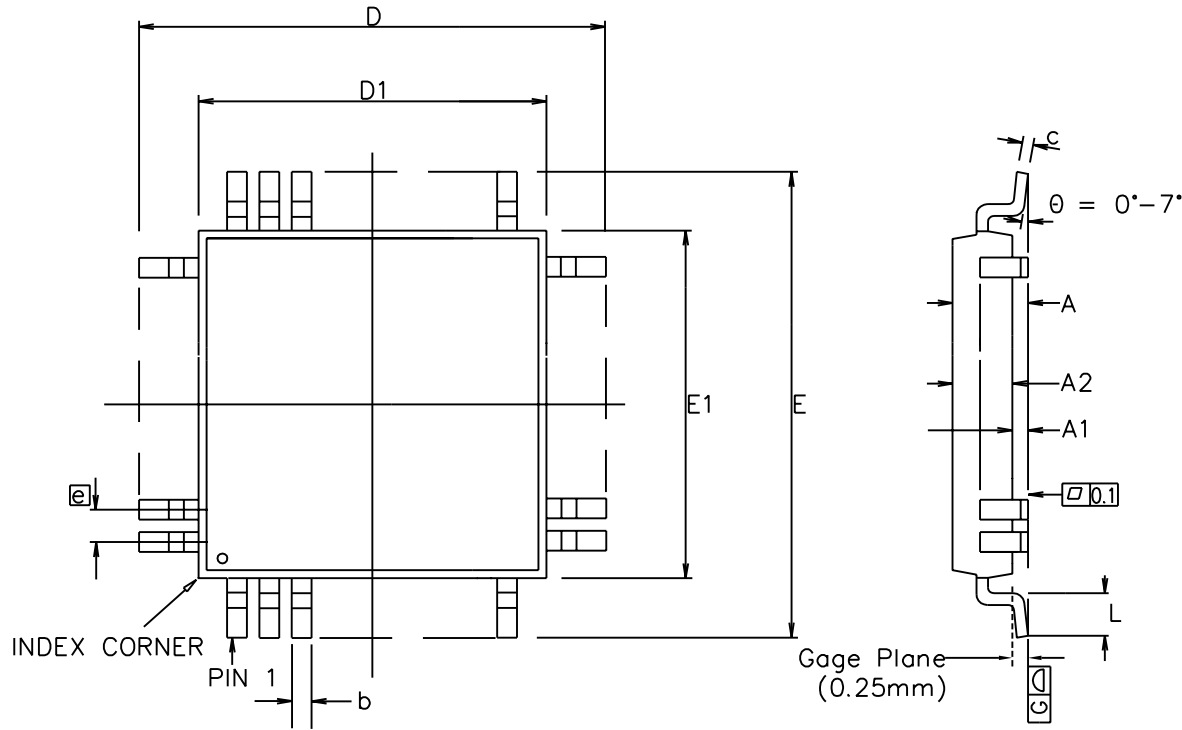
Symbol	Control Dimensions in millimetres		Altern. Dimensions in inches	
	MIN	MAX	MIN	MAX
A	— — —	1.60	0.002	0.063
A1	0.05	0.15	0.010	0.006
A2	1.35	1.45	0.053	0.057
D	16.00 BSC		0.630 BSC	
D1	14.00 BSC		0.551 BSC	
E	16.00 BSC		0.630 BSC	
E1	14.00 BSC		0.551 BSC	
L	0.45	0.75	0.018	0.030
e	0.65 BSC		0.026 BSC	
b	0.22	0.38	0.009	0.015
c	0.09	0.20	0.004	0.008
Pin features				
N	80			
ND	20			
NE	20			
NOTE	SQUARE			

Conforms to JEDEC MS−026 BEC Iss. C

Θ = 0°−7°

Gage Plane (0.25mm)

INDEX CORNER

PIN 1

Notes:
1. Pin 1 indicator may be a corner chamfer, dot or both.
2. Controlling dimensions are in millimeters.
3. The top package body size may be smaller than the bottom package body size by a max. of 0.15 mm.
4. Dimension D1 and E1 do not include mould prorusion.
5. Dimension b does not include dambar protusion.
6. Coplanarity, measured at seating plane G, to be 0.10 mm max.

This drawing supersedes 418/ED/51210/024 (Swindon)

ISSUE	1	2	3	
ACN	201363	207143	212836	
DATE	28Oct96	14Jul99	21May02	
APPRD.				

ZARLINK
SEMICONDUCTOR

Previous package codes
GP / B

Package Code   QC

Package Outline for 80 lead LQFP (14 x 14 x 1.4mm) 2.0mm Footprint

GPD00247

ZARLINK
SEMICONDUCTOR

**For more information about all Zarlink products
visit our Web Site at**

www.zarlink.com

TECHNICAL DOCUMENTATION - NOT FOR RESALE