OKI Semiconductor

This version: Jan. 1998
Previous version: Nov. 1996

MSM65524A/65P524

8-Bit Microcontroller with A/D Converter

GENERAL DESCRIPTION

The MSM65524A is a high-performance 8-bit microcontroller that employs OKI original nX-8/50 CPU core. With a minimum instruction execution time of 400 ns (10MHz clock), the MSM65524A is capable of high-speed processing, and includes 16K bytes of program memory, 384 bytes of data memory, timers, serial ports, an A/D converter and PWMs on chip. Also available are the MSM65P524, which replaces the on-chip program memory with one-time PROM, and the MSM65X524A, which uses the external program memory.

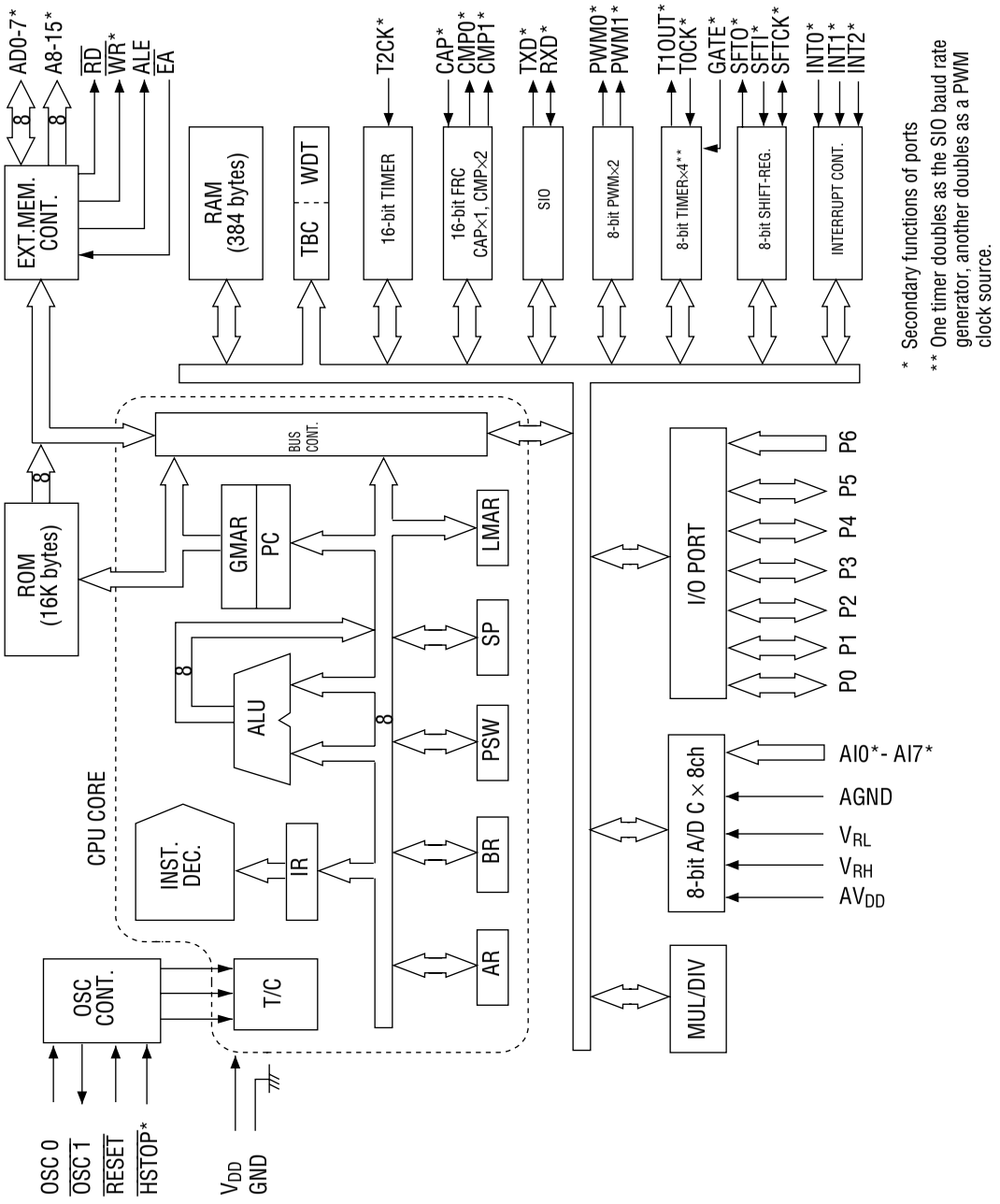
FEATURES

- Operating range
  - Operating frequency : 0 to 10MHz (V_{DD}=4.5 to 5.5V)
    0 to 5MHz (V_{DD}=2.7 to 5.5V)
  - Operating voltage : 2.7 to 5.5V
  - Operating temperature : –40 to +85°C
- Memory space : 64K bytes
  - Internal program memory : 16K bytes
  - Internal data memory : 384 bytes
- Minimum instruction execution time : 400ns @ 10 MHz
- Powerful instruction set : 83 basic instructions
  8/16-bit operation instructions
  Bit manipulation instructions
  Compound function instructions
- Abundant addressing modes
- Multiplication/division operation functions : 8 × 8 → 16
  16 ÷ 8 → 16 ... 8
- I/O port
  - Input-output port : 5 ports × 8 bits
    1 port × 4 bits
  - Input port : 1 port × 8 bits
- Timers : 8-bit auto-reload timer × 2
  16-bit auto-reload timer × 1
  Watchdog timer × 1
- Counters : Time base counter × 1
  16-bit free-running counter × 1
- Capture input : 1 channel
- Compare output : 2 channels
- Serial ports : Shift register × 1
  Serial port with baud rate generator (UART/Synchronous) × 1
- A/D converter : 8 bits × 8 channels
- PWM : 8 bits × 2 channels
  PWM with auto-reload timer for period setting

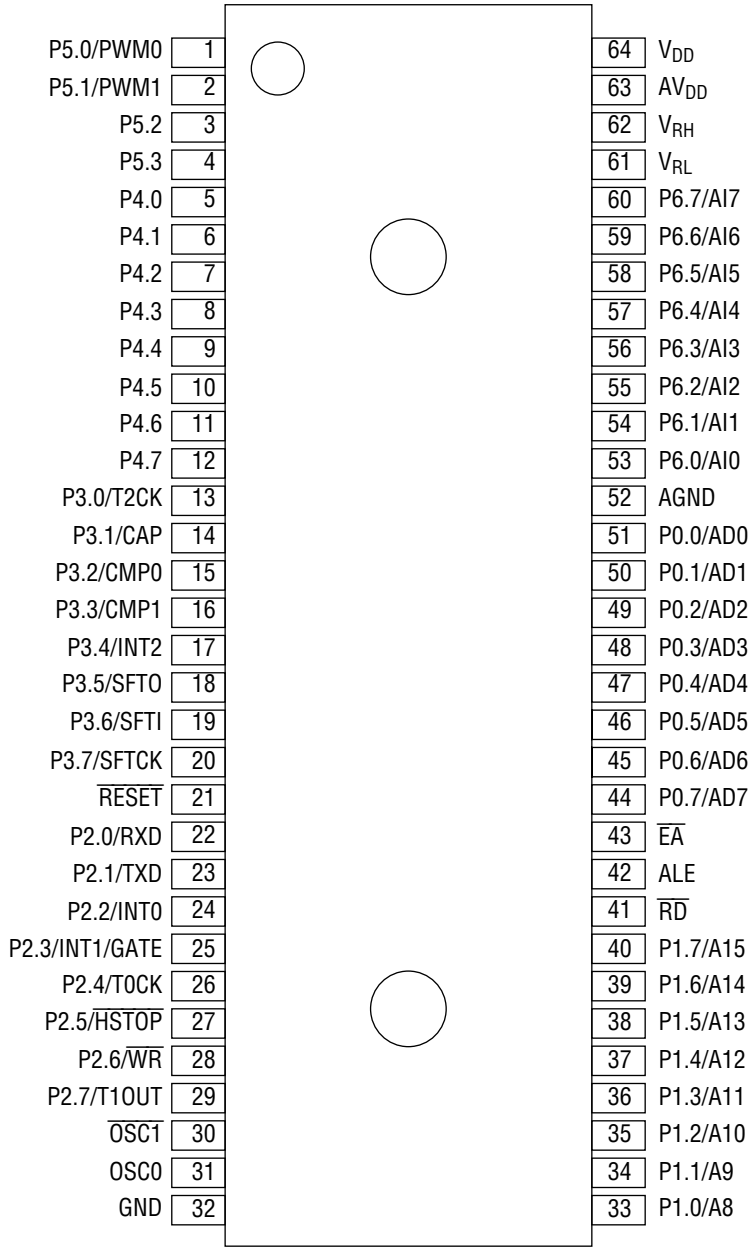
- External interrupts : 3
- Interrupt sources : 19
- Package options
  - 64-pin plastic shrink DIP (SDIP64-P-750-1.78) : (Product name: MSM65524A-×××SS, MSM65P524-×××SS)
  - 64-pin plastic QFP (QFP64-P-1414-0.80-BK) : (Product name: MSM65524A-×××GS-BK, MSM65P524-×××GS-BK)
  - 68-pin plastic QFJ (PLCC) (QFJ68-P-S950-1.27) : (Product name: MSM65524A-×××JS, MSM65P524-×××JS)

  ××× indicates the code number.

BLOCK DIAGRAM

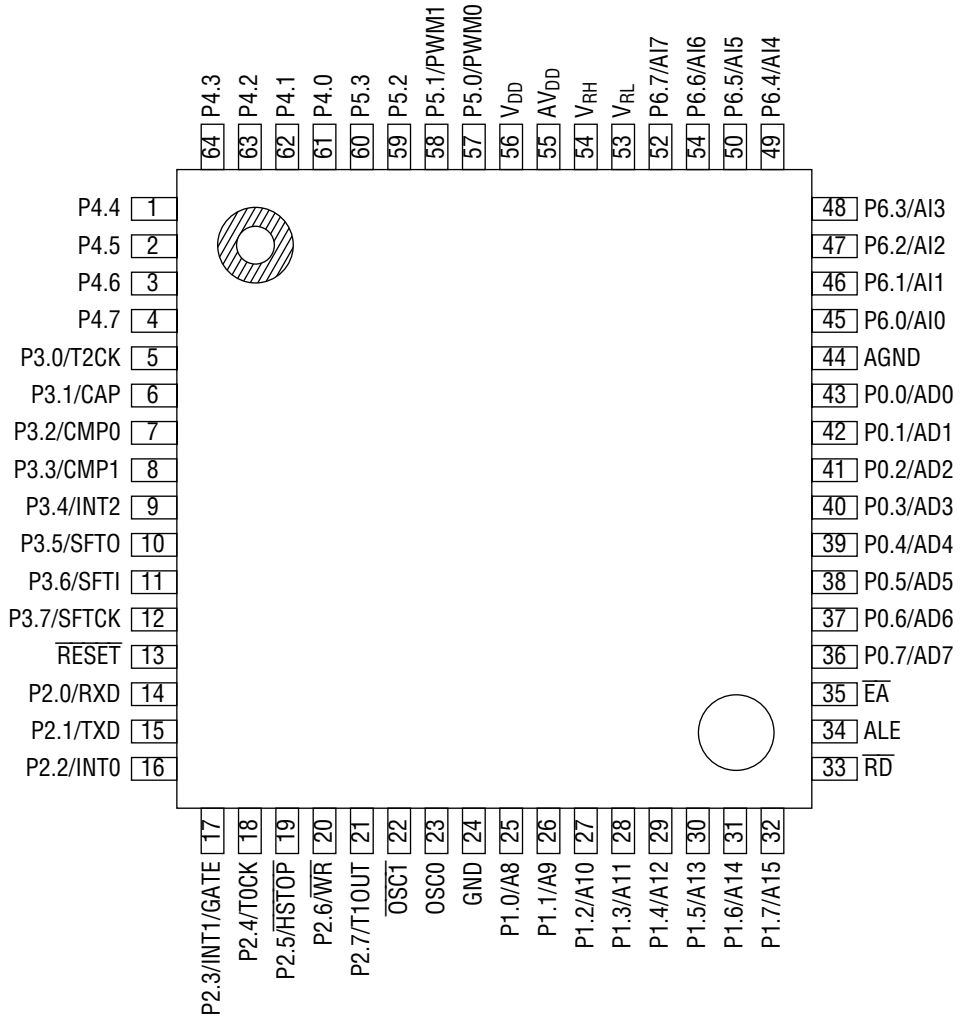


PIN CONFIGURATION (TOP VIEW)



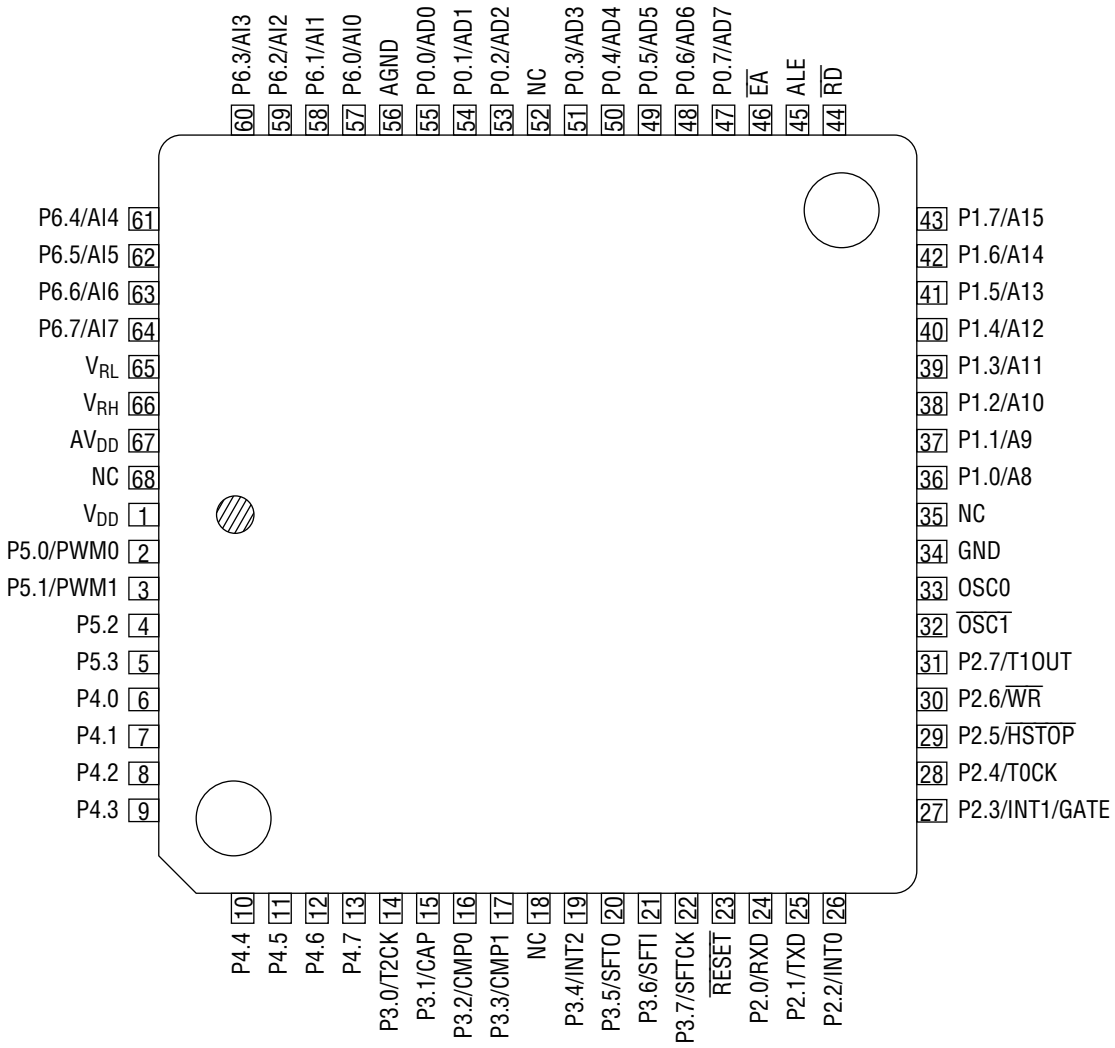
64-Pin Plastic Shrink DIP

PIN CONFIGURATION (TOP VIEW) (Continued)



64-Pin Plastic QFP

PIN CONFIGURATION (TOP VIEW) (Continued)



NC: No-connection pin

68-Pin Plastic QFJ (PLCC)

PIN DESCRIPTION

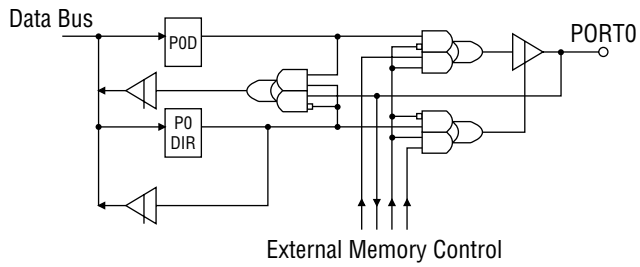
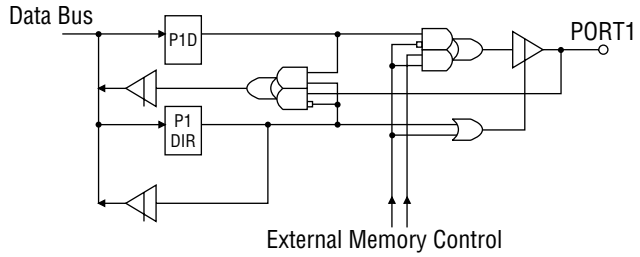
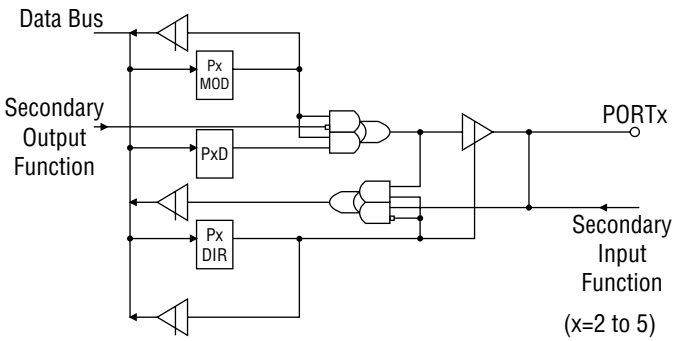
Basic Functions

Function	Symbol	Type	Description
Power Supply	V_{DD}	—	+5V digital power supply
	GND	—	0V digital ground
	AV_{DD}	—	+5V analog power supply
	AGND	—	0V analog ground
	V_{RH}	—	+5V analog reference voltage
	V_{RL}	—	0V analog reference voltage
Oscillation	OSC0	I	System clock input pin. Quartz oscillator or ceramic oscillator is connected between OSC0 and $\overline{OSC1}$. For external clock, input at OSC0, leaving $\overline{OSC1}$ open.
	$\overline{OSC1}$	O	System clock output pin
Control	$\overline{RESET}$	I	System reset input (program starts from address 0040H); internal pull-up resistance
	$\overline{EA}$	I	Program memory select input pin. "L" level input for external program memory; "H" level input for internal program memory.
	$\overline{RD}$	O	Read strobe signal during external memory access
	ALE	O	Address latch signal during external memory access
Port	PORT 0	I/O	8-bit Input-output port During external memory access, becomes address/data bus for address output, instruction fetch or data read/write along with ALE, $\overline{RD}$ and $\overline{WR}$ pins.
	PORT 1	I/O	8-bit Input-output port Address bus during external memory access
	PORT 2 PORT 3 PORT 4	I/O	8-bit Input-output port × 3. Secondary functions shown in following table are added for ports 2 and 3.
	PORT 5	I/O	4-bit Input-output port Secondary functions shown in following table are added for port 5.
	PORT 6	I	8-bit Input port Functions as analog input channel during A/D conversion.

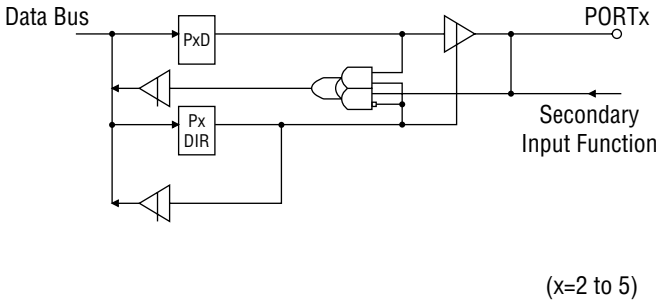
Secondary Functions

Symbol	Type	Description
RXD	I/O	P2.0 secondary function UART: Input pin for serial port receive data. Synchronous: Input/output pin for serial port transmit/receive data.
TXD	O	P2.1 secondary function UART: Output pin for serial port transmit data. Synchronous: Output pin for serial port synchronizing clock.
INT0	I	P2.2 secondary function External interrupt 0 input pin.
INT1/GATE	I	P2.3 secondary functions External interrupt 1 input pin. Also used as input pin for gate signal for timer 0 count enable/disable.
T0CK	I	P2.4 secondary function Timer 0 external clock input pin.
$\overline{\text{HSTOP}}$	I	P2.5 secondary function Hard stop mode input pin; stops system clock oscillation with "L" level input.
$\overline{\text{WR}}$	O	P2.6 secondary function Write strobe signal output pin during external data memory access.
T1OUT	O	P2.7 secondary function Output pin for signal that 2-divided timer 1 overflow.
T2CK	I	P3.0 secondary function Timer 2 external clock input pin.
CAP	I	P3.1 secondary function Capture trigger input pin.
CMP0	O	P3.2 secondary function Compare output channel 0 output pin.
CMP1	O	P3.3 secondary function Compare output channel 1 output pin.
INT2	I	P3.4 secondary function External interrupt 2 input signal.
SFTO	O	P3.5 secondary function Shift register data output pin.
SFTI	I	P3.6 secondary function Shift register data input pin.
SFTCK	I/O	P3.7 secondary function Shift register synchronizing clock input/output pin.
PWM0	O	P5.0 secondary function PWM channel 0 output pin.
PWM1	O	P5.1 secondary function PWM channel 1 output pin.

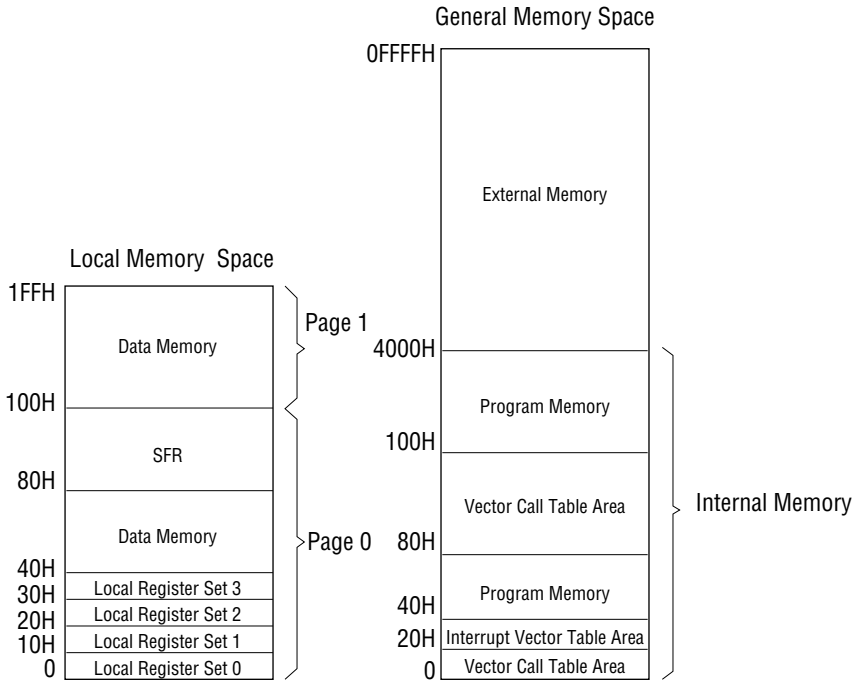
Port Circuit Configuration

Type	Port	Circuit Configuration	Electrical Characteristics (V_{DD}=5V)
1	P0.0/AD0 to P0.7/AD7		"H" Input Voltage: • V_{IH}=2.4V "L" Input Voltage: • V_{IL}=0.8V "H" Output Voltage: • V_{OH}=3.75V • I_{OH}=–400µA "L" Output Voltage: • V_{OL}=0.4V • I_{OL}=3.2mA
2	P1.0/A8 to P1.7/A15		"H" Input Voltage: • V_{IH}=2.4V "L" Input Voltage: • V_{IL}=0.8V "H" Output Voltage: • V_{OH}=3.75V • I_{OH}=–200µA "L" Output Voltage: • V_{OL}=0.4V • I_{OL}=1.6mA
3	P2.0/RXD, P2.1/TXD, P2.6/$\overline{WR}$, P2.7/T1OUT, P3.2/CMP0, P3.3/CMP1, P3.5/SFTO, P3.7/SFTCK, P5.0/PWM0, P5.1/PMW1		"H" Input Voltage: • V_{IH}=2.4V "L" Input Voltage: • V_{IL}=0.8V P2.6/$\overline{WR}$ "H" Output Voltage: • V_{OH}=3.75V • I_{OH}=–400µA "L" Output Voltage: • V_{OL}=0.4V • I_{OL}=3.2mA Ports other than P2.6/$\overline{WR}$ "H" Output Voltage: • V_{OH}=3.75V • I_{OH}=–200µA "L" Output Voltage: • V_{OL}=0.4V • I_{OL}=1.6mA

Port Circuit Configuration (Continued)

Type	Port	Circuit Configuration	Electrical Characteristics (V_{DD}=5V)
4	P2.2/INT0, P2.3/INT1/GATE, P2.4/T0CK, P2.5/$\overline{\text{HSTOP}}$, P3.0/T2CK, P3.1/CAP, P3.4/INT2, P3.6/SFTI, P4.0 to P4.7, P5.2 to P5.3		"H" Input Voltage: • V_{IH}=2.4V "L" Input Voltage: • V_{IL}=0.8V "H" Output Voltage: • V_{OH}=3.75V • I_{OH}=–200µA "L" Output Voltage: • V_{OL}=0.4V • I_{OL}=1.6mA
5	P6.0/AI0 to P6.7/AI7		"H" Input Voltage: • V_{IH}=2.4V "L" Input Voltage: • V_{IL}=0.8V

MEMORY MAPS


General Memory Space
0FFFFH
External Memory
4000H
Program Memory
100H
Vector Call Table Area
80H
Program Memory
40H
Interrupt Vector Table Area
20H
Vector Call Table Area
0
Internal Memory
Local Memory Space
1FFH
Data Memory
100H
SFR
80H
Data Memory
40H
Local Register Set 3
30H
Local Register Set 2
20H
Local Register Set 1
10H
Local Register Set 0
0
Page 1
Page 0

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	V_{DD}=AV_{DD}	Ta=25°C GND=AGND=0V	–0.3 to 7.0	V
Input Voltage	V_I		–0.3 to V_{DD}+0.3	
Output Voltage	V_O		–0.3 to V_{DD}+0.3	
Analog Reference Voltage	V_{RH}, V_{RL}		–0.3 to V_{DD}+0.3	
Analog Input Voltage	V_{AI}		–0.3 to V_{DD}+0.3	
Power Dissipation	P_D	Ta=25°C per package	400	mW
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Supply Voltage	V_{DD}	Refer to Figure 1.	2.7 to 5.5	V
Analog Supply Voltage	AV_{DD}	V_{DD}=AV_{DD}=V_{RH}	2.7 to 5.5	
Analog Reference Voltage	V_{RH}	GND=AGND=V_{RL}=0V	2.7 to 5.5	
Analog Input Voltage	V_{AI}		0 to V_{DD}	
Memory Hold Voltage	V_{DDMH}	f_{OSC}=0 Hz	2.0 to 5.5	
Operating Frequency *1	f_{OSC}	Refer to Figure 1.	1 to 10	MHz
External Clock Operating Frequency	f_{EXTCLK}	Refer to Figure 1.	0 to 10	MHz
Operating Temperature	T_{op}	—	–40 to +85	°C

*1 This is due to the standard of a crystal oscillator or resonator.

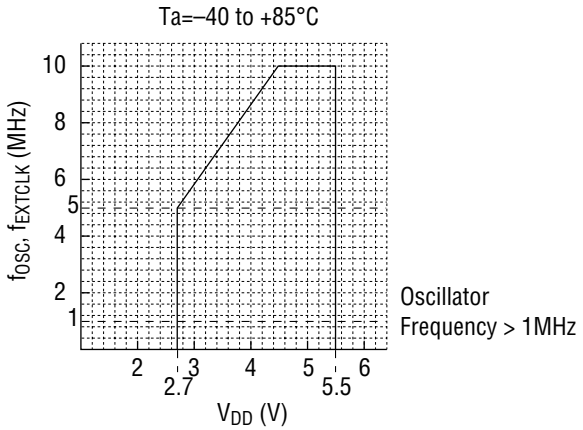


Figure 1. Power Supply Voltage vs. Operating Frequency

ELECTRICAL CHARACTERISTICS

DC Characteristics 1 (V_{DD}=4.5 to 5.5V)

(GND=0V, Ta=–40 to +85°C)

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage 1	*1	V_{IH1}	—	2.4	—	V_{DD}+0.3	V
"H" Input Voltage 2	*2	V_{IH2}	—	0.7V_{DD}	—	V_{DD}+0.3	
"L" Input Voltage		V_{IL}	—	–0.3	—	0.8	
"H" Output Voltage 1	*3	V_{OH1}	I_{OH}=–200µA	0.75V_{DD}	—	—	
"H" Output Voltage 2	*4	V_{OH2}	I_{OH}=–400µA	0.75V_{DD}	—	—	
"L" Output Voltage 1	*3	V_{OL1}	I_{OL}=1.6mA	—	—	0.4	
"L" Output Voltage 2	*4	V_{OL2}	I_{OL}=3.2mA	—	—	0.4	
Input Leakage Current 1	*5	I_{LI1}	V_I=V_{DD}/0V	—	—	±1	µA
Input Leakage Current 2	*6	I_{LI2}	V_I=V_{DD}/0V	—	—	±10	
"L" Input Current	*7	I_{IL}	V_I=0V	–40	–120	–400	
Input Capacitance		C_I	f=1MHz, Ta=25°C	—	5	—	pF
Static Current Consumption		I_{DDS}	5V, stop mode *8	—	—	50	µA
Dynamic Current Consumption		I_{DD}	10MHz, 5V, no load Refer to Figure2	—	20	40	mA

*1 Excluding OSC0 and $\overline{\text{RESET}}$
*2 OSC0 and $\overline{\text{RESET}}$
*3 Excluding P0, ALE, $\overline{\text{RD}}$, P2.6/$\overline{\text{WR}}$
*4 P0, ALE, $\overline{\text{RD}}$, P2.6/$\overline{\text{WR}}$
*5 $\overline{\text{EA}}$, P6
*6 Excluding $\overline{\text{RESET}}$, $\overline{\text{EA}}$, P6
*7 $\overline{\text{RESET}}$
*8 The ports set for input mode are V_{DD} or 0V and the ports except these are no load.

DC Characteristics 2 ($2.7 \leq V_{DD} < 4.5V$)

(GND=0V, Ta=–40 to +85°C)

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage 1	*1	V_{IH1}	—	$0.5V_{DD}+0.2$	—	$V_{DD}+0.3$	V
"H" Input Voltage 2	*2	V_{IH2}	—	$0.6V_{DD}+0.4$	—	$V_{DD}+0.3$	
"L" Input Voltage		V_{IL}	—	–0.3	—	$0.15V_{DD}+0.1$	
"H" Output Voltage 1	*3	V_{OH1}	I_{OH}=–10µA	$0.75V_{DD}$	—	—	
"H" Output Voltage 2	*4	V_{OH2}	I_{OH}=–20µA	$0.75V_{DD}$	—	—	
"L" Output Voltage 1	*3	V_{OL1}	I_{OL}=10µA	—	—	0.1	
"L" Output Voltage 2	*4	V_{OL2}	I_{OL}=20µA	—	—	0.1	
Input Leakage Current 1	*5	I_{LI1}	$V_I=V_{DD}/0V$	—	—	±1	µA
Input Leakage Current 2	*6	I_{LI2}	$V_I=V_{DD}/0V$	—	—	±10	
"L" Input Current	*7	I_{IL}	V_{DD}=2.7 to 3.3V V_I=0V	–40	–120	–240	
Input Capacitance		C_I	f=1MHz, Ta=25°C	—	5	—	pF
Static Current Consumption		I_{DDS}	3V, stop mode *8	—	—	25	µA
Dynamic Current Consumption		I_{DD}	5MHz, 3V, no load Refer to Figure 2	—	6	15	mA

*1 Excluding OSC0 and $\overline{\text{RESET}}$
*2 OSC0 and $\overline{\text{RESET}}$
*3 Excluding P0, ALE, $\overline{\text{RD}}$, P2.6/$\overline{\text{WR}}$
*4 P0, ALE, $\overline{\text{RD}}$, P2.6/$\overline{\text{WR}}$
*5 $\overline{\text{EA}}$, P6
*6 Excluding $\overline{\text{RESET}}$, EA, P6
*7 $\overline{\text{RESET}}$
*8 The ports set for input mode are V_{DD} or 0V and the ports except these are no load.

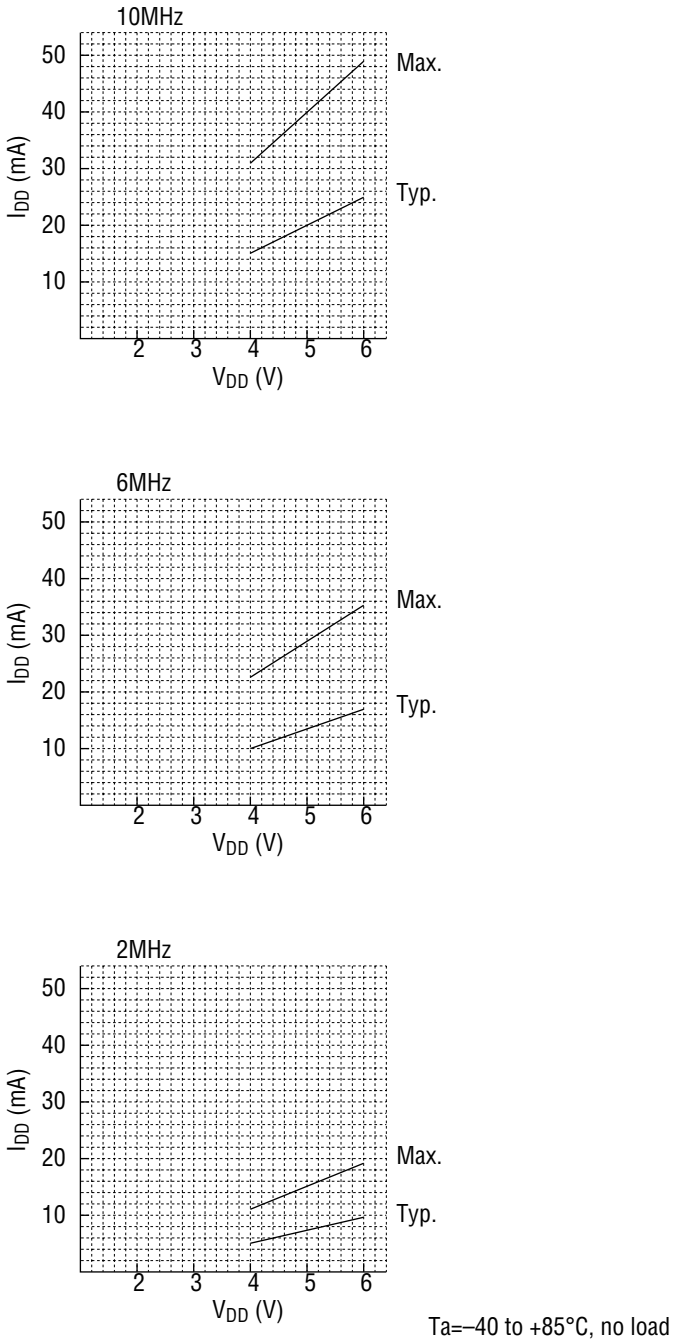


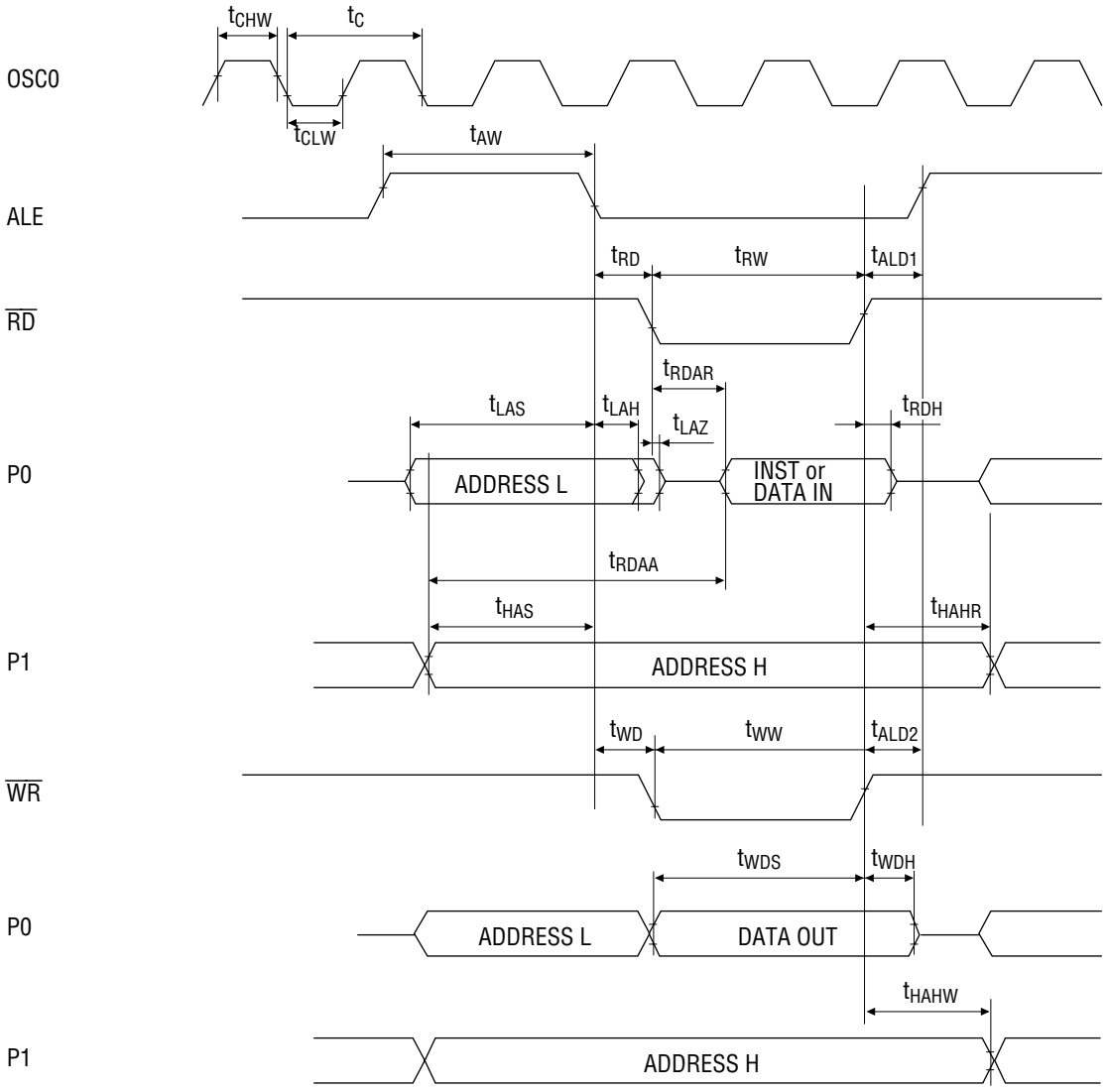
Figure 2. Voltage vs. Current

AC Characteristics

- **External memory control**

(V_{DD}=AV_{DD}=V_{RH}=2.7 to 5.5V, GND=AGND=V_{RL}=0V, Ta=–40 to +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Clock Period	t_C	V_{DD}=4.5 to 5.5V	100	—	ns
"L" Clock Pulse Width	t_{CLW}		45	—	
"H" Clock Pulse Width	t_{CHW}		45	—	
Clock Period	t_C	V_{DD}=2.7 to 5.5V	200	—	
"L" Clock Pulse Width	t_{CLW}		90	—	
"H" Clock Pulse Width	t_{CHW}		90	—	
ALE Pulse Width	t_{AW}	C_L=100pF	$t_C+t_{CHW}-20$	—	
ALE Pulse Delay Time 1	t_{ALD1}		$t_{CLW}-20$	—	
ALE Pulse Delay Time 2	t_{ALD2}		$t_{CLW}-20$	—	
$\overline{RD}$ Pulse Width	t_{RW}		$t_C+t_{CHW}-20$	—	
$\overline{RD}$ Pulse Delay Time	t_{RD}		$t_{CLW}-20$	$t_{CLW}+20$	
$\overline{WR}$ Pulse Width	t_{WW}		$t_C+t_{CHW}-40$	—	
$\overline{WR}$ Pulse Delay Time	t_{WD}		$t_{CLW}-20$	$t_{CLW}+40$	
"L" Address Setup Time	t_{LAS}		t_C-40	—	
"H" Address Setup Time	t_{HAS}		t_C-40	—	
"L" Address Hold Time	t_{LAH}		$t_{CLW}-20$	—	
Bus Float Time	t_{LAZ}		—	20	
"H" Address Hold Time	t_{HAHR}		t_C-20	—	
"H" Address Hold Time	t_{HAHW}		t_C-20	—	
Read Data Access Time	t_{RDAA}		—	$t_C+t_{CLW}-15$	
Read Data Access Time	t_{RDAR}		—	$t_{CHW}+10$	
Read Data Hold Time	t_{RDH}		0	—	
Write Data Setup Time	t_{WDS}		$t_C+t_{CHW}-40$	—	
Write Data Hold Time	t_{WDH}		$t_{CLW}-20$	—	


OSC0
ALE
RD
P0
P1
WR
P0
P1
tCHW
tC
tCLW
tAW
tRD
tRW
tALD1
tRDAR
tLAS
tLAH
tLAZ
tRDH
ADDRESS L
INST or
DATA IN
tRDAA
tHAS
tHAHR
ADDRESS H
tWD
tWW
tALD2
tWDS
tWDH
ADDRESS L
DATA OUT
tHAHW
ADDRESS H

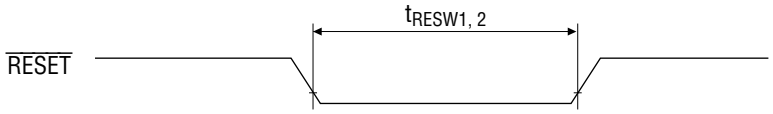
- **CPU control**

(V_{DD}=AV_{DD}=V_{RH}=2.7 to 5.5V, GND=AGND=V_{RL}=0V, Ta=–40 to +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
$\overline{\text{RESET}}$ Pulse Width *1	t_{RESW1}	—	20	—	ns
$\overline{\text{RESET}}$ Pulse Width *2	t_{RESW2}	—	*3	—	—

*1 Excluding power ON, stop mode and hard stop mode.
*2 In power ON, stop mode and hard stop mode.
*3 Oscillation stabilization time depends on resonator.

$\overline{\text{RESET}}$ Pulse Width

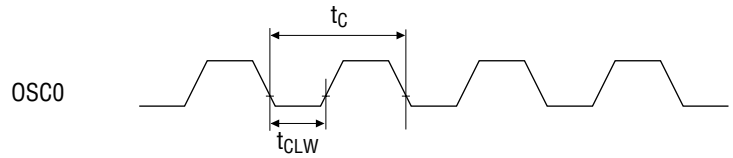


- **Peripheral control 1**

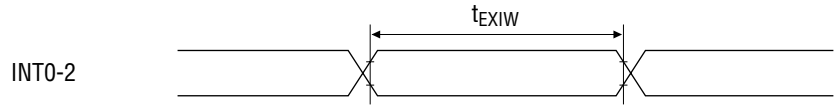
(V_{DD}=AV_{DD}=V_{RH}=2.7 to 5.5V, GND=AGND=V_{RL}=0V, Ta=–40 to +85°C)

Parameter		Symbol	Condition	Min.	Max.	Unit
OSC	Clock Period	t_C	V_{DD}=4.5 to 5.5V	100	—	ns
			V_{DD}=2.7 to 5.5V	200	—	
EXI	External Interrupt Pulse Width	t_{EXIW}	—	4 t_C	—	
T0	External Clock Pulse Width	t_{T0CW}		4 t_C	—	
	GATE Pulse Width	t_{T0GW}		1 t_{T0CLK} *1	—	
T2	External Clock Pulse Width	t_{T2CW}		4 t_C	—	
CAP	CAP Pulse Width	t_{CAPW}		12 t_C	—	

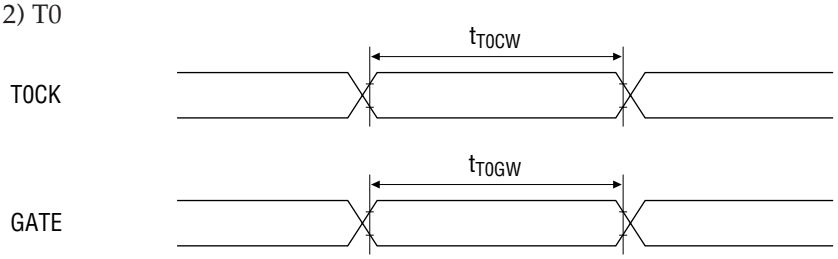
*1 t_{T0CLK} : Timer 0 count clock period selected by T0CON.



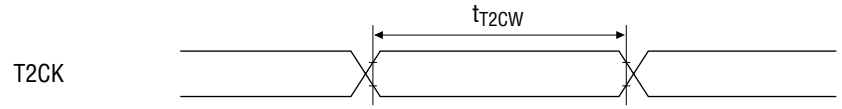
1) EXI pulse width



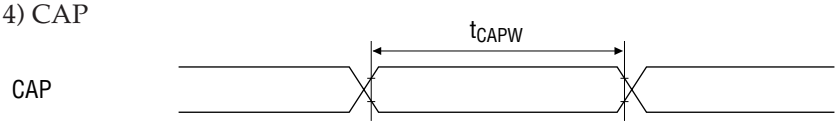
2) T0



3) T2



4) CAP

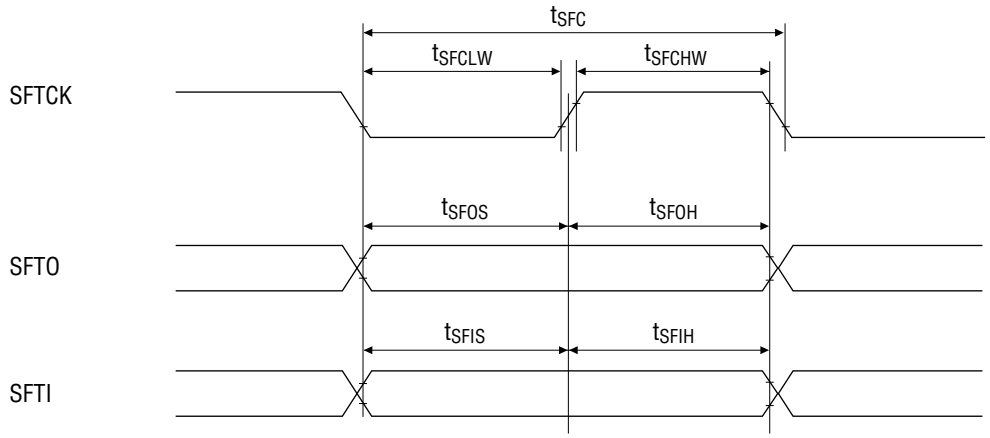


- **Peripheral control 2**

(V_{DD}=AV_{DD}=V_{RH}=2.7~5.5V, GND=AGND=V_{RL}=0V, Ta=–40 to +85°C)

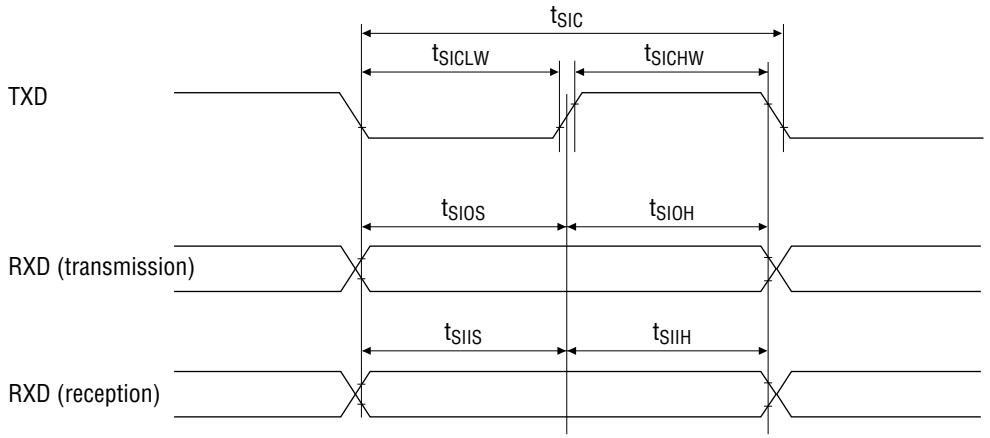
Parameter		Symbol	Condition	Min.	Max.	Unit
OSC	Clock Period	t_C	V_{DD}=4.5 to 5.5V	100	—	ns
			V_{DD}=2.7 to 5.5V	200	—	
SFT	SFTCK Period	t_{SFC}	C_L=100pF	8 t_C	—	
	SFTCK "L" Pulse Width	t_{SFCLW}		4 t_C–20	—	
	SFTCK "H" Pulse Width	t_{SFCHW}		4 t_C–20	—	
	SFTCK Setup Time	t_{SFOS}		t_{SFCLW}–100	—	
	SFTO Hold Time	t_{SFOH}		t_{SFCHW}–100	—	
	SFTI Setup Time	t_{SFIS}		100	—	
	SFTI Hold Time	t_{SFIH}		100	—	
SIO (Clock Synchro-nous Mode)	Synchronous Clock Period	t_{SIC}		8 t_C	—	
	Synchronous Clock "L" Pulse Width	t_{SICLW}		4 t_C–20	—	
	Synchronous Clock "H" Pulse Width	t_{SICHW}		4 t_C–20	—	
	Output Data Setup Time	t_{SIOS}		6 t_C–100	—	
	Output Data Hold Time	t_{SIOH}		2 t_C–100	—	
	Input Data Setup Time	t_{SIIS}		t_C+t_{CLW}+100	—	
	Input Data Hold Time	t_{SIIH}		0	—	

1) SFT



2) SIO

(Clock synchronous mode)



A/D Converter Characteristics 1

(V_{DD}=AV_{DD}=V_{RH}=5V±10%, GND=AGND=V_{RL}=0V, Ta=-40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	See the recommended circuit (Fig. 3). Analog input source impedance R_I≤5kΩ	—	8	—	bit
Absolute Error	E_L		—	—	+1.5 –1.5	LSB
Differential Linearity Error	E_D		—	—	±0.5	LSB
Zero Point Error	E_{ZS}		—	—	+1.5	LSB
Full Scale Error	E_{FS}		—	—	–1.5	LSB
Crosstalk	E_{CT}	See the measuring circuit (Fig. 4).	—	—	±0.5	LSB
Conversion time *	t_{CONV}	f_{OSC}=10 MHz	—	16	—	µs/CH

* The transition time after the G0 bit goes to "1" is 14.8µs/CH.

A/D Converter Characteristics 2

(V_{DD}=AV_{DD}=V_{RH}=2.7 to 4.5V, GND=AGND=V_{RL}=0V, Ta=-40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	See the recommended circuit (Fig. 3). Analog input source impedance R_I≤5kΩ	—	8	—	bit
Absolute Error	E_L		—	—	+2 –2	LSB
Differential Linearity Error	E_D		—	—	±1	LSB
Zero Point Error	E_{ZS}		—	—	+2	LSB
Full Scale Error	E_{FS}		—	—	–2	LSB
Crosstalk	E_{CT}	See the measuring circuit (Fig. 4).	—	—	±1	LSB
Conversion time *	t_{CONV}	f_{OSC}=5 MHz	—	32	—	µs/CH

* The transition time after the G0 bit goes to "1" is 29.6µs/CH.

• Definitions of terms

(1) Resolution
The minimum distinguishable analog value. For 8 bits, 2^8=256, i.e. $(V_{RH}–V_{RL}) \div 256$.

(2) Linearity Error
The variance between the ideal conversion characteristics as an 8-bit A/D converter and actual conversion characteristics (does not include quantatized error).

The ideal conversion characteristics refer to steps of the voltage between V_{RH} and V_{RL} into 256 intervals.

(3) Differential Linearity Error
Indicates the smoothness of the conversion. The width of analog input voltage corresponding to the change by one bit of digital output is 1 LSB = $(V_{RH}-V_{RL}) \div 256$ ideally. The variance between this ideal bit size and bit size at arbitrary point in the conversion range.

(4) Zero Scale Error
The variance between the ideal conversion characteristics at the switching point of digital output "000H to 001H" and actual conversion characteristics.

(5) Full Scale Error
The variance between the ideal conversion characteristics at the switching point of digital output "0FEH to 0FFH" and actual conversion characteristics.

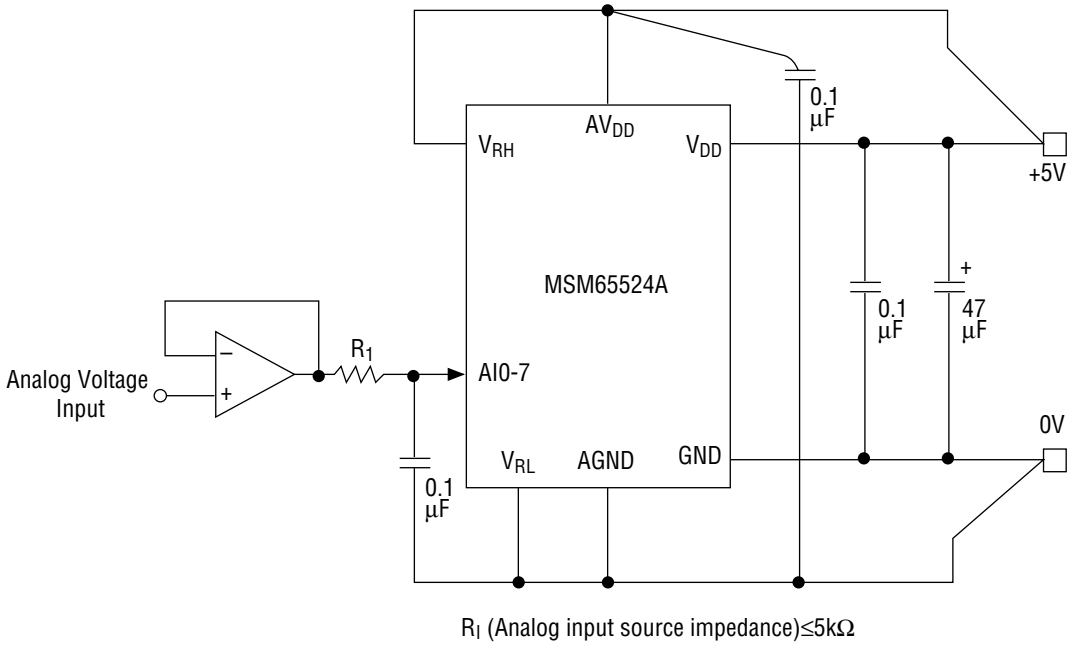


Figure 3. Recommended Circuit

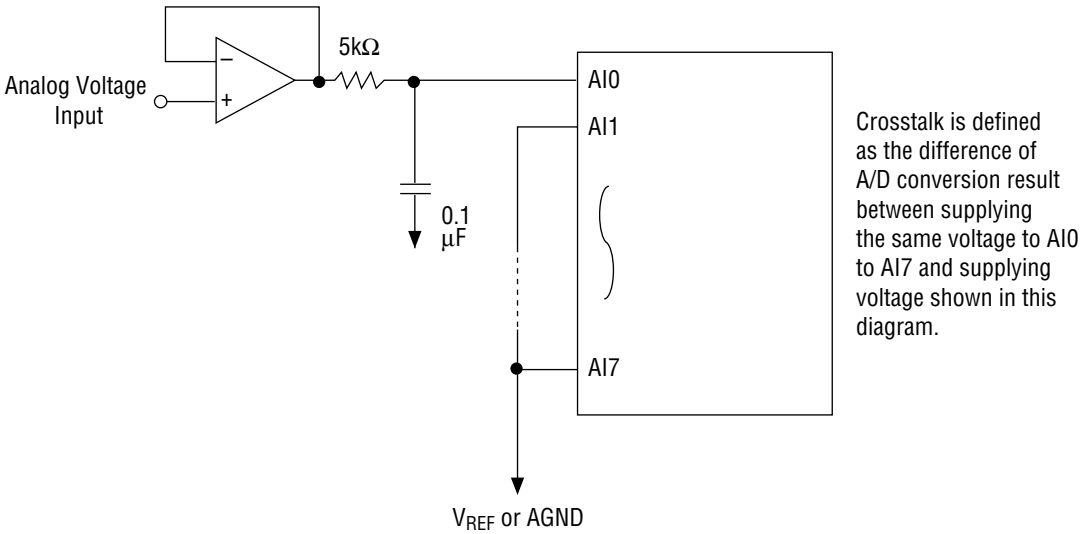
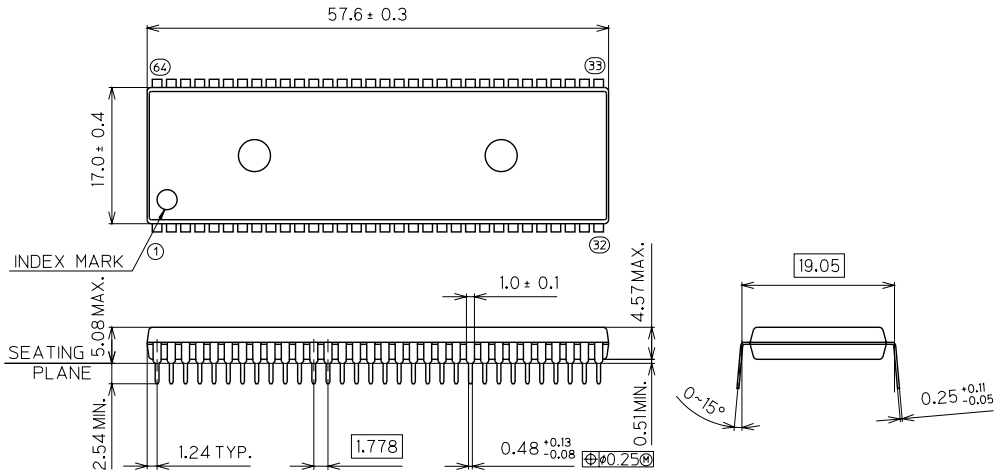


Figure 4. Crosstalk Measuring Circuit

PACKAGE DIMENSIONS

(Unit : mm)

SDIP64-P-750-1.78



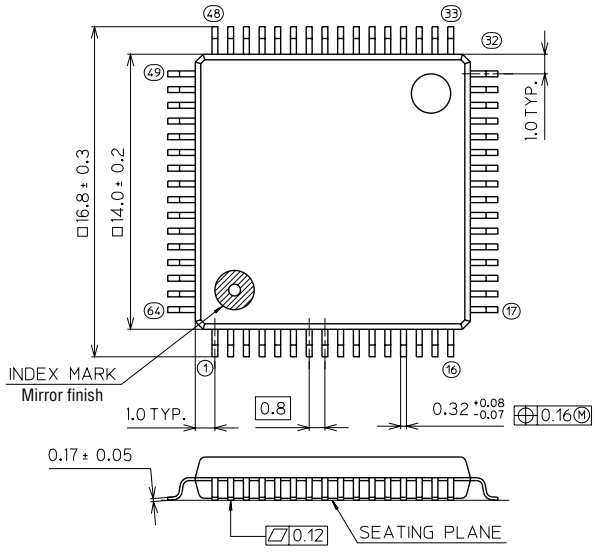
Package material	Epoxy resin
Lead frame material	Cu alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	8.70 TYP.

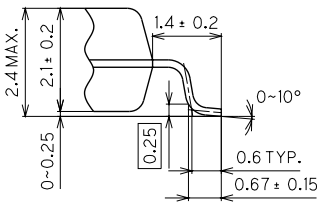
Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

QFP64-P-1414-0.80-BK





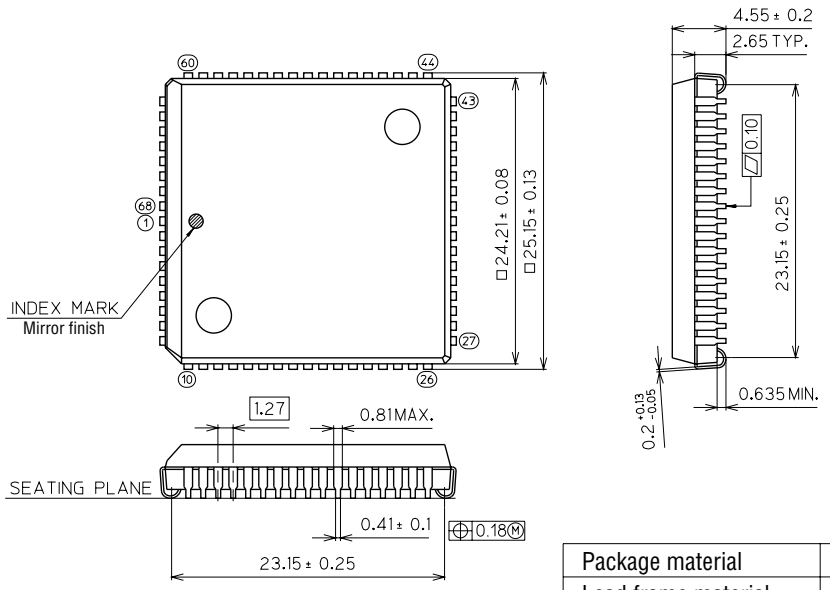
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.87 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

QFJ68-P-S950-1.27



Package material	Epoxy resin
Lead frame material	Cu alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	4.50 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).