MOTOROLA

MC54/74F568
MC54/74F569

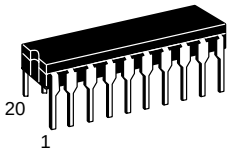
4-BIT BIDIRECTIONAL COUNTERS (WITH 3-STATE OUTPUTS)

4-BIT BIDIRECTIONAL COUNTERS (WITH 3-STATE OUTPUTS)

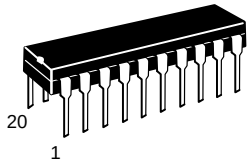
FAST™ SCHOTTKY TTL

The MC54/74F568 and MC54/74F569 are fully synchronous, reversible counters with 3-state outputs. The F568 is a BCD decade counter; the F569 is a binary counter. They feature preset capability for programmable operation, carry lookahead for easy cascading, and a U/$\overline{D}$ input to control the direction of counting. For maximum flexibility there are both synchronous and master asynchronous reset inputs as well as both Clocked Carry ($\overline{CC}$) and Terminal Count ($\overline{TC}$) outputs. All state changes except Master Reset are initiated by the rising edge of the clock. A HIGH signal on the Output Enable ($\overline{OE}$) input forces the output buffers into the high impedance state but does not prevent counting, resetting or parallel loading.

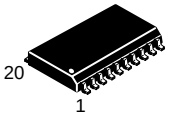
- 4-Bit Bidirectional Counting
  - F568 Decade Counter
  - F569 Binary Counter
- Synchronous Counting and Loading
- Lookahead Carry Capability for Easy Cascading
- Preset Capability for Programmable Operation
- 3-State Outputs for Bus Organized Systems
- Master Reset ($\overline{MR}$) Overrides All Other Inputs
- Synchronous Reset ($\overline{SR}$) Overrides Counting and Parallel Loading



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03

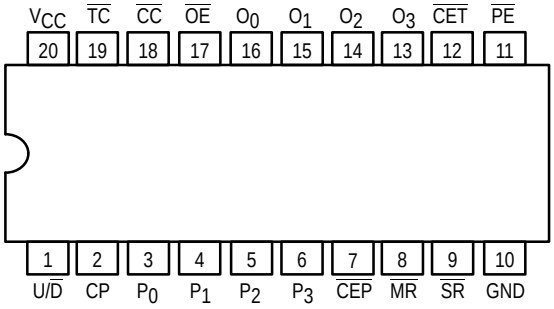


DW SUFFIX
SOIC
CASE 751D-03

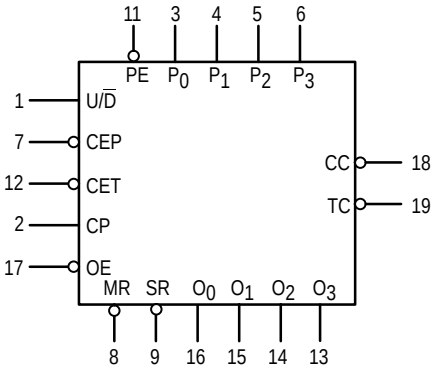
ORDERING INFORMATION

MC54FXXXJ	Ceramic
MC74FXXXN	Plastic
MC74FXXXDW	SOIC

CONNECTION DIAGRAM



LOGIC SYMBOL



Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54	–55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			–3.0	mA
I_{OL}	Output Current — Low	54, 74			24	mA

FUNCTIONAL DESCRIPTION

The F568 counts modulo-10 in the BCD (8421) sequence. From state 9 (HLLH) it will increment to 0 (LLLL) in the Up mode; in Down mode it will decrement from 0 to 9.The F569 counts in the modulo-16 binary sequence. From state 15 it will increment to state 0 in the Up mode; in the Down mode it will decrement from 0 to 15. The clock inputs of all flip-flops are driven in parallel through a clock buffer. All state changes (except due to Master Reset) occur synchronously with the LOW-to-HIGH transition of the Clock Pulse (CP) input signal.

The circuits have five fundamental modes of operation, in order of precedence: asynchronous reset, synchronous reset, parallel load, count and hold. Five control inputs — Master Reset ($\overline{MR}$), Synchronous Reset ($\overline{SR}$), Parallel Enable ($\overline{PE}$), Count Enable Parallel ($\overline{CEP}$) and Count Enable Trickle ($\overline{CET}$) — plus the Up/Down (U/$\overline{D}$) input, determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces the flip-flop Q outputs LOW. A LOW signal on $\overline{SR}$ overrides counting and parallel loading and allows the Q outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{MR}$, $\overline{SR}$ and $\overline{PE}$ HIGH, $\overline{CEP}$ and $\overline{CET}$ permit counting when both are LOW. Conversely, a HIGH signal on either $\overline{CEP}$ or $\overline{CET}$ inhibits counting.

The F568 and F569 use edge-triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, $\overline{CEP}$, $\overline{CET}$ or U/$\overline{D}$ inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

Two types of outputs are provided as overflow/underflow indicators. The Terminal Count ($\overline{TC}$) output is normally HIGH and goes LOW providing $\overline{CET}$ is LOW, when the counter reaches zero in the Down mode, or reaches maximum (9 for the F568,15 for the F569) in the Up mode. $\overline{TC}$ will then remain LOW until a state change occurs, whether by counting or presetting, or until U/$\overline{D}$ or $\overline{CET}$ is changed. To implement synchronous multistage counters, the connections between the $\overline{TC}$ output and the $\overline{CEP}$ and $\overline{CET}$ inputs can provide either slow or fast carry propagation. Figure A shows the connections for simple ripple carry, in which the clock period must be longer than the CP to $\overline{TC}$ delay of the first stage, plus the cumulative $\overline{CET}$ to $\overline{TC}$ delays of the intermediate stages, plus the $\overline{CET}$ to CP setup time of the last stage. This total delay plus setup time sets the upper limit on clock frequency. For faster clock rates, the carry lookahead connections shown in Figure B are recommended. In this scheme the ripple delay through the intermediate stages commences with the same clock that causes the first stage to tick over from max to min in the Up mode, or min to max in the Down mode, to start its final cycle. Since this final cycle takes 10 (F568) or 16 (F569) clocks to complete, there is plenty of time for the ripple to progress through the intermediate stages. The critical timing that limits the clock period is the CP to $\overline{TC}$ delay of the first stage plus the $\overline{CEP}$ to CP setup time of the last stage. The $\overline{TC}$ output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, registers or counters. For such applications, the Clocked Carry ($\overline{CC}$) output is provided. The $\overline{CC}$ output is normally HIGH. When $\overline{CEP}$, $\overline{CET}$, and $\overline{TC}$ are LOW, the $\overline{CC}$ output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again, as shown in the $\overline{CC}$ Truth Table. When the Output Enable ($\overline{OE}$) is LOW, the parallel data outputs O_0–O_3 are active and follow the flip-flop Q outputs. A HIGH signal on $\overline{OE}$ forces O_0–O_3 to the High Z state but does not prevent counting, loading or resetting.

LOGIC EQUATIONS:

Count Enable = $\overline{CEP}\cdot\overline{CET}\cdot PE$

Up ('F568): $\overline{TC} = Q_0\cdot\overline{Q}_1\cdot\overline{Q}_2\cdot Q_3\cdot(Up)\cdot\overline{CET}$

('F569): $\overline{TC} = Q_0\cdot Q_1\cdot Q_2\cdot Q_3\cdot(Up)\cdot\overline{CET}$

Down (Both): $\overline{TC} = \overline{Q}_0\cdot\overline{Q}_1\cdot\overline{Q}_2\cdot\overline{Q}_3\cdot(Down)\cdot\overline{CET}$

$\overline{CC}$ TRUTH TABLE

Inputs						Output
$\overline{SR}$	$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	$\overline{TC}$*	CP	$\overline{CC}$
L	X	X	X	X	X	H
X	L	X	X	X	X	H
X	X	H	X	X	X	H
X	X	X	H	X	X	H
X	X	X	X	H	X	H
H	H	L	L	L	⊓	⊓

* = $\overline{TC}$ is generated internally

X = Don't Care

L = LOW Voltage Level

⊓ = Low Pulse

H = HIGH Voltage Level

FUNCTION TABLE

Inputs							Operating Mode
$\overline{MR}$	$\overline{SR}$	$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	CP	
L	X	X	X	X	X	X	Asynchronous reset
h	l	X	X	X	X	↑	Synchronous reset
h	h	l	X	X	X	↑	Parallel load
h	h	h	l	l	h	↑	Count up (increment)
h	h	h	l	l	l	↑	Count down (decrement)
h	H	H	H	X	X	X	Hold (do nothing)
h	H	H	X	H	X	X	

H = HIGH voltage level

h = HIGH voltage level one setup prior to the Low-to-High Clock transition

L = LOW voltage level

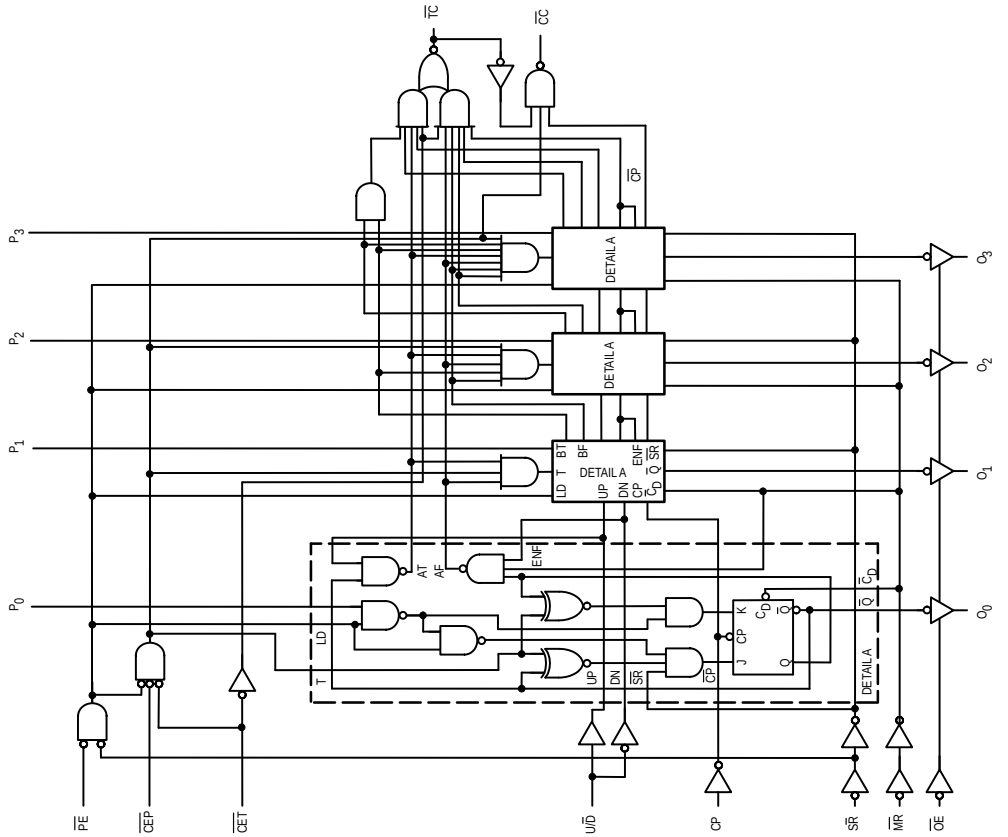
l = LOW voltage level one setup prior to the Low-to-High clock transition

X = Don't care

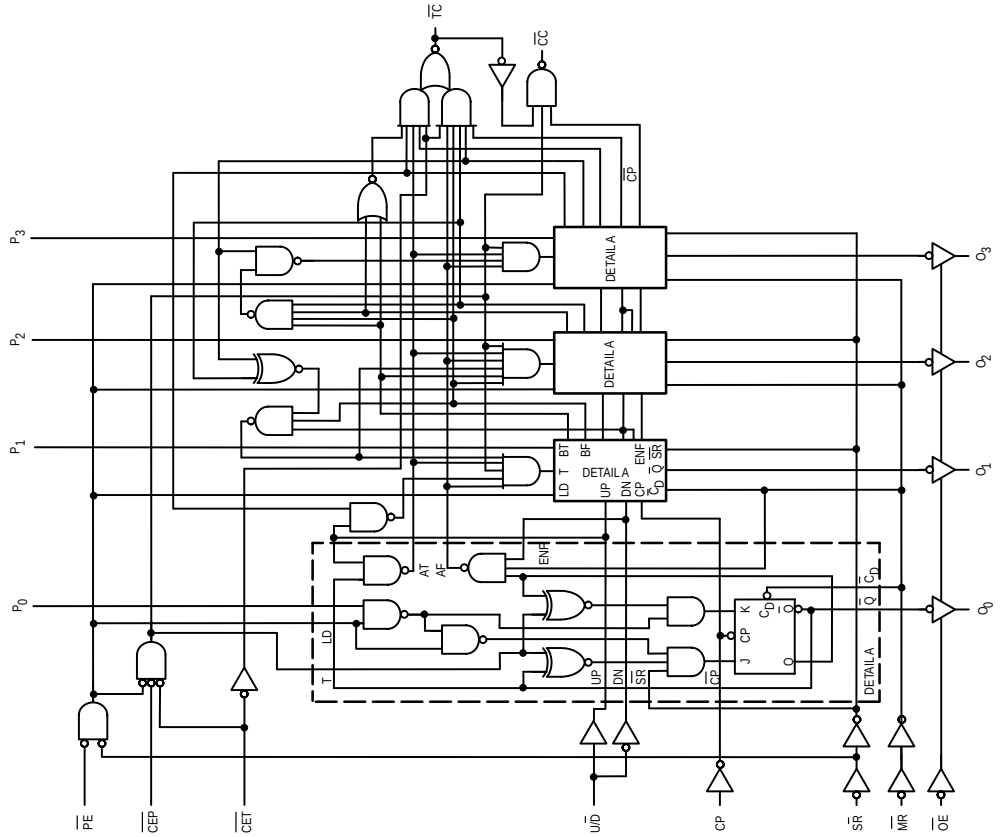
↑ = Low-to-High clock transition

LOGIC DIAGRAMS

MC54/74F569



MC54/74F568



Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure A. Multistage Counter with Ripple Carry

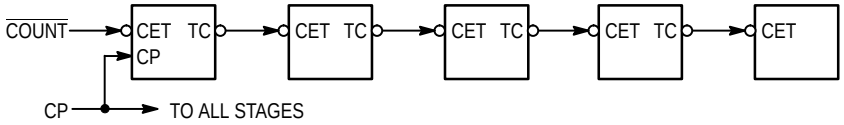
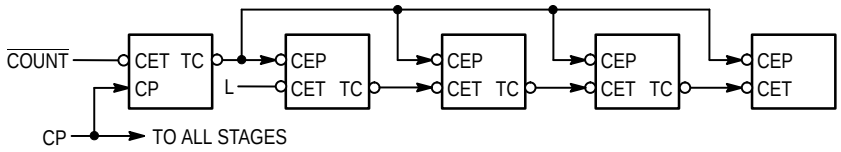


Figure B. Multistage Counter with Lookahead Carry



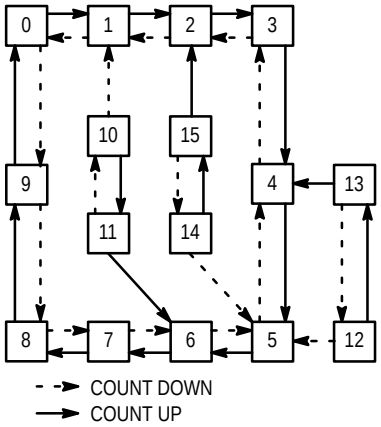
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage for All Inputs	
V_{IK}	Input Clamp Diode Voltage				–1.2	V	V_{CC} = MIN, I_{IN} = –18 mA	
V_{OH}	Output HIGH Voltage	54, 74	2.4	3.3		V	I_{OH} = –3.0 mA	V_{CC} = 4.5 V
		74	2.7	3.3		V	I_{OH} = –3.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage			0.3	0.5	V	I_{OL} = 24 mA	V_{CC} = MIN
I_{OZH}	Output OFF Current — HIGH				50	µA	V_{OUT} = 2.7 V	V_{CC} = MAX
I_{OZL}	Output OFF Current — LOW				–50	µA	V_{OUT} = 0.5 V	V_{CC} = MAX
I_{IH}	Input HIGH Current				20	µA	V_{IN} = 2.7 V	V_{CC} = MAX
					100		V_{IN} = 7.0 V	
I_{IL}	Input LOW Current $\overline{PE}$, $\overline{CET}$ Others				–1.2 –0.6	mA	V_{CC} = MAX, V_{IN} = 0.5 V	
I_{OS}	Output Short Circuit Current (Note 2)		–60		–150	mA	V_{OUT} = 0 V	V_{CC} = MAX
I_{CC}	Power Supply Current (ALL Outputs OFF)				67	mA	V_{CC} = MAX	

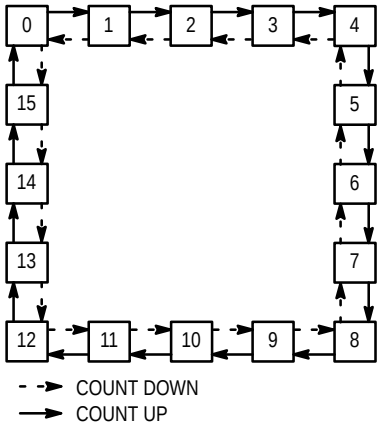
NOTES:
1. For conditions such as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

STATE DIAGRAMS

MC54/74F568



MC54/74F569



AC CHARACTERISTICS

Symbol	Parameter	54/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF		54F T_A = −55 to +125°C V_{CC} = 5.0 V ±10% C_L = 50 pF		74F T_A = 0 to +70°C V_{CC} = 5.0 V ±10% C_L = 50 pF		Unit
		Min	Max	Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	100		60		85		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to O_n ($\overline{PE}$ HIGH or LOW)	3.0 4.0	8.5 11.5	3.0 4.0	10.5 14	3.0 4.0	9.5 13	ns
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$	5.5 4.0	15.5 11	5.5 4.0	18.5 13.5	5.5 4.0	17.5 12.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	2.5 2.5	6.0 8.0	2.5 2.5	8.0 10	2.5 2.5	7.0 9.0	ns
t_{PLH} t_{PHL}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$ ('F568)	3.5 4.0	11 16	3.5 4.0	13.5 19	3.5 4.0	12.5 18	ns
t_{PLH} t_{PHL}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$ ('F569)	3.5 4.0	11 10.5	3.5 4.0	13.5 13	3.5 4.0	12.5 12	ns
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{CC}$	2.5 2.0	7.0 6.0	2.5 2.0	9.0 8.0	2.5 2.0	8.0 7.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CEP}$, $\overline{CET}$ to $\overline{CC}$	2.5 4.0	6.5 11	2.5 4.0	8.5 13.5	2.5 4.0	7.5 12.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to O_n	5.0	13	5.0	15.5	5.0	14.5	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	2.5 3.0	7.0 8.0	2.5 3.0	9.0 10	2.5 3.0	8.0 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	1.5 2.0	6.5 6.0	1.5 2.0	8.5 8.0	1.5 2.0	7.5 7.0	ns

AC OPERATING REQUIREMENTS

Symbol	Parameter	54/74F T_A = +25°C V_{CC} = +5.0 V		54F T_A = −55°C to +125°C V_{CC} = 5.0 V ±10%		74F T_A = 0°C to +70°C V_{CC} = 5.0 V ±10%		Unit
		Min	Max	Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW P_n to CP	4.0 4.0		5.5 5.5		4.5 4.5		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW P_n to CP	3.0 3.0		3.5 3.5		3.5 3.5		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{CEP}$ or $\overline{CET}$ to CP	5.0 5.0		7.0 7.0		6.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{CEP}$ or $\overline{CET}$ to CP	0 0		0 0		0 0		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{PE}$ to CP	8.0 8.0		10 10		9.0 9.0		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{PE}$ to CP	0 0		0 0		0 0		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW U/$\overline{D}$ to CP (F568)	11 16.5		13.5 18.5		12.5 17.5		ns
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW U/$\overline{D}$ to CP (F569)	11 7.0		13.5 10		12.5 8.0		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW U/$\overline{D}$ to CP	0 0		0 0		0 0		ns
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{SR}$ to CP	10 8.0		12 10.5		11 9.5		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{SR}$ to CP	0 0		0 0		0 0		
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	4.0 6.0		6.0 8.0		4.5 6.5		ns
$t_w(L)$	$\overline{MR}$ Pulse Width, LOW	4.5		6.0		5.0		ns
t_{rec}	$\overline{MR}$ Recovery Time	6.0		8.0		7.0		ns