TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

JTMP04030-XXXS

CMOS 4 BIT LL MICROCONTROLLER
(LL : LOW-POWER CONSUMPTION & LOW-VOLTAGE OPERATION)

JTMP04030-XXXS is a high-performance 4 bit LL microcontroller designed to be used in applications where low voltage operation is required.

JTMP04030-XXXS integrates a high-performance CPU, memory (static work RAM, Data RAM, program ROM), LCD driver, and multifunction timers on a single chip.

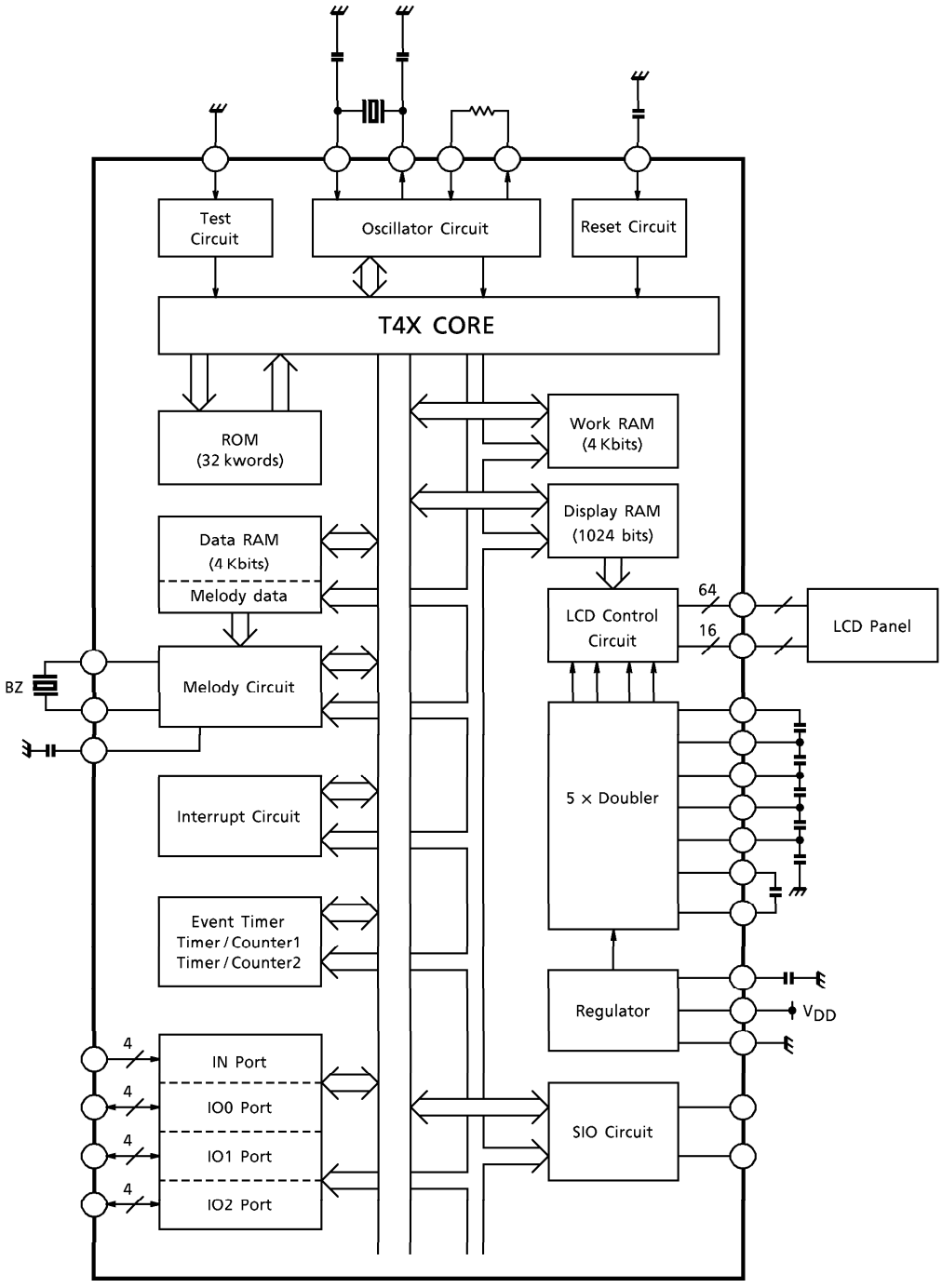
The basic features are as follows:

FEATURES

- Number of instructions : 56
- Minimum instruction execution time : 61 μs (at 32.768 kHz)
  1 μs (at 2 MHz / 3.0 V)
- Oscillator circuit : High-speed crystal oscillator (external resistor)
  Low-speed crystal oscillator (32.768 kHz / 36.864 kHz)
- Built-in ROM size : 32 K words
  (1 word = 16 bits)
- Built-in RAM size :
  Work RAM : 256 nibbles × 4 banks (including 64 stacks)
  Data RAM : 256 bytes × 2 banks (including melody data area)
- Input pins : 4 pins (with interrupts)
- Input / output pins : 12 pins (4 with interrupts)
- Output pins : 2 melody pins (BZ, $\overline{BZ}$)
- Interrups : 2 external interrupts (IN, IO0)
  5 internal interrupts (timer / counter 1, 2 timing, SIO, melody)
- Timers : Event / timer × 1
  8 bits × 2 channels or 16 bits × 1 channel timer / counter
  Watchdog timer × 1 channel
- Melody : Builtin scale generator circuit with Autoplay function
- Serial interface : 8 bit serial transfer
- LCD display driver controller : 16 COM × 64 SEG

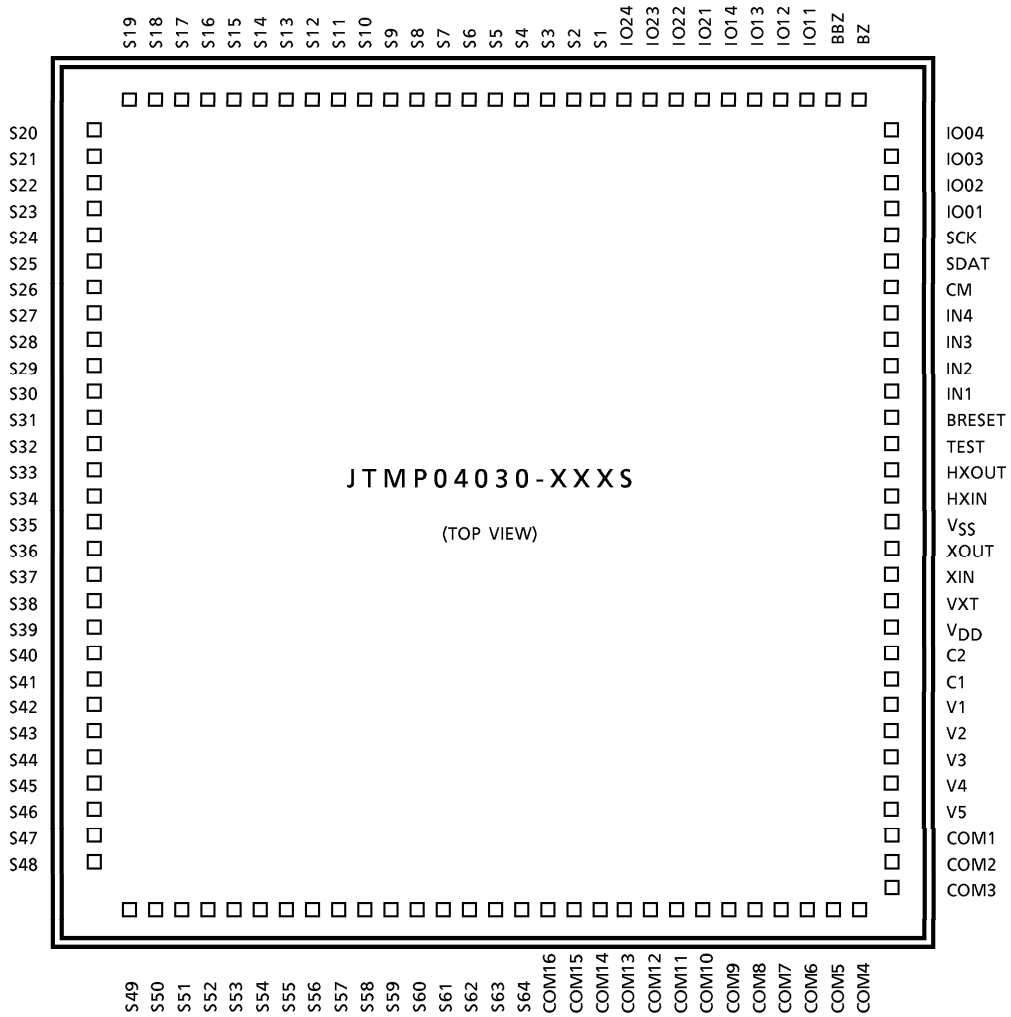
980910EBA1

SYSTEM BLOCK DIAGRAM



PAD / PIN LAYOUT

1. Pad Layout



CHIP SIZE 5.25 × 5.31 (mm)
CHIP THICKNESS 450 ± 30 (μm)

REFERENCE VOLTAGE V_{SS}

2. Pad Locations and Functions

No.	NAME	X POINT	Y POINT	FUNCTION
1	S_{49}	– 2181	– 2489	Segment output pins
2	S_{50}	– 2025	– 2489	
3	S_{51}	– 1870	– 2489	
4	S_{52}	– 1714	– 2489	
5	S_{53}	– 1558	– 2489	
6	S_{54}	– 1402	– 2489	
7	S_{55}	– 1246	– 2489	
8	S_{56}	– 1091	– 2489	
9	S_{57}	– 935	– 2489	
10	S_{58}	– 779	– 2489	
11	S_{59}	– 623	– 2489	
12	S_{60}	– 467	– 2489	
13	S_{61}	– 312	– 2489	
14	S_{62}	– 156	– 2489	
15	S_{63}	0	– 2489	
16	S_{64}	156	– 2489	
17	COM16	312	– 2489	Common output pins
18	COM15	467	– 2489	
19	COM14	623	– 2489	
20	COM13	779	– 2489	
21	COM12	935	– 2489	
22	COM11	1091	– 2489	
23	COM10	1246	– 2489	
24	COM9	1402	– 2489	
25	COM8	1558	– 2489	
26	COM7	1714	– 2489	
27	COM6	1870	– 2489	
28	COM5	2025	– 2489	
29	COM4	2181	– 2489	
30	COM3	2517	– 2190	
31	COM2	2517	– 2039	
32	COM1	2517	– 1888	
33	V_5	2517	– 1737	Capacitor connecting pins for stabilizing LCD reference voltage
34	V_4	2517	– 1586	
35	V_3	2517	– 1435	
36	V_2	2517	– 1284	
37	V_1	2517	– 1133	
38	C_1	2517	– 982	Capacitor connecting pins for LCD booster
39	C_2	2517	– 831	
40	V_{DD}	2517	– 680	Supply voltage pin
41	VXT	2517	– 529	Capacitor connecting pin for stabilizing reference voltage applied to low-speed oscillator circuit

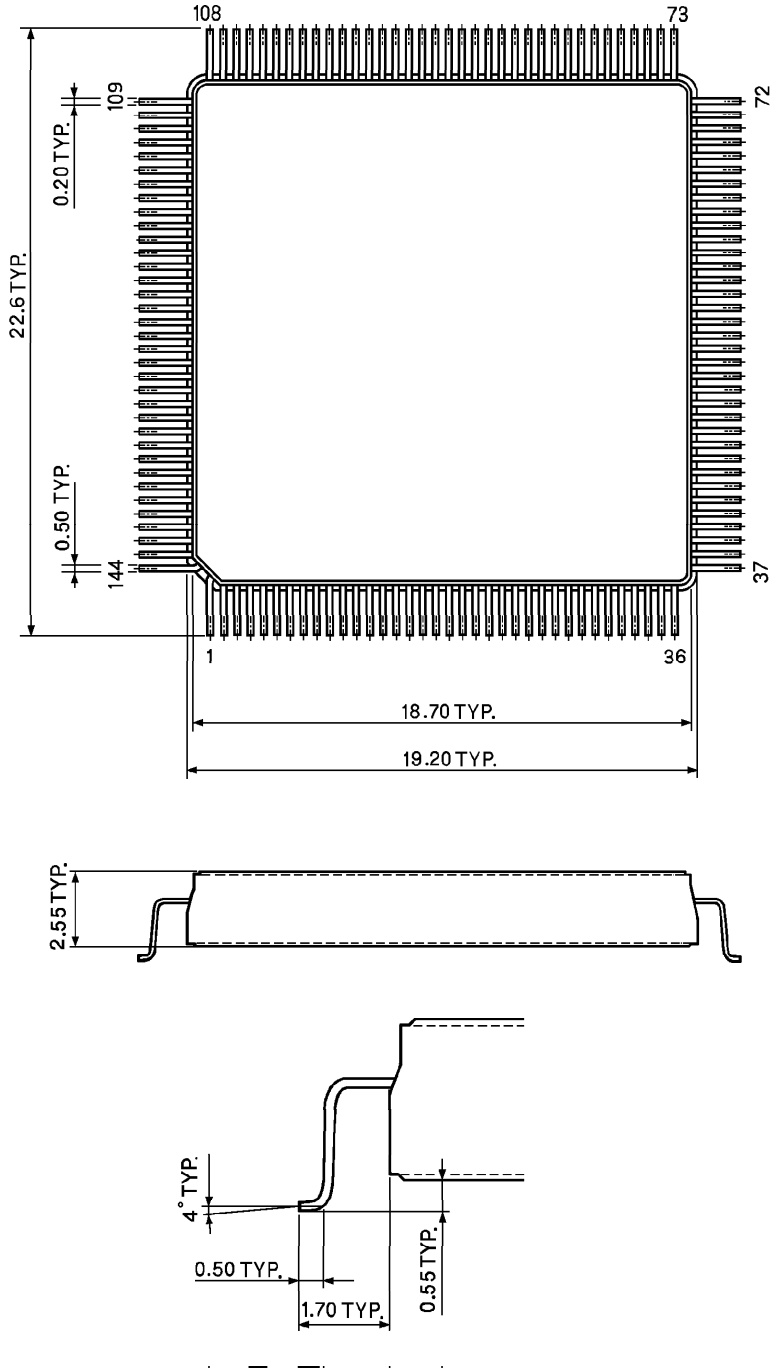
No.	NAME	X POINT	Y POINT	FUNCTION
42	XLIN	2517	– 378	Crystal connecting pins for low-speed oscillation
43	XLOUT	2517	– 226	
44	V_{SS}	2517	– 75	Ground pin
45	XHIN	2517	76	Resistor connecting pin for high-speed oscillation
46	XHOUT	2517	227	
47	TEST	2517	378	Always grounded (test pin)
48	BRESET	2517	529	Reset capacitor connecting pin
49	IN1	2517	680	Input port pins (with interrupts)
50	IN2	2517	831	
51	IN3	2517	982	
52	IN4	2517	1133	
53	CM	2517	1284	Melody capacitor connecting pin
54	SDAT	2517	1435	Serial Data
55	SCK	2517	1586	Serial clock
56	IO01	2517	1737	Input / output port 0 pins
57	IO02	2517	1888	
58	IO03	2517	2039	
59	IO04	2517	2190	
60	BZ	2181	2489	Melody output
61	BBZ	2025	2489	Inverted Melody output / carrier output (switchable by software)
62	IO11	1870	2489	Input / output port 1 pins
63	IO12	1714	2489	
64	IO13	1558	2489	
65	IO14	1402	2489	
66	IO21	1246	2489	Input / output port 2 pins
67	IO22	1091	2489	
68	IO23	935	2489	
69	IO24	779	2489	
70	S_1	623	2489	Segment output pins
71	S_2	467	2489	
72	S_3	312	2489	
73	S_4	156	2489	
74	S_5	0	2489	
75	S_6	– 156	2489	
76	S_7	– 312	2489	
77	S_8	– 467	2489	
78	S_9	– 623	2489	
79	S_{10}	– 779	2489	
80	S_{11}	– 935	2489	
81	S_{12}	– 1091	2489	
82	S_{13}	– 1246	2489	
83	S_{14}	– 1402	2489	
84	S_{15}	– 1558	2489	

No.	NAME	X POINT	Y POINT	FUNCTION
85	S_{16}	– 1714	2489	Segment output pins
86	S_{17}	– 1870	2489	
87	S_{18}	– 2025	2489	
88	S_{19}	– 2181	2489	
89	S_{20}	– 2517	2186	
90	S_{21}	– 2517	2030	
91	S_{22}	– 2517	1874	
92	S_{23}	– 2517	1719	
93	S_{24}	– 2517	1563	
94	S_{25}	– 2517	1407	
95	S_{26}	– 2517	1251	
96	S_{27}	– 2517	1095	
97	S_{28}	– 2517	940	
98	S_{29}	– 2517	784	
99	S_{30}	– 2517	628	
100	S_{31}	– 2517	472	
101	S_{32}	– 2517	316	
102	S_{33}	– 2517	161	
103	S_{34}	– 2517	5	
104	S_{35}	– 2517	– 151	
105	S_{36}	– 2517	– 307	
106	S_{37}	– 2517	– 463	
107	S_{38}	– 2517	– 618	
108	S_{39}	– 2517	– 774	
109	S_{40}	– 2517	– 930	
110	S_{41}	– 2517	– 1086	
111	S_{42}	– 2517	– 1242	
112	S_{43}	– 2517	– 1397	
113	S_{44}	– 2517	– 1553	
114	S_{45}	– 2517	– 1709	
115	S_{46}	– 2517	– 1865	
116	S_{47}	– 2517	– 2021	
117	S_{48}	– 2517	– 2176	

3. Dimensions for engineer-sampling package

Unit mm

* This package is only available with an engineer-sampling device; hence, the package is not in mass production. Please take this into account.



4. Pin assignment for engineer-sampling package

No.	NAME	No.	NAME	No.	NAME	No.	NAME
1	S_{49}	37	COM3	73	BZ	109	S_{20}
2	S_{50}	38	COM2	74	BBZ	110	S_{21}
3	S_{51}	39	COM1	75	IO11	111	S_{22}
4	S_{52}	40	V_5	76	IO12	112	S_{23}
5	S_{53}	41	V_4	77	IO13	113	S_{24}
6	S_{54}	42	V_3	78	IO14	114	S_{25}
7		43	V_2	79		115	S_{26}
8	S_{55}	44		80	IO21	116	
9	S_{56}	45	V_1	81	IO22	117	S_{27}
10	S_{57}	46	C_1	82	IO23	118	S_{28}
11	S_{58}	47	C_2	83	IO24	119	S_{29}
12	S_{59}	48	V_{DD}	84		120	S_{30}
13		49	VXT	85	S_1	121	
14	S_{60}	50	XIN	86	S_2	122	S_{31}
15	S_{15}	51		87	S_3	123	S_{32}
16		52	XOUT	88		124	
17	S_{62}	53		89	S_4	125	S_{33}
18	S_{63}	54	V_{SS}	90	S_5	126	S_{34}
19		55	HXIN	91		127	
20	S_{64}	56		92	S_6	128	S_{35}
21		57	XHOUT	93	S_7	129	
22	COM16	58		94	S_8	130	S_{36}
23	COM15	59	TEST	95		131	S_{37}
24		60	BRESET	96	S_9	132	
25	COM14	61	IN1	97	S_{10}	133	S_{38}
26	COM13	62	IN2	98	S_{11}	134	S_{39}
27	COM12	63	IN3	99		135	S_{40}
28		64		100	S_{12}	136	
29	COM11	65	IN4	101	S_{13}	137	S_{41}
30	COM10	66	CM	102		138	S_{42}
31	COM9	67	SDAT	103	S_{14}	139	S_{43}
33	COM8	68	SCK	104	S_{15}	140	S_{44}
33	COM7	69	IO01	105	S_{16}	141	S_{45}
34	COM6	70	IO02	106	S_{17}	142	S_{46}
35	COM5	71	IO03	107	S_{18}	143	S_{47}
36	COM4	72	IO04	108	S_{19}	144	S_{48}

MEMORY MAP

1. Program ROM

The instruction word of T4X is 16 bits long. Op-codes and operands are executed in one-word units. Program ROM consists of 4 K words per page. The internal program ROM area is 8 pages (32 Kwords).
This program ROM area can be used for constant data ROM. In this case, it can be used in byte units (1 byte = 8 bits).

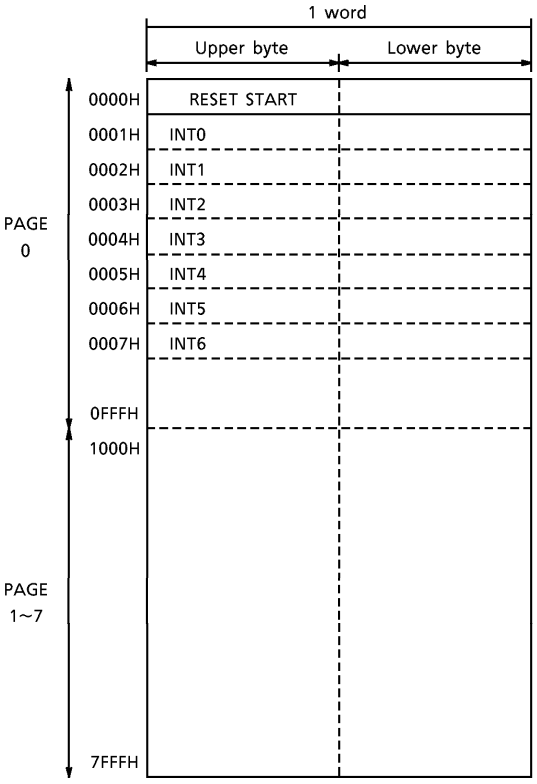


Fig.2 Program Memory Map

(Note) When coding interrupt entry addresses, use a CALL instruction.
Code NOP for interrupts not used.

```
Example  CALL A   ; INT0
         NOP      ; INT1
         CALL B   ; INT2
         NOP      ; INT3
         NOP      ; INT4
         NOP      ; INT5
         NOP      ; INT6
```

2. Word RAM

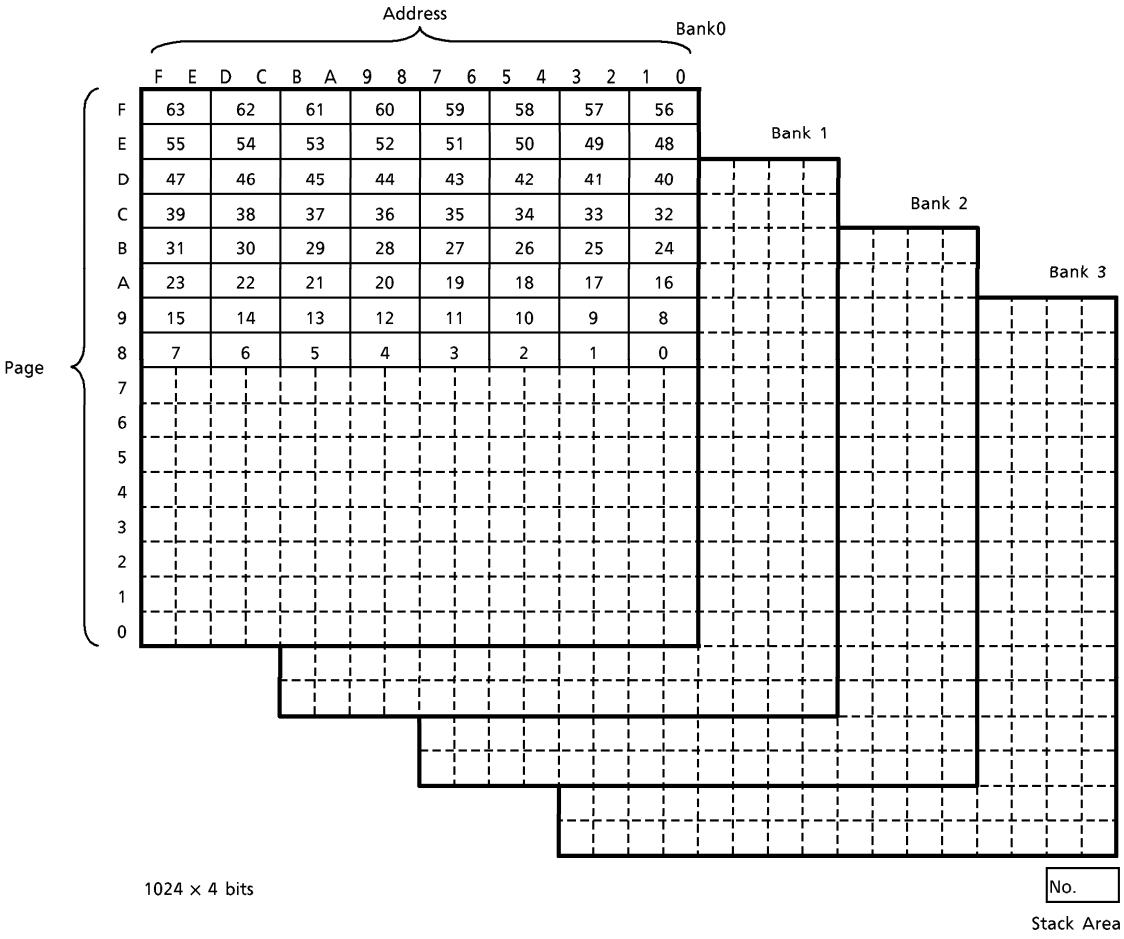


Fig.3 Work RAM

Work RAM consists of 1024 × 4 bits.
R / W is performed at the address specified as fllows.

(1) Indirect addressing mode (Fig.4 (a))

Specify a bank using DMB, a page using the H-Register, and an address in the page using the L-register.
(Example)

LD A, M : A ← RAM (HL)

(2) Directly addressing mode (Fig.4 (b))

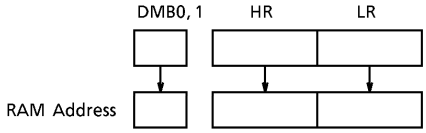
Directly specify an address in the bank using the 8 bits (operand) in the instruction field.
(Example)

LDI 2CH, 0AH : RAM (2CH) ← AH

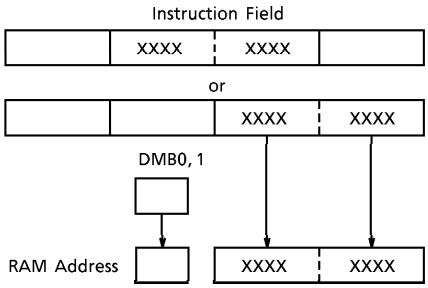
(3) Index addressing mode (Fig.4 (c))

Specify an address in the page using the sum of the LRegister contents and the 4 bits (operand) in the instruction field.
(Example)

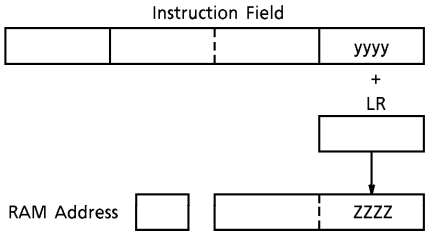
LDRI 4H, 3H : RAM (HL + 4)
← RAM (3H, L)
L ← L + 1, A ← A − 1



(a) Indirectly Addressing



(b) Directly Addressing



(c) Index Addressing

Fig.4 Addressing mode

(4) Bank selector

F-REGISTER		BANK SWITCHING
BIT 3	BIT 2	
DMB0	DMB1	
0	0	Bank 0
1	0	Bank 1
0	1	Bank 2
1	1	Bank 3

Pages 8 to F in Bank 0 can be used as a stack.
When using the CALL / CALLS instruction, or when the interrupt request occurred, the current contents of the program counter and the program memory bank are stored on the stack.
The program returns using the RET instruction to the return address stored on the stack.
The PUSH instruction is used to store register data, two 8 bit registers at a time, in the stack.
The POP instruction is used to return the data to the registers.
The size of the stack is up to 64 bits (0 to 64), with each stack consisting of 8 bits.

3. Data RAM

JTMP04030-XXXS has a 4 Kbit data RAM (256 addresses × 2 banks × 8 bits). Addressing and data read / write is done using the register file as follows.

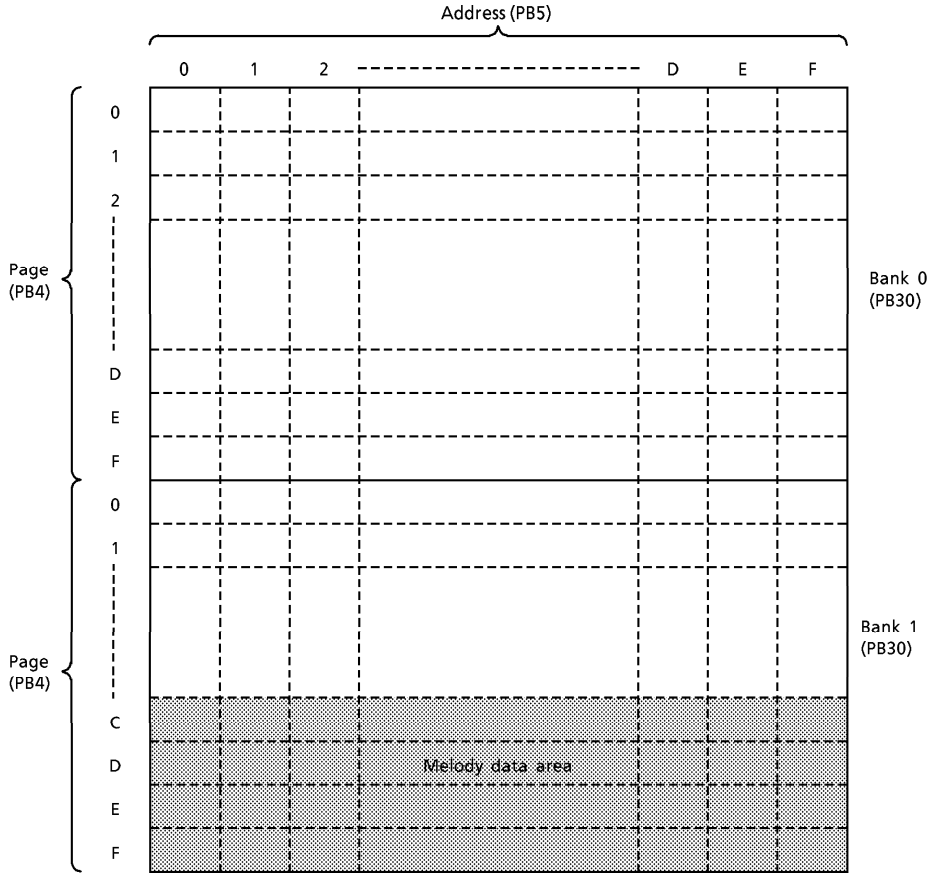


Fig.5 Data RAM

Before writing / reading data to / from data RAM, CE (PB00) must be set to 1. Before executing the HALT instruction, CE (PB00) must be set to 0.

	3	2	1	0
PB0				CE
Initial Value				0

CE : 0-Disables data RAM.
1-Enables data RAM.

The addresses of data RAM are set using RAB (PB31), RAR 1 to RAR4 (PB4), and RAC1 to RAC4 (PB5).

Bank :

	3	2	1	0
PB3				RAB
Initial Value				0

RAB : 0 Selects bank 0.
1 Selects bank 1.

Page :

	3	2	1	0
PB4	RAR4	RAR3	RAR2	RAR1
Initial Value	0	0	0	0

RAR1 to RAR4 : Set page in a Bank.

Address :

	3	2	1	0
PB5	RAC4	RAC3	RAC2	RAC1
Initial Value	0	0	0	0

RAC1 to RAC4 : Set addresses in a page.

Data at the addresses specified by the bank, page, and address registers are read / written through RAD1 to RAD8 (PB6, PB7).

Since data are read / written in units of 8 bits, use 8 bit transfer instructions, not 4 bit transfer instructions.

Setting AINC (PA23) to 1 increments by 1 the address in a bank every after data writing / reading. This is useful for continuous data write or read. Note that at auto increment on, write must be performed after one cycle or more. Continuous write does not automatically increment the address.

	3	2	1	0
PB6	RAD4	RAD3	RAD2	RAD1
Initial Value	*	*	*	*
PB7	RAD8	RAD7	RAD6	RAD5
Initial Value	*	*	*	*

* : Undefined
RAD1 to RAD8 : 8 bit data at the address specified by the data RAM bank, page, and address registers.

	3	2	1	0
PA2	AINC		WDT2	WDT1
Initial Value	0		0	0

AINC : 0-Auto increment OFF
1-Auto increment ON

4. Display RAM

JTMP04030-XXXS incorporates display RAM. Data are set and addressing is performed using the register file. Before writing or reading display RAM, DRCE (PC32) must be set to 1. Before executing a HALT instruction, DRCE (PC32) must be set to 0.

	3	2	1	0
PC3	LOWCP	DRCE	DON	DSTA
Initial Value	0	0	0	0

DRCE : 0-Disables display RAM.
1-Enables display RAM.

Addresses in display RAM are set using DRR1 to DRR4 (PC4) and DRC1 to DRC3 (PC5). (DRR1 is the least significant bit, DRC3 the most significant bit)

	3	2	1	0
PC4	DRR4	DRR3	DRR2	DRR1
Initial Value	0	0	0	0
PC5		DRC3	DRC2	DRC1
Initial Value		0	0	0

DRR1 to DRR4, DRC1 to DRC3 : Used to set addresses in display RAM.

Data DRD1 to DRD8 (PC6, PC7) are read from / written to the specified address. Since data are read / written in units of 8 bits, use 8 bit transfer instructions, not 4 bit transfer instructions.

	3	2	1	0
PC6	DRD4	DRD3	DRD2	DRD1
Initial Value	*	*	*	*
PC7	DRD8	DRD7	DRD6	DRD5
Initial Value	*	*	*	*

* : Undefined
DRD1 to DRD8 : 8 bit data in display RAM

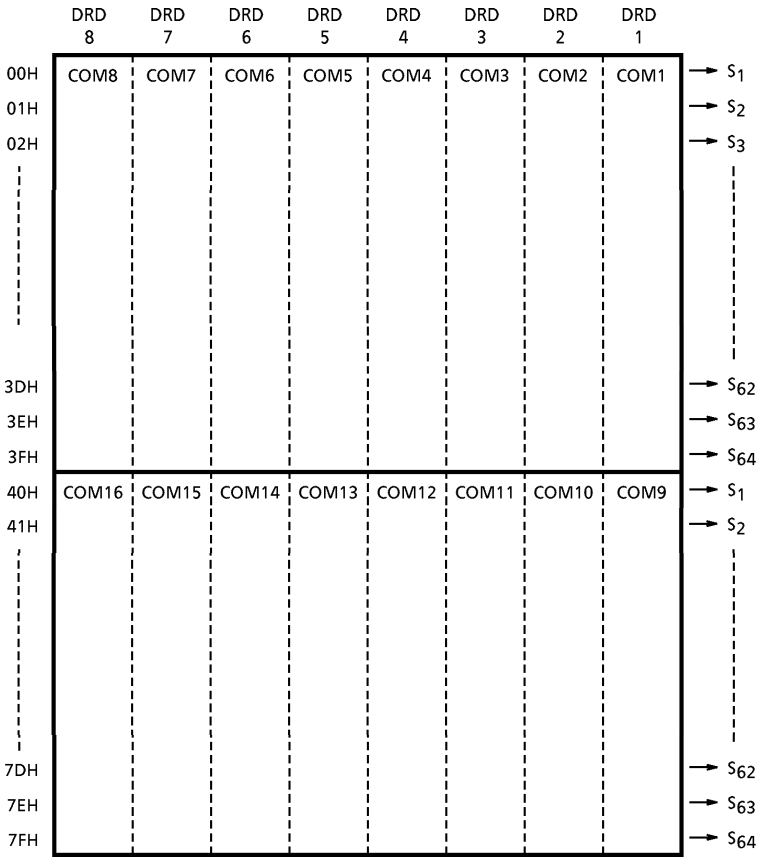
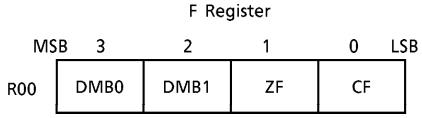


Fig.6 Display RAM

REGISTER FILE

The register file contains general registers and peripheral circuit control registers.

1. Flag (F) register (R00)

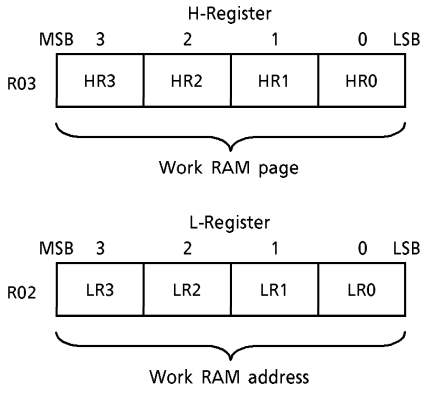


CF : Carry flag
ZF : Zero flag
DMB1 :
DMB0 : } Select work RAM bank.

DMB0	DMB1	WORK RAM BANK
0	0	Bank 0
1	0	Bank 1
0	1	Bank 2
1	1	Bank 3

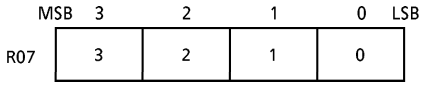
2. Accumulator (A) register (R01)
3. H-, L-register (R03, R02)

   The H- and L-registers are used to set work RAM addresses in the bank specified by DMB.



4. Bank (B) register (R07)

The B register is used as a ROM page.



0000 = page 0
0001 = page 1
0010 = page 2
0011 = page 3
0100 = page 4
0101 = page 5
0110 = page 6
0111 = page 7

5. D-register, E-register, P-register

D-, E- and P- are general-purpose registers (R05, R04, R06).
When using ROM as a data table, the B-, P-, D-, and E-registers are used to set ROM addresses.
(Data table function : The user can store constants in ROM in advance and access the constants using the LDBL and LDBH instructions.)

REGISTER FILE

PAGE (RFB)	ADDRESS		0		1		2		3		4		5		6		7	
	8-BIT ADDRESS		0				2				4				6			
			Lower4-BIT		Upper4-BIT		Lower4-BIT		Upper4-BIT		Lower4-BIT		Upper4-BIT		Lower4-BIT		Upper4-BIT	
	R/W		READ	WRITE	READ	WRITE	READ	WRITE	READ	WRITE	READ	WRITE	READ	WRITE	READ	WRITE	READ	WRITE
0	MSB	BIT 3	F-REGISTER		A-REGISTER		L-REGISTER		H-REGISTER		E-REGISTER		D-REGISTER		P-REGISTER		B-REGISTER	
		BIT 2																
		BIT 1																
	LSB	BIT 0																
1 (R1x)	MSB	BIT 3	STACK POINTER (SP)		0		INT2E		INT6E		IOD14	IOO14	IOD24	IOO24				
		BIT 2					INT1E		INT5E		IOD13	IOO13	IOD23	IOO23				
		BIT 1					INT0E		INT4E		IOD12	IOO12	IOD22	IOO22				
	LSB	BIT 0	0				0		INT3E		IOD11	IOO11	IOD21	IOO21				
2 (PAx)	MSB	BIT 3	IND04		IOD04	IOO04	AINC		TIS4		TIE4				TI4			TIR4
		BIT 2	IND03		IOD03	IOO03			TIS3		TIE3				TI3			TIR3
		BIT 1	IND02		IOD02	IOO02	WDT2		TIS2		TIE2		FLSEL		TI2			TIR2
	LSB	BIT 0	IND01		IOD01	IOO01	WDT1		TIS1		TIE1		TSTOP		TI1			TIR1
3 (PBx)	MSB	BIT 3									RAR4		RAC4		RAD4		RAD8	
		BIT 2									RAR3		RAC3		RAD3		RAD7	
		BIT 1									RAR2		RAC2		RAD2		RAD6	
	LSB	BIT 0	CE						RAB		RAR1		RAC1		RAD1		RAD5	
4 (PCx)	MSB	BIT 3	ERA4		ERD4		CKG2		LOWCP		DRR4				DRD4		DRD8	
		BIT 2	ERA3		ERD3		CKG1		DRCE		DRR3		DRC3		DRD3		DRD7	
		BIT 1	ERA2		ERD2		CPMODE2		DON		DRR2		DRC2		DRD2		DRD6	
	LSB	BIT 0	ERA1		ERD1		CPMODE1		DSTA		DRR1		DRC1		DRD1		DRD5	
5 (PDx)	MSB	BIT 3	IIE4		IOE4		SINE						MINE		MADR14			
		BIT 2	IIE3		IOE3		SSTA				CRYO		REPLY		MADR13			
		BIT 1	IIE2		IOE2		SRSEL				CRYS		MPM2		MADR12		MADR16	
	LSB	BIT 0	IIE1		IOE1		SIO				MLSEL		MPM1		MADR11		MADR15	
6 (PEx)	MSB	BIT 3	IINT4	IIL4	ION4	IOL4	TCR14		TCR18		TCR24		TCR28		MADR24			
		BIT 2	IINT3	IIL3	ION3	IOL3	TCR13		TCR17		TCR23		TCR27		MADR23			
		BIT 1	IINT2	IIL2	ION2	IOL2	TCR12		TCR16		TCR22		TCR26		MADR22			
	LSB	BIT 0	IINT1	IIL1	ION1	IOL1	TCR11		TCR15		TCR21		TCR25		MADR21		MADR25	
7 (PFx)	MSB	BIT 3					TCFSL		TCPS		TC1EN		TC2EN		SDATA4		SDATA8	
		BIT 2					CKS13		CKS23			TC1R		TC2R	SDATA3		SDATA7	
		BIT 1	TC1EI		TC2EI		CKS12		CKS22		CMPEN1		CMPEN2		SDATA2		SDATA6	
	LSB	BIT 0		TC1RI		TC2RI	CKS11		CKS21		CHASEL		TCO		SDATA1		SDATA5	

(Note) Blank means undefined.

EXPANDED REGISTER FILE

PC0 ADDRESS	EXPANDED REGISTER NAME	PC1 DATA			
		3	2	1	0
00H	ER0	HCPON		P2	P1
01H	ER1	IISL4	IISL3	IISL2	IISL1
02H	ER2		IOSL13	IOSL12	IOSL11
03H	ER3		IOSL23	IOSL22	IOSL21
04H	ER4		IOSL33	IOSL32	IOSL31
05H	ER5		IOSL43	IOSL42	IOSL41
06H	ER6	SET14	SET13	SET12	SET11
07H	ER7	SET18	SET17	SET16	SET15
08H	ER8	SET24	SET23	SET22	SET21
09H	ER9	SET28	SET27	SET26	SET25
0AH	ERA	IO1S4	IO1S3	IO1S2	IO1S1
0BH	ERB	IO2S4	IO2S3	IO2S2	IO2S1
0CH	ERC		SIGC	SIGB	SIGA

PERIPHERAL CIRCUITS

Peripheral circuits can be read / written / set via the register file.

1. Oscillator Block

The CPU clock is generated by the oscillator circuits as an asynchronous low-speed or a high-speed clock.

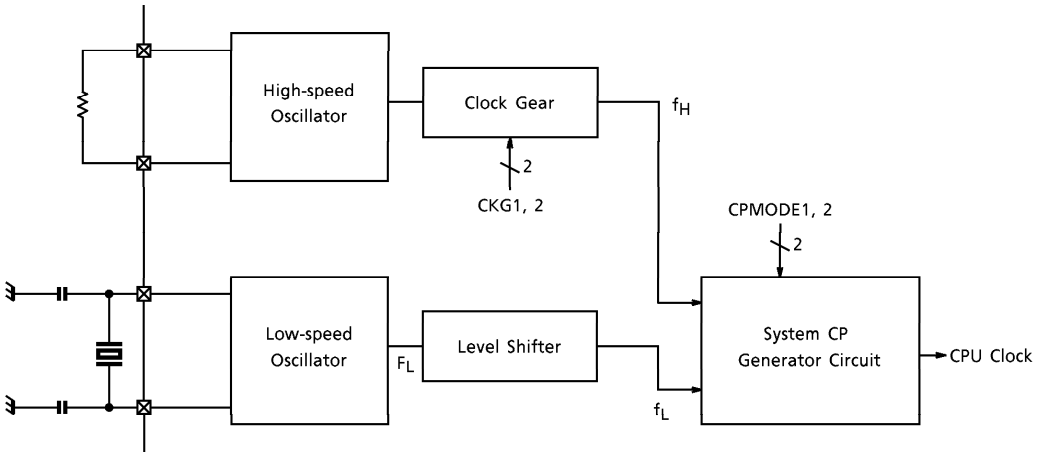


Fig.7 Oscillator Block

	3	2	1	0
PC2	CKG2	CKG1	CPMODE2	CPMODE1
Initial Value	0	0	1	1

CPMODE1, 2 : Set oscillator mode.
CKG1, 2 : Set high-speed oscillation divider.

Oscillator modes are controlled by CPMODE1 (PC20) AND CPMODE2 (PC21) of the register file.

CPMODE 2	CPMODE 1	LOW-SPEED OSCILLATOR	HIGH-SPEED OSCILLATOR	SYSTEM CP	MODE NAME	
0	0	OFF	OFF	OFF	(CPM0)	
0	1	ON	OFF	Low-speed	(CPM1)	
1	0	OFF	ON	High-speed	(CPM2)	
1	1	ON	ON	High-speed	(CPM3)	(Initial value)

The high-speed oscillation divider are controlled by CKG1 (PC22) and CKG2 (PC23) of the register file. Signals divided by the divider are supplied to the system CP generator circuit and peripheral circuits such as the timer / counter.

CKG2	CKG1	DIVISOR	
0	0	Source clock	(Initial value)
0	1	1 / 2	
1	0	1 / 4	
1	1	1 / 8	

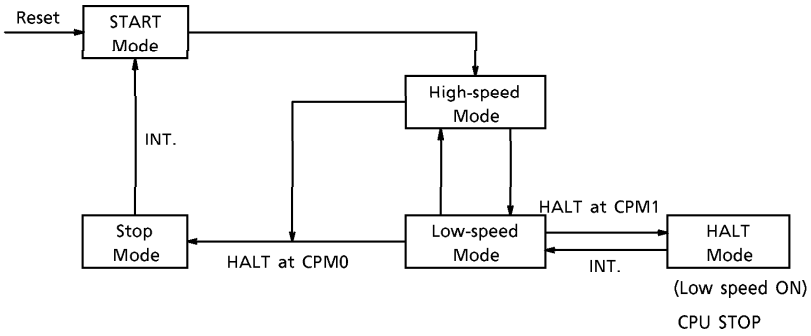


Fig.8 Mode Status

CAUTIONS

1. Do not set the system CP to low-speed when the low-speed oscillator is not in operation or before the oscillator is stable.
2. Do not set the system CP to high-speed when the high-speed oscillator is not in operation or before the oscillator is stable.
3. The low-speed oscillator circuit has a warm-up function. However some crystal oscillators do not start oscillating within the warm-up time decided by hardware-timer. Thus, in order to start the low-speed oscillator, take appropriate warm-up time using soft ware-timer.
4. Executing an instruction to change from CPM1 / 2 / 3 to CPM0 does not actually change to CPM0. The mode changes to Stop after a HALT instruction is executed.

2. Interrupt function

Interrupts are triggered by IN1 to IN4, IO01 to IO04, timing, timer/counter, melody, or SIO.

(Interrupt priority)

The interrupt priority is specified by P1 (ER00) and P2 (ER01) of the expanded register file.

	3	2	1	0
ER0	HCPON		P2	P1
Initial Value	0		0	0

P2	P1	INT0	INT1	INT2	INT3	INT4	INT5	INT6
0	0	IINT	IOINT	TIN	TCIN1	TCIN2	MIN	SIN
0	1	TIN	IINT	IOINT	TCIN1	TCIN2	MIN	SIN
1	0	TCIN1	TCIN2	IINT	IOINT	TIN	MIN	SIN
1	1	SIN	TCIN1	TCIN2	IINT	IOINT	TIN	MIN

(high) ← priority → (low)

(IINT : IN1 to IN4, IOINT : IO01 to IO04, TIN : timing
TCIN1 : timer / counter 1, TCIN2 : timer / counter 2
MIN : melody, SIN : SIO)

(Interrupt enable / disable)

Interrupts (IINT, IOINT, TIN, TCIN1, TCIN2, MIN, SIN) are enabled / disabled as follows:

IINT : IIE1~4
IOINT : IOE1~4
TIN : TINE
TCIN1 : TC1E
TCIN2 : TC2E
MIN : MINE
SIN : SINE

Interrupts with priority by P1 and P2 are enabled / disabled by INT0 to INT6.
At initial settings, disable interrupts which are not required, using IIE1 to IIE4, IOE1 to IOE4, TINE, TC1E, TC2E, MINE, or SINE.

	3	2	1	0
R12	INT2	INT1	INT0	
Initial Value	0	0	0	
R13	INT6	INT5	INT4	INT3
Initial Value	0	0	0	0

INT0 to INT6 : 0-Disables an interrupt
1-Enables an interrupt

(Interrupt reset)

After an interrupt generation is detected, reset the interrupt as follows:
First, reset the interrupt latch by disabling the interrupt using the interrupt enable / disable register, then reset the core interrupt latch circuit by setting interrupt enable / disable using R12 or R13 of the register file.

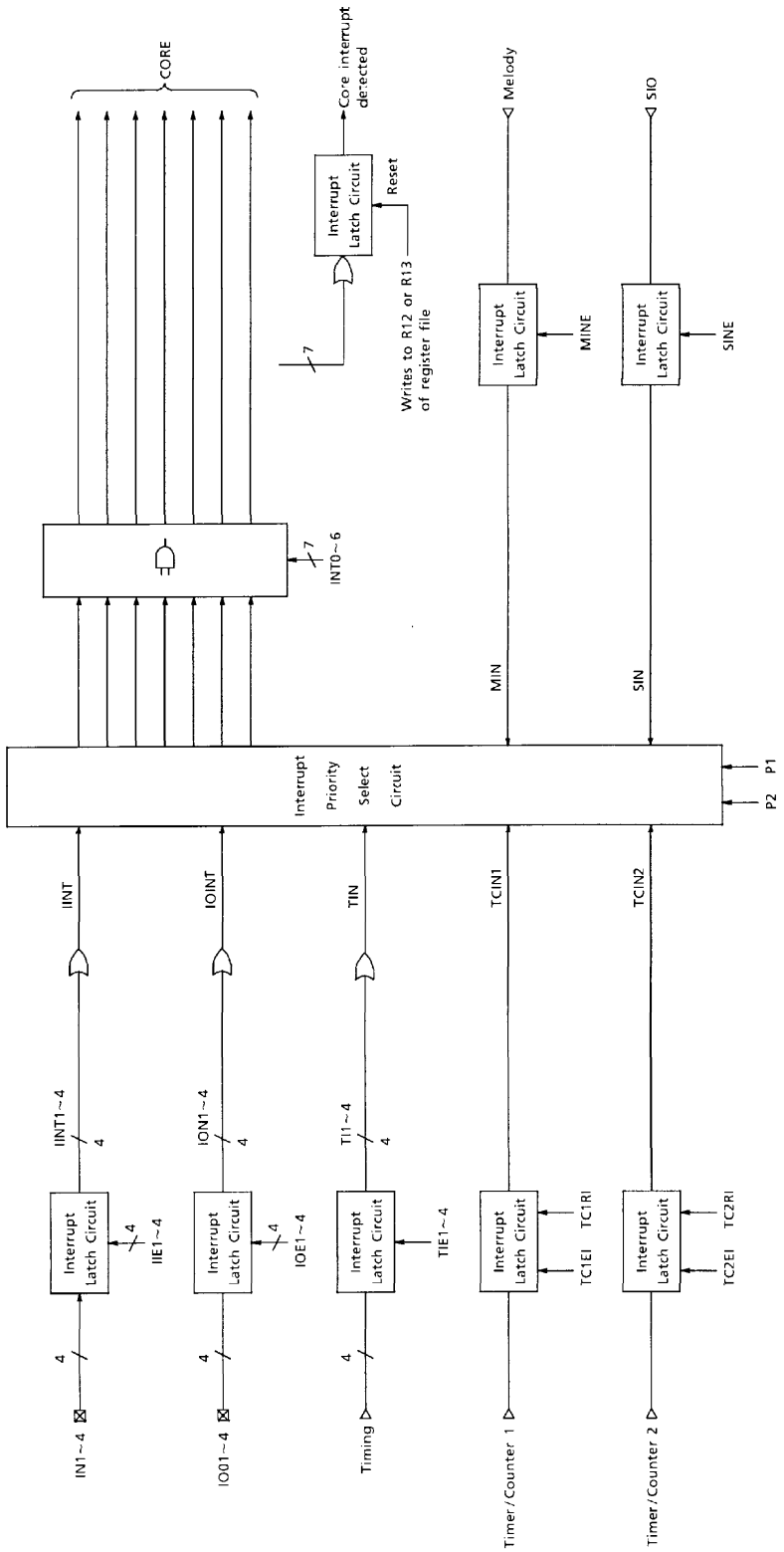


Fig.9 Block Diagram of Interrupt Circuit Configuration

2-1. IN Interrupt

(Interrupt enable / disable)

	3	2	1	0
PD0	IIE4	IIE3	IIE2	IIE1
Initial Value	0	0	0	0

IIE1 to IN4 : 0-Disables an interrupt
1-Enables an interrupt

Disabling interrupts resets also the interrupt data.

(Interrupt data read)

	3	2	1	0
PE0 (R)	IINT4	IINT3	IINT2	IINT1
Initial Value	0	0	0	0
PE0 (W)	IIL4	IIL3	IIL2	IIL1
Initial Value	0	0	0	0

IINT1 to IN4 : Interrupt data
0-No interrupt
1-Interrupt generated

IIL1 to IN4 : Interrupt level / edge select
0-High-level interrupt
1-Rising-edge interrupt

* Detecting a high-level interrupt requires the input pin to remain at high level for two or more cycles of the low-speed clock.
Even when level interrupt is selected, an edge interrupt latch holds interrupt data. Thus, when the interrupt type is changed from level to edge, interrupts must be cleared (disabled).

2-2. IO0 Interrupt

(Interrupt enable / disable)

	3	2	1	0
PD1	IOE4	IOE3	IOE2	IOE1
Initial Value	0	0	0	0

IOE1 to IOE4 : 0-Disables an interrupt
1-Enables an interrupt

Disabling interrupts resets the interrupt data.

(Interrupt data read)

	3	2	1	0
PE1 (R)	ION4	ION3	ION2	ION1
Initial Value	0	0	0	0
PE1 (W)	IOL4	IOL3	IOL2	IOL1
Initial Value	0	0	0	0

ION1 to ION4 : Interrupt data
0-No interrupt
1-Interrupt generated

IOL1 to ION4 : Interrupt level / edge select
0-High-level interrupt
1-Rising-edge interrupt

* Detecting a high-level interrupt requires the IO pin to remain at high level for two or more cycles of the low-speed clock. Even when level interrupt is selected, an edge interrupt latch holds interrupt data. Thus, when the interrupt type is changed from level to edge, interrupts must be cleared (disabled).

2-3. Timing Interrupt

(Interrupt select)

	3	2	1	0
PA3	TIS4	TIS3	TIS2	TIS1
Initial Value	0	0	0	0

TIS1 : 0-Selects a 128 Hz interrupt
1-Selects a 256 Hz interrupt
TIS2 : 0-Selects a 16 Hz interrupt
1-Selects a 32 Hz interrupt
TIS3 : 0-Selects a 4 Hz interrupt
1-Selects a 8 Hz interrupt
TIS4 : 0-Selects a 1 Hz interrupt
1-Selects a 2 Hz interrupt

Before changing the frequency of timing interrupts, disable the interrupts.

(Interrupt enable / disable)

	3	2	1	0
PA4	TIE4	TIE3	TIE2	TIE1
Initial Value	0	0	0	0

TIE1 : 0-Disables a 128 / 256 Hz interrupt
1-Enables a 128 / 256 Hz interrupt
TIE2 : 0-Disables a 16 / 32 Hz interrupt
1-Enables a 16 / 32 Hz interrupt
TIE3 : 0-Disables a 4 / 8 Hz interrupt
1-Enables a 4 / 8 Hz interrupt
TIE4 : 0-Disables a 1 / 2 Hz interrupt
1-Enables a 1 / 2 Hz interrupt

Disabling interrupts resets also the interrupt data.

2-4. Timer / Counter 1, 2 Interrupt

When either timer / counter 1 or 2 overflows or a match with the TIME / COUNT set value occurs, the corresponding interrupt is generated.

	3	2	1	0
PF0			TC1EI	TC1RI
Initial Value			0	0

TC1EI : 0-Disables a timer / counter 1 interrupt
1 -Enables a timer / counter 1 interrupt
TC1R : ⎍ Resets timer / counter 1 interrupt data

	3	2	1	0
PF1			TC2EI	TC2RI
Initial Value			0	0

TC2EI : 0-Disables a timer / counter 2 interrupt
1-Enables a timer / counter 2 interrupt
TC2RI : ⎍ Resets timer / counter 2 interrupt data

When timer / counters 1 and 2 are linked to make a 16 bit timer / counter, a timer / counter 1 interrupt only can occur, but a timer / counter 2 interrupt cannot. In such a case, the settings in TC2EI and TC2RI are invalid. The 16 bit timer / counter is controlled by settings in TC1EI and TC1RI.

2-5. Melody Interrupt

An interrupt occurs at the end of playing melodies.

	3	2	1	0
PD5	MINE	REPLY	MPM2	MPM1
Initial Value	0	0	0	0

MINE : 0-Disables a melody interrupt
1-Enables a melody interrupt

2-6. 8 bit Serial Transfer Interrupt

An interrupt occurs at the end of serial transfer.

	3	2	1	0
PD2	SINE	SSTA	SRSEL	SIO
Initial Value	0	0	0	0

SINE : 0-Disables an 8 bit serial transfer interrupt
1-Enables an 8 bit serial transfer interrupt

3. Timing Circuit

Timings are generated using the low-speed clock as the source clock. Interrupts are generated at timings selected by PA3 of the register file.

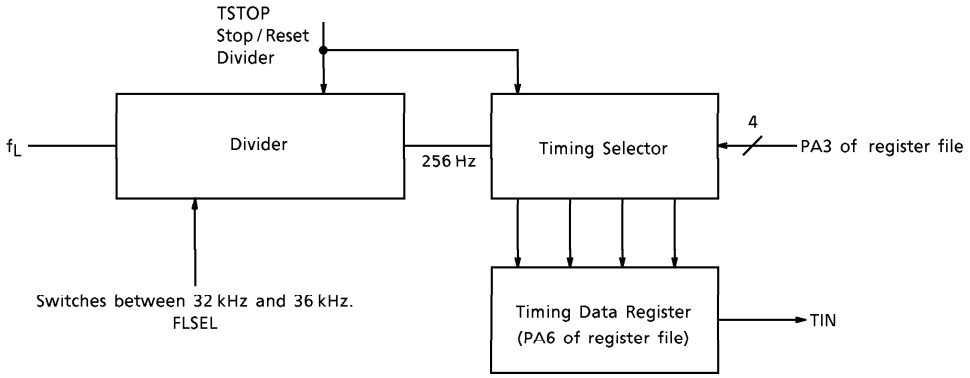


Fig.10 Block Diagram of Timing Signal Supply

	3	2	1	0
PA5			FLSEL	TSTOP
Initial Value			0	0

TSTOP : 0-Resets and stops the entire timing circuit.
Also stops supplying clocks to the melody circuit.
1-Timing circuit operates
FLSEL : 0-When low-speed crystal is 32.768 kHz
1-When low-speed crystal is 36.864 kHz

Specify timing interrupt frequency in PA3 of the register file.

	3	2	1	0
PA3	TIS4	TIS3	TIS2	TIS1
Initial Value	0	0	0	0

TIS1 : 0-Selects a 128 Hz interrupt
1-Selects a 256 Hz interrupt
TIS2 : 0-Selects a 16 Hz interrupt
1-Selects a 32 Hz interrupt
TIS3 : 0-Selects a 4 Hz interrupt
1-Selects a 8 Hz interrupt
TIS4 : 0-Selects a 1 Hz interrupt
1-Selects a 2 Hz interrupt

The selected timing interrupts can be enabled, disabled, or reset using PA4 and PA7 of the register file. The occurrence of each Interrupts can be read using PA6 of the register file.

	3	2	1	0
PA4	TIE4	TIE3	TIE2	TIE1
Initial Value	0	0	0	0

TIE1 : 0-Disables a 128 / 256 Hz interrupt
1-Enables a 128 / 256 Hz interrupt
TIE2 : 0-Disables a 16 / 32 Hz interrupt
1-Enables a 16 / 32 Hz interrupt
TIE3 : 0-Disables a 4 / 8 Hz interrupt
1-Enables a 4 / 8 Hz interrupt
TIE4 : 0-Disables a 1 / 2 Hz interrupt
1-Enables a 1 / 2 Hz interrupt

	3	2	1	0
PA7 (W)	TIR4	TIR3	TIR2	TIR1
Initial Value	0	0	0	0

TIR1 : Clears 128 / 256 Hz interrupt data
TIR2 : Clears 16 / 32 Hz interrupt data
TIR3 : Clears 4 / 8 Hz interrupt data
TIR4 : Clears 1 / 2 Hz interrupt data.
Clears interrupt data at write (⎍).
Clear status is not held.

	3	2	1	0
PA6 (R)	TI4	TI3	TI2	TI1
Initial Value	0	0	0	0

TI1 : 128 / 256 Hz interrupt data
TI2 : 16 / 32 Hz interrupt data
TI3 : 4 / 8 Hz interrupt data
TI4 : 1 / 2 Hz interrupt data.
0-No interrupt
1-Interrupt generated

4. Timer / Counter Circuit

The timer / counter circuit can be used as an 8 bit × 2-channel or 16 bit × 1-channel timer / counter. The timer / counter can also be used as general-purpose timer / counter or multi interrupts. The circuit can be switched between 8 and 16 bits using TCPS (PF34) of the register file. The source clock can be selected from low-speed, high-speed, or external clock.

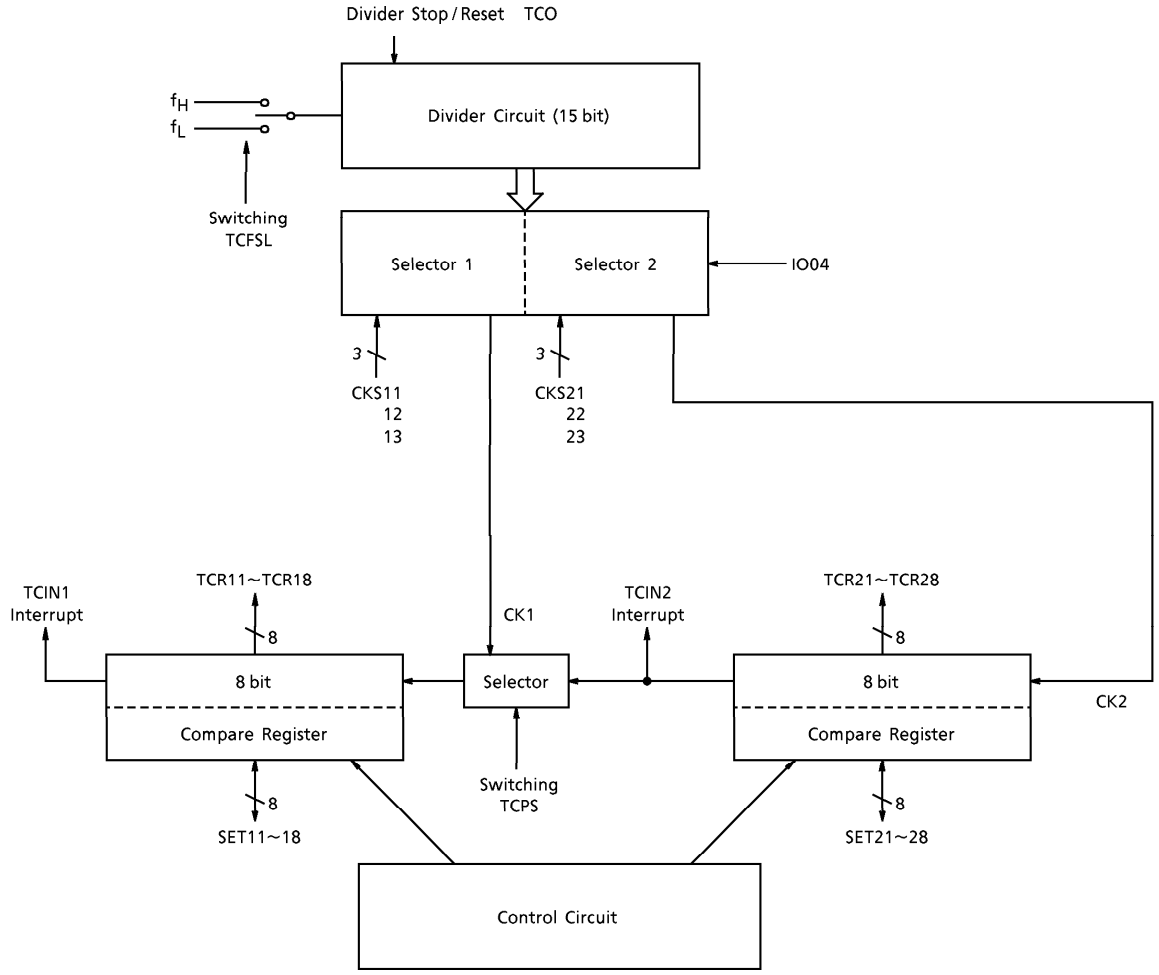


Fig.11 Block Diagram of Timer / Counter

Timer / counter source clock frequencies are selected as below:

	3	2	1	0
PF2	TCFSL	CKS13	CKS12	CKS11
Initial Value	0	0	0	0
PF3	TCPS	CKS23	CKS22	CKS21
Initial Value	0	0	0	0

TCPS : 0-8 bit timer / counter × 2-channel
1-16 bit timer / counter × 1-channel
TCFSL : Timer source clock frequency select 0-Low-speed (f_L)
1-High-speed (f_H)

CKS11 to CKS13
CKS21 to CKS 23
} Timer / counter 1, 2 source clock select

SOURCE CLOCK SELECT BIT			SELECTED DIVISOR	SOURCE CLOCK FREQUENCY	
CKS13	CKS12	CKS11		TCFSL = 0 f_L = 32.768 kHz	TCFSL = 1 f_H = 2 MHz
0	0	0	2^{15}	1 Hz	61.0 Hz
0	0	1	2^{13}	4 Hz	244 Hz
0	1	0	2^{11}	16 Hz	977 Hz
0	1	1	2^{9}	64 Hz	3.91 kHz
1	0	0	2^{7}	256 Hz	15.6 kHz
1	0	1	2^{5}	1024 Hz	62.5 kHz
1	1	0	2^{3}	4096 Hz	250 kHz
1	1	1	2^{1}	16.384 kHz	1.00 MHz
CKS23	CKS22	CKS21	SELECTED DIVISOR	TCFSL = 0 f_L = 32.768 kHz	TCFSL = 1 f_H = 2 MHz
0	0	0	2^{15}	1 Hz	61.0 Hz
0	0	1	2^{13}	4 Hz	244 Hz
0	1	0	2^{11}	16 Hz	977 Hz
0	1	1	2^{9}	64 Hz	3.91 kHz
1	0	0	2^{7}	256 Hz	15.6 kHz
1	0	1	2^{5}	1024 Hz	62.5 kHz
1	1	0	2^{3}	4096 Hz	250 kHz
1	1	1	IO04 input signal is selected		

* When the source clock is changed, the timer / counter may count incorrectly. After changing the source clock, reset the timer / counter.

Timer / counter is controlled by PF4 and PF5 of the register file.

	3	2	1	0
PF4	TC1EN	TC1R	CMPEN1	CHASEL
Initial Value	0	0	0	0
PF5	TC2EN	TC2R	CMPEN2	TCO
Initial Value	0	0	0	0

CHASEL : 0- Eliminates chattering of IO04 signal
1- Does not eliminate chattering of IO04 signal
CMPEN1 : 0- Generates an interrupt when timer / counter 1 overflows
1- Generates an interrupt when timer / counter 1 value matches the target value
TC1R : 1- Resets (Clears) timer / counter 1. After reset, counting restarts
TC1EN : 0- Stops source clock input to timer / counter 1
1- Starts source clock input to timer / counter 1
TCO : 0- Stops the divider circuit for supplying source clock
1- Starts the divider circuit for supplying source clock
CMPEN2 : 0- Generates an interrupt when timer / counter 2 overflows
1- Generates an interrupt when timer / counter 2 value matches the target value
TC2R : 1- Resets (Clears) timer / counter 2. After reset, counting restarts
TC2EN : 0- Stops source clock input to timer / counter 2
1- Stops source clock input to timer / counter 2

* When a 16-bit single-channel timer / counter is selected (i.e. when PF3 <TCPS> = 1), it can be controlled using PF4 (TC1EN, CMPEN1) of Timer Control Register 1 and PF5 (TC2R) of Timer Control Register 2. PF4 (TC1R) of timer Control Register 1 and PF5 (TC2EN, CMPEN2) are not used in this case.
The 8-bit and 16-bit counters both have a margin for error of one source clock cycle (CK1 or CK2).

Timer / counter 1 / 2 data can be read from PE2, PE3, and PE4 of the register file.

	3	2	1	0
PE2	TCR14	TCR13	TCR12	TCR11
Initial Value	0	0	0	0
PE3	TCR18	TCR17	TCR16	TCR15
Initial Value	0	0	0	0
PE4	TCR24	TCR23	TCR22	TCR21
Initial Value	0	0	0	0
PE5	TCR28	TCR27	TCR26	TCR25
Initial Value	0	0	0	0

Timer / counter 1 / 2 compare data are set using ER6, ER7, ER8, and ER9 of the expanded register file.

	3	2	1	0
ER6	SET14	SET13	SET12	SET11
Initial Value	0	0	0	0
ER7	SET18	SET17	SET16	SET15
Initial Value	0	0	0	0
ER8	SET24	SET23	SET22	SET21
Initial Value	0	0	0	0
ER9	SET28	SET27	SET26	SET25
Initial Value	0	0	0	0

(Notes)

1. To detect a match between the timer / counter value and the target value (SET11 to SET18, SET21 to SET28), first set the values in the expanded register file (ER6, ER7, ER8, and ER9), then set CMPEN1 / 2 to 1 (Match Detect mode).
2. When a 16 bit timer / counter is configured by linking timer / counters 1 and 2, and interrupts condition is set to match detection, set CMPEN1, CMPEN2, TC1EN, and TC2EN to 1.
3. When system clock is switched from low to high or vice versa using TCFSL, or the source clock is switched using CKS11 to CKS13 and CKS21 to CKS23 while a timer / counter is in operation, countup may malfunction.
   Before switching, set TC1EN and TC2EN to 0 (stop the source clock).
4. Do not use TCPS to switch between 8 bit and 16bit timer / counters while a timer / counter is in operation, or data may be destroyed.
5. Timer / counter source clock and control instructions are asynchronous; thus, time is measured to a tolerance of up to 1 count of the source clock.

JTMP04030-XXXS incorporates a one-channel independent dedicated watchdog timer. Watchdog time can be selected from 32.768 kHz, 0.5, 1.0, or 2.0 seconds. Writing to PA2 of the register file clears the watchdog timer.

	3	2	1	0
PA2	AINC		WDT2	WDT1
Initial Value	0		0	0

WDT2	WDT1	OPERATION
0	0	Stop
0	1	Resets system at 0.5 s
1	0	Resets system at 1.0 s
1	1	Resets system at 2.0 s

(At 32.768 kHz of low-speed clock)

* To run the watchdog timer, the timing circuit must be run.

5. LCD Circuit

The display status and duty of the LCD driver are set using PC3 of the register file and ERC of the expanded register file. Display duty can be selected from 1/8, 1/10, or 1/16.
JTMP04030-XXXS incorporates a 5 × doubler circuit for supplying power to the LCD drivers.

DUTY	FRAME FREQUENCY	COMMON	SEGMENT
1/8	97.5 Hz	COM1~COM8	S_1~S_{64}
1/10	117.0 Hz	COM1~COM10	S_1~S_{64}
1/16	97.5 Hz	COM1~COM16	S_1~S_{64}

The LCD driver circuits are controlled by DSTA (PC30) and DON (PC31) of PC3 of register file. Access to display RAM is enabled/disabed using DRCE (PC32).

	3	2	1	0
PC3	LOWCP	DRCE	DON	DSTA
Initial Value	0	0	0	0

DSTA : 0-Fixes all commons and segments to V_{SS} level
1-Normal display possible
DON : 0-Sets the 5 × doubler circuit to off
1-Sets the 5 × doubler circuit to on
DRCE : 0-Disable display RAM
1-Enable display RAM
LOWCP : 0-Stop supplying the low speed clock to the LCD driver
1-Supply the low speed clock to the LCD driver

The display duty is selected using SIGA (ERC0), SIGB (ERC1), and SIGC (ERC2) of ERC of the expanded register.

	3	2	1	0
ERC		SIGC	SIGB	SIGA
Initial Value		0	0	0

SIGC	SIGB	SIGA	Duty
1	0	0	1/8
0	1	1	1/10
0	0	0	1/16

(Note) Do not set other than the above.

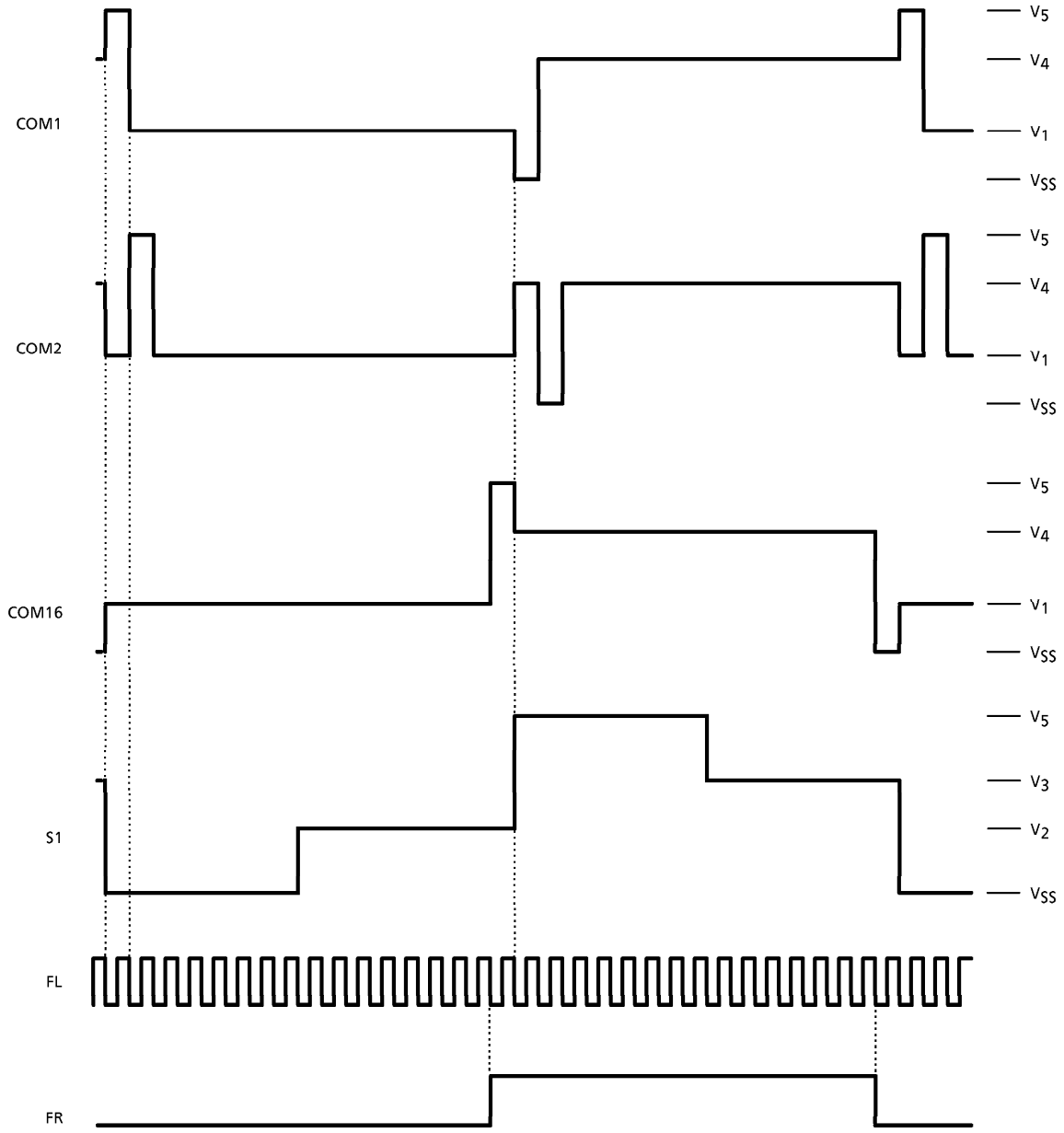


Fig.12 1 / 16 Duty Display Output Waveform

(Note 1) When the low-speed oscillator is not operating, display is not output even if the high-speed oscillator is operating.

(Note 2) DON and DSTA of PC3 of the register file are read into the LCD circuit according to the clock generated by display clock LOWCP. Therefore, after DON and DSTA are updated, LOWCP (PC33) must be set to off after up to 103 ms (32.768 kHz of low-speed clock).

6. Melody Circuit

The melody is automatically played according to the melody data stored in data RAM.

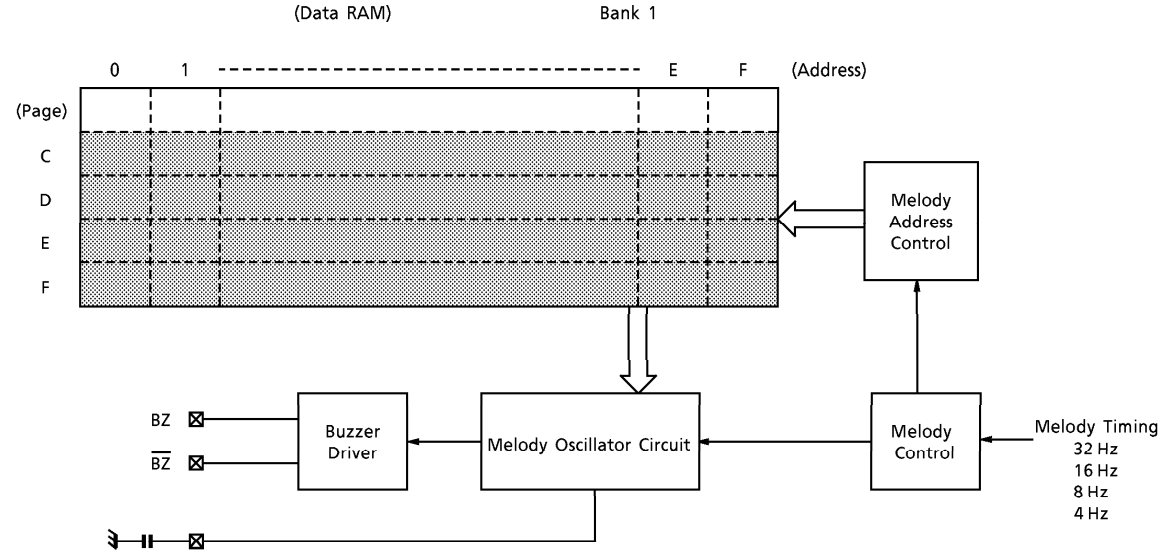


Fig.13 Melody Play Block

Set Melody Play mode using PD5 of the register file; set the play start address using PD6, PD7, PE6, and PE7 of the register file.

	3	2	1	0
PD4		CRYO	CRYS	MLSEL
Initial Value		0	0	0
PD5	MINE	REPLY	MPM2	MPM1
Initial Value	0	0	0	0
PD6	MADR14	MADR13	MADR12	MADR11
Initial Value	0	0	0	0
PD7			MADR16	MADR15
Initial Value			0	0
PE6	MADR24	MADR23	MADR22	MADR21
Initial Value	0	0	0	0
PE7				MADR25
Initial Value				0

CRYS : 0 ; Melody mode
1 ; Remote Control mode

CRYO : 0 ; Sets the BZ output pin to Low
1 ; Outputs remote carrier (low-speed oscillation) from the BZ output pin
} In Remote Control mode

MLSEL : 0 ; Generates the scale from the melody oscillator
1 ; Generates the scale from the highspeed oscillator

MPM1, 2 : SET PLAY MODE

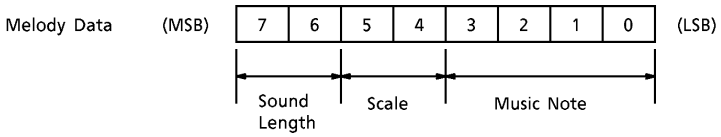
MPM2	MPM1	MODE	DESCRIPTION
0	0	STOP	Stops play
0	1	LONG	Continuous play up to 16 seconds. Start address: 11 000000 ~ 11 111111 C0H ↑ FFH ↑ └MADR11~6
1	0	SHORT1	Halves melody data area. While playing the SHORT1 area, music note data in the SHORT2 area can be modified. Start address: 110 00000 ~ 110 11111 C0H ↑ DFH ↑ └MADR11~5
1	1	SHORT2	Halves melody data area. While playing the SHORT2 area, music note data in the SHORT1 area can be modified. Start address: 111 00000 ~ 111 11111 E0H ↑ FFH ↑ └MADR21~5

REPLY : 0-Automatically shifts to Stop mode
1-Repeats play from start to end addresses in the same mode

MINE : 0-Disables melody interrupts
(also resets interrupt data MIN)
1-Enables melody interrupts

Note: Play stop (MPM 1,2 = 0) interval must be longer than five periods of low-speed clock.

Melody data consist of music note data (4 bit), scale data (2 bit), and sound length data (2 bit).



MUSIC NOTE		bit DATA
do	C	0100
	$C^{\#}$, D^{b}	0101
re	D	0110
	$D^{\#}$, E^{b}	0111
mi	E	1000
fa	F	1001
	$F^{\#}$, G^{b}	1010
sol	G	1011
	$G^{\#}$, A^{b}	1100
ra	A	1101
	$A^{\#}$, B^{b}	1110
si	B	1111
Mute		0000

SCALE	bit DATA	FREQUENCY
High	11	f_M
Mid-high	10	$f_M / 2$
Mid-low	01	$f_M / 4$
Low	00	$f_M / 8$

SOUND LENGTH	bit DATA
31.25 msec	00
62.5 msec	01
125 msec	10
250 msec	11

(at 32.768 kHz of low-speed clock)

7. 8 bit Serial Interface

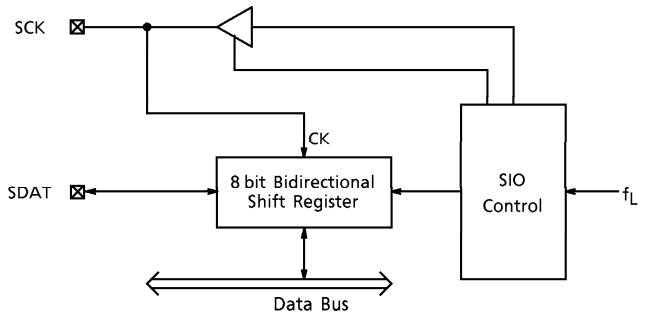
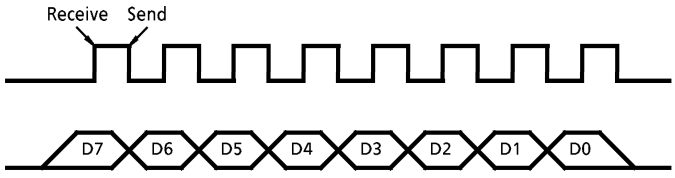


Fig.14 SIO Block

	3	2	1	0
PD2	SINE	SSTA	SRSEL	
Initial Value	0	0	0	
PF6	SDAT4	SDAT3	SDAT2	SDAT1
Initial Value	0	0	0	0
PF7	SDAT8	SDAT7	SDAT6	SDAT5
Initial Value	0	0	0	0

SRSEL : 0 -Receive mode
1 -Transmit mode
SSTA : -Starts serial transfer (in Transmit mode only)
SINE : 0 -Disables SIO interrupts (also resets interrupt data SIN)
1 -Enables SIO interrupts
SDAT1to SDAT8 : Serial transfer data

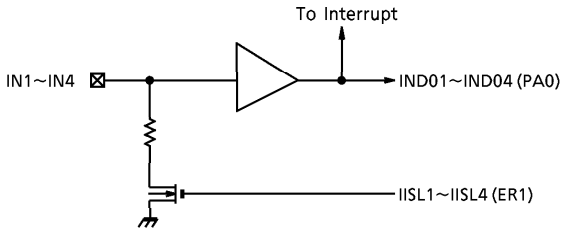
(Note) At transmission, set mode and transfer data, then start serial transfer (SSTA = 1).



8. Input / Output Ports

JTMP04030-XXXS has four input ports and 12 input / output ports.

8-1 IN pin



Input data can be read from PA0 of the register file.

	3	2	1	0
PA0	IND04	IND03	IND02	IND01
Initial value	0	0	0	0

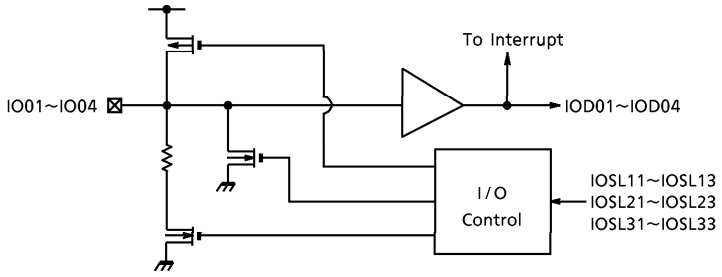
IND01 to IND04 : Input data
(*The initial values are when the IN1 to IN4 pins are open or connected to low-level (V_{SS}).)

The pull-down resistors of pins are set bit-wise.

	3	2	1	0
ER1	IISL4	IISL3	IISL2	IISL1
Initial value	0	0	0	0

IISL1 to IISL4 : 0-Connects pull-down resistors
1-No pull-down resistor

8-2 IO0 pin



Input / output data can be read or written using PA1 of the register file.

	3	2	1	0
PA1 (R)	IOD04	IOD03	IOD02	IOD01
Initial value	0	0	0	0
PA1 (W)	IOO04	IOO03	IOO02	IOO01
Initial value	0	0	0	0

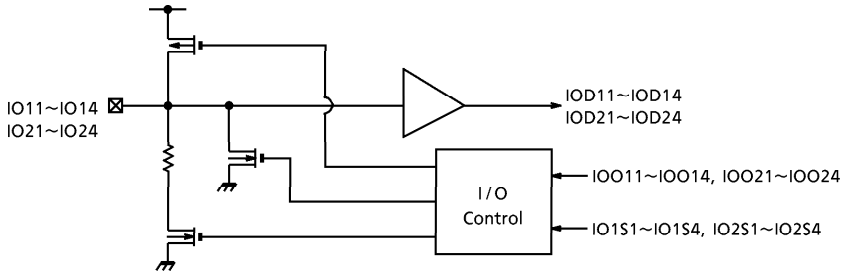
IOD01 to IOD04 : Input data
(*The initial values are when the IO01 to IO04 pins are open or connected to low-level (V_{SS}).)
IOO01 to IOO04 : Output data

Input / output formats for the pins are set bit-wise.

	3	2	1	0
ER2		IOSL13	IOSL12	IOSL11
Initial value		0	0	0
ER3		IOSL23	IOSL22	IOSL21
Initial value		0	0	0
ER4		IOSL33	IOSL32	IOSL31
Initial value		0	0	0
ER5		IOSL43	IOSL42	IOSL41
Initial value		0	0	0

IOSL*3	IOSL*2	IOSL*1	PORT FORMAT
0	0	0	Input with pull-down resistor
0	0	1	Input without pull-down resistor
0	1	0	CMOS output
0	1	1	Pch open drain output
1	0	0	Nch open drain output
1	0	1	CMOS output with pull-down resistor

8-3 IO1 and IO2 pins



Input / output data can be read or written using R14 and R15 of the register file.

	3	2	1	0
R14 (R)	IOD14	IOD13	IOD12	IOD11
Initial Value	0	0	0	0
R14 (W)	IOO14	IOO13	IOO12	IOO11
Initial Value	0	0	0	0
R15 (R)	IOD24	IOD23	IOD22	IOD21
Initial Value	0	0	0	0
R15 (W)	IOO24	IOO23	IOO22	IOO21
Initial Value	0	0	0	0

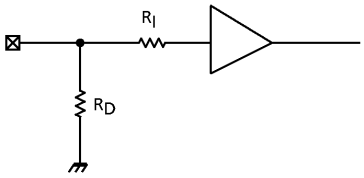
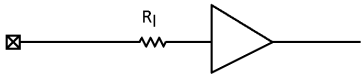
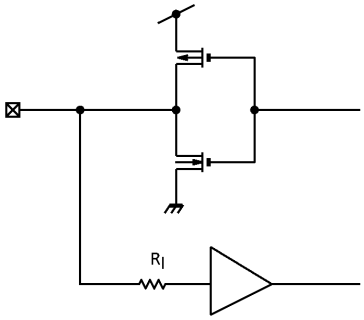
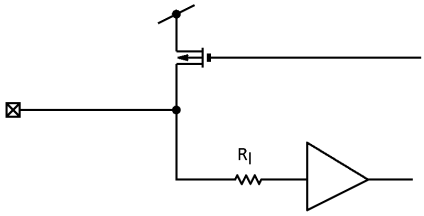
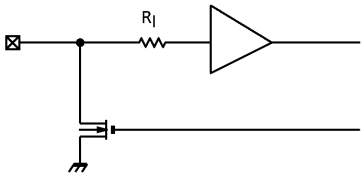
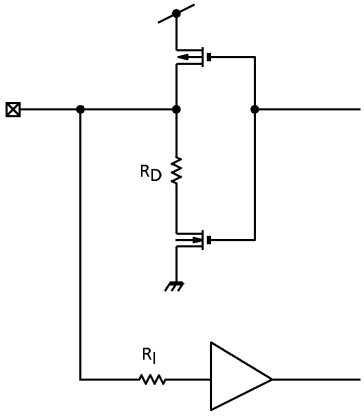
IOD11 to IOD14, IOD21 to IOD24: Input data
(The initial values are when the IOD11 to IOD14 pins and IOD21 to IOD24 are open or connected to low-level (V_{SS}).)
IOO11 to IOO14, IOO21 to IOO24: Output data

Input / output formats for the pins are set bit-wise.

	3	2	1	0
ERA	IO1S4	IO1S3	IO1S2	IO1S1
Initial Value	0	0	0	0
ERB	IO2S4	IO2S3	IO2S2	IO2S1
Initial Value	0	0	0	0

IO1S1 to IO1S4, IO2S1 to IO2S4
: 0-CMOS output with pull-down resistor
1-CMOS output without pull-down resistor

8-4 Pin Diagrams

INPUT WITH PULL-DOWN RESISTOR	INPUT WITHOUT PULL-DOWN RESISTOR
	
CMOS OUTPUT	**P-ch OPEN DRAIN OUTPUT**
	
N-ch OPEN DRAIN OUTPUT	**CMOS OUTPUT WITH PULL-DOWN RESISTOR**
	

R_I : 100 [Ω] (typ.)
R_D : 400 [kΩ] (typ.)

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS (V_{SS} = 0 V)

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	−0.3~6.0	V
Input Voltage	V_{IN}	−0.3~V_{DD} + 0.3	V
Power Dissipation (T_{opr} = 80°C)	P_D	—	mW
Soldering Temperature	T_{sol}	—	°C
Storage Temperature	T_{stg}	−55~125	°C
Operating Temperature	T_{opr}	0~40	°C

RECOMMENDED OPERATING CONDITIONS

(Unless otherwise specified, V_{SS} = 0 V, V_{DD} = 3 V, T_{opr} = 25°C, f_{XTH} = 2 MHz, f_{XTL} = 32.768 kHz, no load, no input)

PARAMETER		SYMBOL	TEST CIR-CUIT	MIN	TYP.	MAX	UNIT
Supply Voltage		V_{DD}	—	2.5	3.0	3.5	V
Oscillation Frequency		f_{XTL}	—	—	32.768	—	kHz
		f_{XTH}	—	—	2.0	—	MHz
Input Voltage	"H" Level	V_{IH}	—	V_{DD} × 0.8	—	V_{DD}	V
	"L" Level	V_{IL}	—	0	—	V_{DD} × 0.2	
Booster Capacitor		C_1	—	—	0.1	—	μF
		C_2	—	—	0.1	—	
Smoothing Capacitor		V_1	—	—	0.1	—	μF
		V_2	—	—	0.1	—	
		V_3	—	—	0.1	—	
		V_4	—	—	0.1	—	
		V_{XT}	—	—	0.1	—	

OSCILLATION CHARACTERISTICS
(Unless otherwise specified, V_{SS} = 0 V, V_{DD} = 3 V, T_{opr} = 25°C, f_{XTH} = 2 MHz, f_{XTL} = 32.768 kHz, no load, no input)

PARAMETER	SYMBOL	TEST CIR-CUIT	TEST CIRCUIT	MIN	TYP.	MAX	UNIT
Oscillation Start Voltage (low-speed)	V_{STA1}	—	T_{STA} = 10 s	2.2	—	—	V
Oscillation Hold Voltage (low-speed)	V_{HOLD1}	—	—	2.0	—	—	V
High-speed Oscillation Frequency	f_{OSCH}	—	R_f = 10 kΩ	—	2.0	—	MHz

DC CHARACTERISTICS

(unless otherwise specified, V_{SS} = 0 V, V_{DD} = 3 V, T_{opr} = 25°C, f_{XTH} = 2 MHz, f_{XTL} = 32.768 kHz, no load, no input)

CHARACTERISTICS	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Input Current (1-1) IN1~4	I_{IH1}	—	V_{DD} = 3.5 V, V_{IN} = 0 V	– 2.0		2.0	μA
	I_{IL1}	—	V_{DD} = 2.5 V, V_{IN} = 2.5 V	4.5	6.3	10.4	
Input Current (1-2) IO01~4	I_{IH1}	—	V_{DD} = 3.5 V, V_{IN} = 0 V	– 2.0		2.0	μA
Input Current (1-3) IO11~4	I_{IH1}	—	V_{DD} = 3.5 V, V_{IN} = 0 V	– 2.0		2.0	μA
Input Current (1-4) IO21~4	I_{IH1}	—	V_{DD} = 3.5 V, V_{IN} = 0 V	– 2.0		2.0	μA
Input Current (2) BRESET	I_{IH2H}	—	V_{DD} = 3.5 V, V_{IN} = 0 V During reset (high-resistance side)	– 11.6	– 7.0	– 5.0	μA
	I_{IH2L}	—	V_{DD} = 3.5 V, V_{IN} = 3.0 V After reset (low-resistance side)	– 16.0	– 10.0	– 7.0	
Input Current (3) TEST	I_{IL3}	—	V_{DD} = 3.5 V, V_{IN} = 3.5 V	250	350	583	μA
Input Current (4) SCK, SDAT	I_{IH1}	—	V_{DD} = 3.5 V, V_{IN} = 0 V	– 2.0		2.0	μA
	I_{IL1}	—	V_{DD} = 2.5 V, V_{IN} = 2.5 V	17.8	25.0	41.6	
Output Current (1-1) IO01~4	I_{OH1}	—	V_{DD} = 2.5 V, V_{OH} = 2.0 V			– 1.5	mA
	I_{OL1A}	—	V_{DD} = 2.5 V, V_{OL} = 0.5 V (N-ch Transitor only)	1.5			
	I_{OL1B}	—	V_{DD} = 2.5 V, V_{OL} = 0.5 V (Resistance + Nch Transitor)	4.5	6.25	10.4	μA
Output Current (1-2) IO11~4	I_{OH1}	—	V_{DD} = 2.5 V, V_{OH} = 2.0 V			– 1.5	mA
	I_{OL1A}	—	V_{DD} = 2.5 V, V_{OL} = 0.5 V (N-ch Transitor only)	1.5			
	I_{OL1B}	—	V_{DD} = 2.5 V, V_{OL} = 0.5 V (Resistance + N-ch Transitor)	4.5	6.25	10.4	μA
Output Current (1-3) IO21~4	I_{OH1}	—	V_{DD} = 2.5 V, V_{OH} = 2.0 V			– 1.5	mA
	I_{OL1A}	—	V_{DD} = 2.5 V, V_{OL} = 0.5 V (N-ch Transitor only)	1.5			
	I_{OL1B}	—	V_{DD} = 2.5 V, V_{OL} = 0.5 V (Resistance + N-ch Transitor)	4.5	6.25	10.4	μA
Output Current (2) BZ, BBZ	I_{OH2}	—	V_{DD} = 2.5 V, V_{OH} = 2.0 V			– 1.5	mA
	I_{OL2}	—	V_{DD} = 2.5 V, V_{OL} = 0.5 V	1.5			

CHARACTERISTICS	SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN	TYP.	MAX	UNIT
Output Current (3) COMMON	I_{OML3}	—	V_5 = 5.2 V, V_4 = 4.16 V, V_1 = 1.04 V	$V_{OM} = V_4 - 0.5$ V	—	—	−250	μA
	I_{OMH3}	—		$V_{OM} = V_1 + 0.5$ V	250	—	—	
	I_{OH3}	—		$V_{OH} = V_5 - 0.5$ V	—	—	−250	
	I_{OL3}	—		V_{OL} = 0.5 V	250	—	—	
Output Current (4) SEGMENT	I_{OML4}	—	V_5 = 5.2 V, V_3 = 3.12 V, V_2 = 2.08 V	$V_{OM} = V_3 - 0.5$ V	—	—	−150	μA
	I_{OMH4}	—		$V_{OM} = V_2 + 0.5$ V	150	—	—	
	I_{OH4}	—		$V_{OH} = V_5 - 0.5$ V	—	—	−150	
	I_{OL4}	—		V_{OL} = 0.5 V	150	—	—	
Output Current (5) SCK, SDAT	I_{OH5}	—	V_{DD} = 2.5V, V_{OH} = 2.0V		—	—	−1.0	mA
	I_{OL5}	—	V_{DD} = 2.5V, V_{OL} = 0.5V		1.0	—	—	
5 × Doubler Output Voltage	V_2	—			1.99	2.08	2.17	V
	V_1	—				$V_2 \times 0.5$		
	V_3	—				$V_2 \times 1.5$		
	V_4	—				$V_2 \times 2.0$		
	V_5	—				$V_2 \times 2.5$		
Supply Current	I_{DDOP}	—	CPM3, CKG1, 2 = 0 (Source clock)	Display ON		0.85	1.5	mA
	I_{DDSLOW}	—	CPM1	Display ON		18	30	μA
				Display OFF		8	15	
	I_{DDHOLD}	—	at HOLD	Display ON		14	20	
				Display OFF		4	7	
	I_{DDSTOP}	—	at STOP	Display OFF		0.8	1.4	