PM5342

SPECTRA-155

SPECTRA-155 DS3 DESYNCHRONIZER

REFERENCE DESIGN

PRELIMINARY

ISSUE 1: AUGUST 1999

REVISION HISTORY

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1	August 1999	Document Creation

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1 DEFINITIONS

DAC	Digital to Analog Converter.
Desynchronizer	A circuit that accommodates the interface of a signal carried over a synchronous or a pleisosynchronous network to a user line. The desynchronizer circuit averages the frequency of a gapped network clock; gaps in the network clock being the product of a bit stuffing operation, a synchronization of an original signal to the network clock.
DS3	Digital Service, Level 3. A framed digital signal coded as a bipolar signal at 44.736 Mbps. A DS3 signal carries the equivalent of seven DS2 signals, or 28 DS1 signals.
FIFO	First In First Out. A queue. A data structure or hardware buffer from which items are taken out in the same order they were put in.
LIU	Line Interface Unit. A circuit that can interface a standard unipolar logic (TTL, CMOS, PECL) to the line and vice versa.
LO	Local Oscillator. A circuit that supplies a signal that enables the translation of a lower frequency modulation signal to an Intermediate Frequency (IF) and vice versa.
LUT	Look Up Table. A circuit usually implemented as a Read Only Memory (ROM).
NCO	Numerically Controlled Oscillator. The oscillator frequency is programmable, and set by an input numerical value.
PLL	Phase Locked Loop. A feedback system that locks the phase of a variable frequency signal source to an incoming reference phase.
RAM	Random Access Memory.
ROM	Read Only Memory.
SONET	Synchronous Optical NETwork. A network synchronized to a Primary Reference Source of a high frequency stability.

SSB Modulator	Single Side Band Modulator. A circuit that upconverts a low frequency signal to a higher frequency using a high frequency LO signal. The new signal frequency is a sum or a difference of the LO signal and the modulation signal frequencies. The process of SSB modulation requires suppression of the LO signal and the other sideband signal.

2 FEATURES

- Embodies PMC-Sierra's recommendations for DS3 desynchronization.
- Reduces SONET mapping jitter below the requirements of GR-253-CORE and ITU-T G.783.
- Meets GR-253-CORE and ITU-T G.783 requirements for pointer adjustment test sequences.
- Meets American National Standards Institute, T1.506 specification regarding delay through the network.
- Desynchronizes up to twelve DS3 channels using a minimum number of components and board space.
- 3.3 Volt CMOS DS3 interface to the SPECTRA-155 Telecom bus in DS3 serial mode.
- Three DS3 LIUs.

3 APPLICATIONS

- Desynchronization of up to 12 DS3 channels.

4 REFERENCES

1. ITU-T Recommendation G.709 - "Synchronous Multiplexing Structure," Helsinki, March 1993.

2. Bellcore GR-253-CORE , Issue 2, December 1995

3. American National Standards Institute, T1.105.03, 1994

4. American National Standards Institute, T1.506, 1994

5. RF Micro Devices, AN0001. “Optimization of Quadrature Modulator Performance”

6. RF Micro Devices, TA0019, “Quadrature Modulator/Demodulator IC Covers Baseband to 250 MHz”

7. Xilinx: Virtex XCV150PQ240 data sheet .

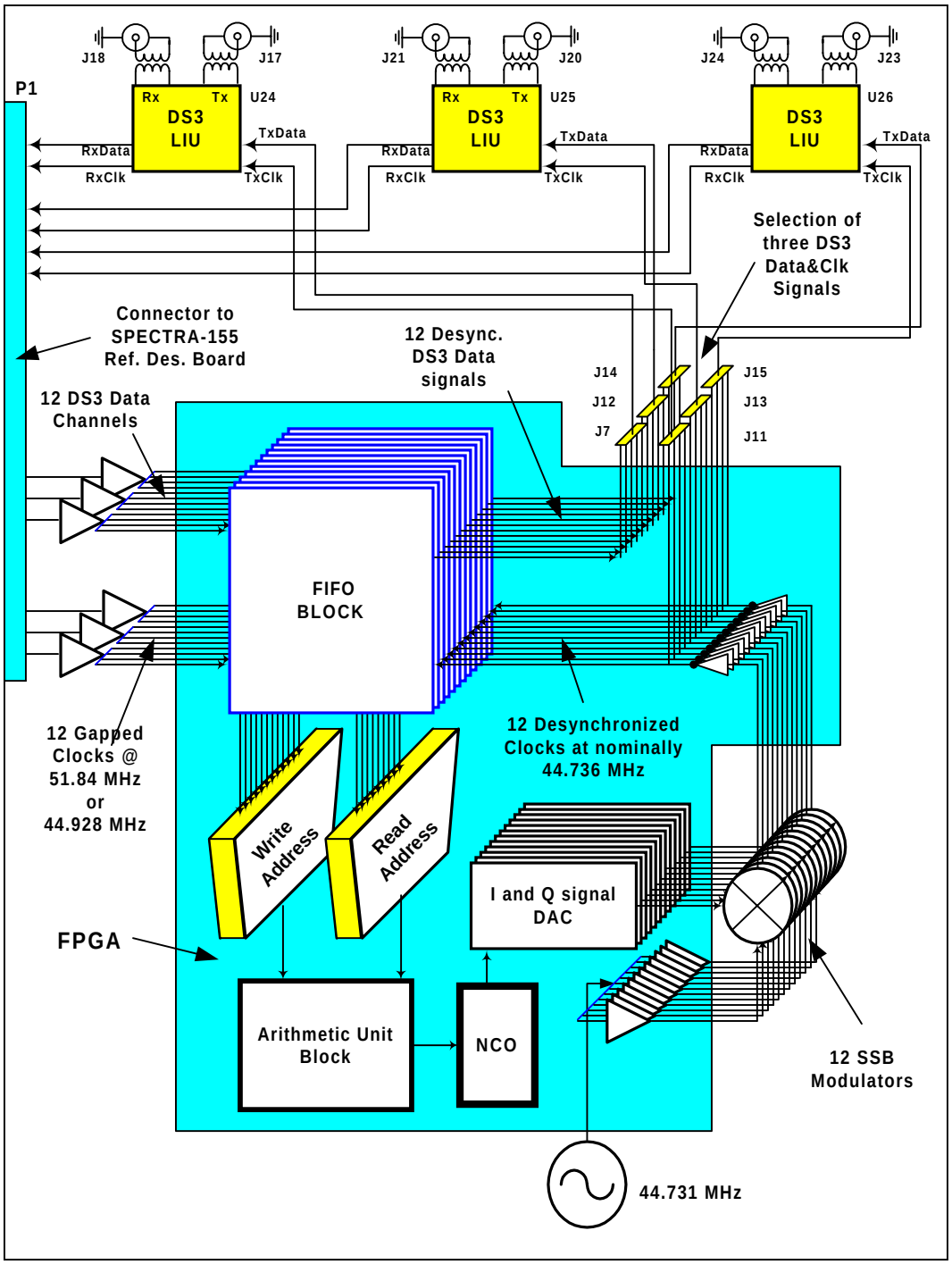
8. RF Micro Devices : RF2703 data sheet.

9. PMC-Sierra, Inc. “SPECTRA-155 DS3 Desynchronization” Applications Note PMC-990390.

10. PMC-Sierra, Inc. “SONET/SDH Node Optical Interface for WAN Networks Reference Design (SNOW BOARD) ”, PMC-970285

5 BLOCK DIAGRAM

Figure 1 - Desynchronizer Block Diagram

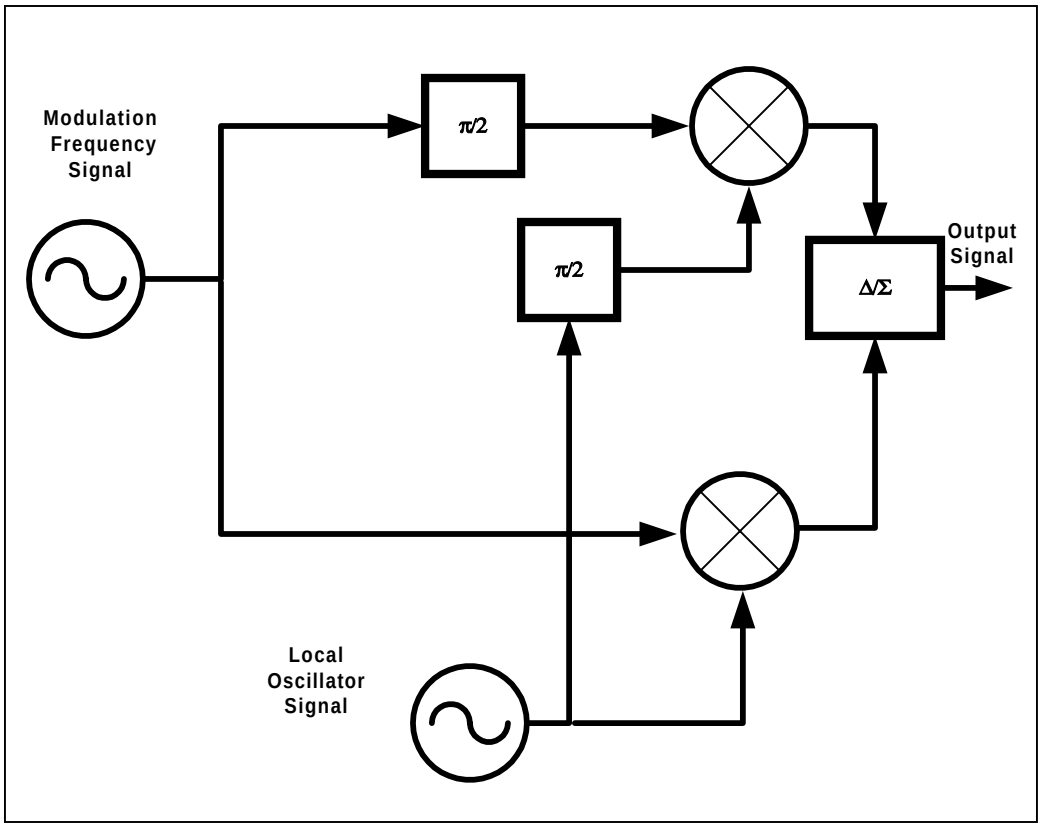


6 FUNCTIONAL DESCRIPTION

The DS3 Desychronizer Reference Design shown in Figure 1 consists of several modules. The DS3 data is read from the SPECTRA-155 and stored in a 4096 bit FIFO circuit. The FIFO write clock is a 51.84 MHz or 44.928 MHz gapped clock from the SPECTRA-155 reference design board. The DS3 data is read from the FIFO using a variable 44.736 MHz +/- 5 kHz clock generated by the SSB modulator. The frequency of the SSB modulator is controlled by an NCO and a DAC. The write and read FIFO address difference, representing the FIFO fill level, is used as an error signal for a second order PLL that is partially implemented in the AU block. The result of the processing in the AU block is fed to the NCO block that generates an offset frequency. The offset frequency is passed to two DACs, which generate a complex offset frequency signal (I and Q channels). This complex offset frequency is used by the SSB modulator to generate a desired average DS3 frequency.

6.1 Single Sideband Modulator

Figure 2 - SSB Modulator Block Diagram



The SSB modulator, as shown in Figure 2, uses two double balanced mixers. A local oscillator signal is split and one copy is shifted 90 degrees. Similarly, a modulation signal is split to two signals and one copy of the modulation signal is shifted 90 degrees. The two output signals from the mixers can form a sum to pick the upper sideband, thus changing the 44.731 MHz clock to the desired frequency.

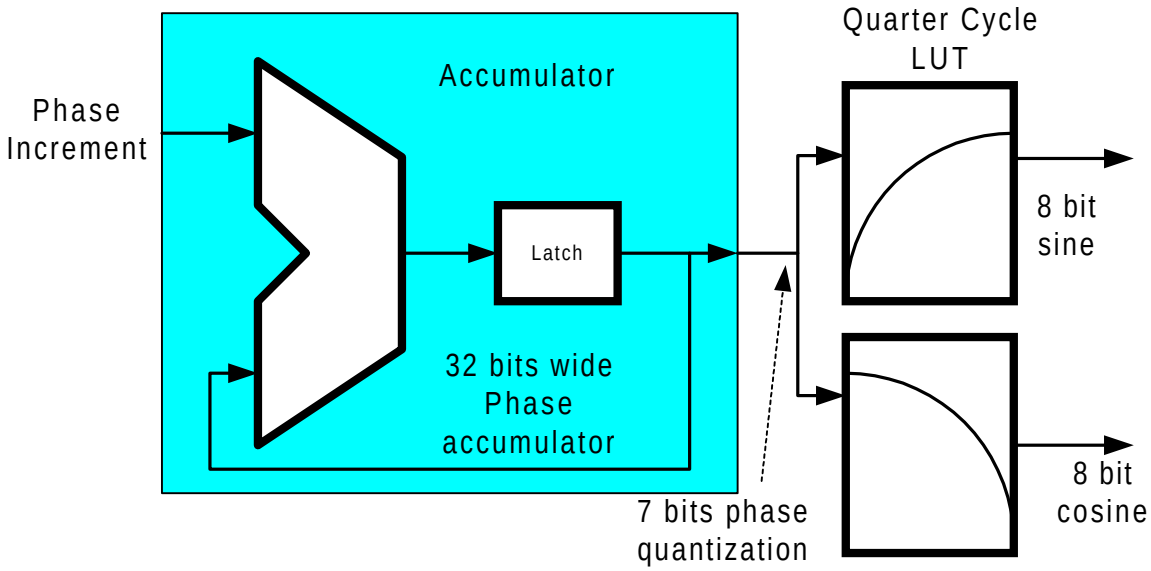
It is advantageous to digitally generate the FIFO read clock because the frequency will not depend on temperature variations or changes in the FIFO fill level. This approach is also economical, since the circuitry needs only one crystal oscillator at 44.731 MHz for multiple DS3 FIFO read clocks.

We shall not explain the operation of this circuit. A good treatment of this subject is in RF Micro-Devices application notes AN0001 and TA0019.

6.2 FPGA Circuitry

6.2.1 Numerically Controlled Oscillator

Figure 3 - NCO Block Diagram



The SSB modulator requires an LO signal and a modulation signal. The modulation signal is a complex sinusoid with I and Q components (sine and cosine). The NCO block helps generate these I and Q signals.

The NCO can be implemented as a 32 bit wide accumulator with the 7 most significant bits used as a phase representation of the modulation signal. This 7 bit phase coding accounts for 128 possible phases that are in fact the 128 possible addresses of a look up table. The phase of the modulation signal is converted to amplitude using an 8 bit Look Up Table (LUT). One LUT is shared among all twelve channels. Accumulators can share the same adder hardware with a 16x32 RAM containing the current value of phase for all twelve DS3 channels. One quarter of the sinusoid is encoded in the sine LUT. Simple manipulation of the addresses of the LUT is used to create the sine and cosine signals.

6.2.2 Digital to Analog Converter

The DACs generate the I and Q modulation signals for the SSB modulator. An 8 bit DAC with a minimum 160 kHz sampling rate is recommended. In order to

achieve a small part count and a compact design, all twenty four DACs were implemented in an unorthodox fashion trading speed for amplitude precision.

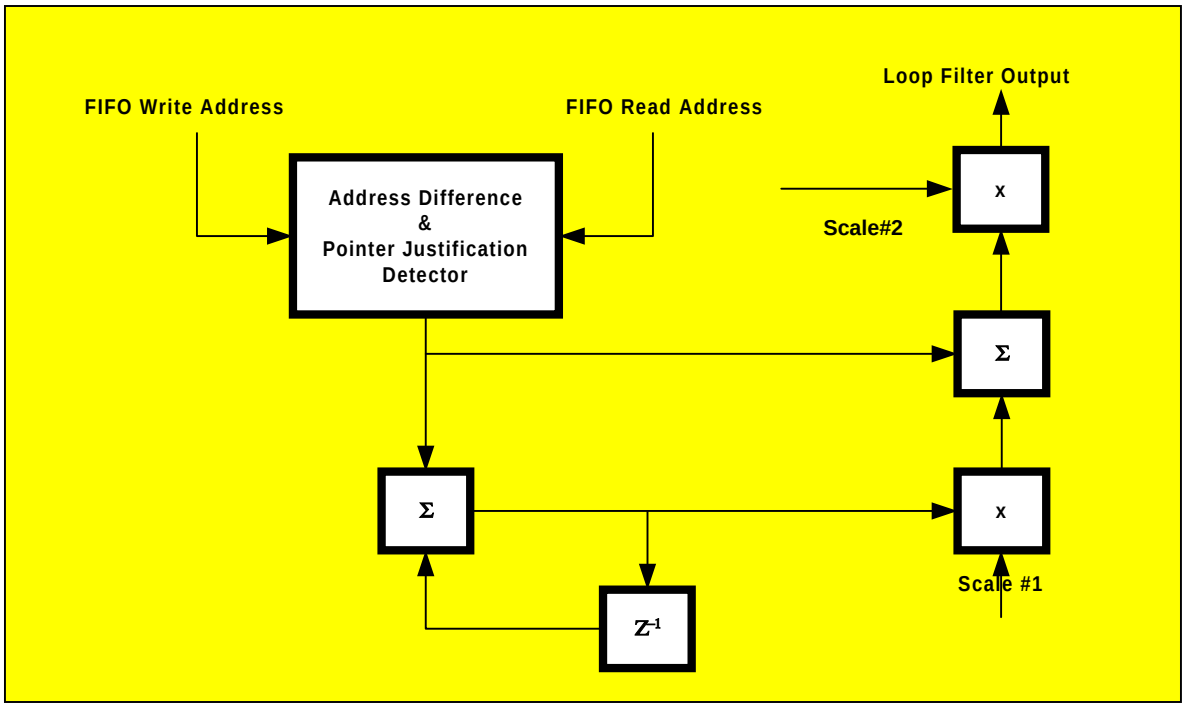
The DAC circuitry uses a system clock (51.84 MHz or 44.928 MHz clock) and generates a TTL signal at this rate. It will generate a number of TTL high level pulses equal to the input word within 256 clock cycles. These pulses are distributed in time as uniformly as possible. A first order RC low-pass filter, external to the FPGA, averages a sequence of TTL high and low pulses and produces the correct analog value. Every 256 clock cycles (at the rate of 202.5 kHz or 175.5 kHz) the input value changes.

6.2.3 FIFO and Write and Read Counters

A one channel FIFO is implemented using a 4096 bit dual port RAM, implying a worst-case delay of 91.559µsec, well within the specification of ANSI T1.506 minimum of 4.0msec. The system clock (51.84 MHz or 44.928 MHz) is used to write to the 4096 bit FIFO and also to read from it. A second 8 bit FIFO is used to synchronize to different speeds of the system clock and the 44.736 MHz clock from the SSB modulator.

6.2.4 Arithmetic Unit Block

Figure 4 - AU Loop Filter Block Diagram



The Phase Detector and the Loop Filter portion of the PLL circuit is implemented in the Arithmetic Unit Block. The functions required from the Phase Detector and Loop Filter are shown above in Figure 4. The fill level of the FIFO is equal to difference between the read and write FIFO addresses. The fill level determines if the FIFO read clock should be faster or slower. If the FIFO fill level is low, the read frequency should be reduced. If the FIFO fill level is high, the read frequency should be increased. A loop filter prevents the FIFO read clock from changing frequency too quickly and creating jitter. A loop filter with a perfect integrator should be used because it will eventually reduce the phase error to zero, even in the case of sustained pointer adjustments. Simulations have indicated that the PLL should have a natural frequency of 0.1 Hz and a damping factor of 5. Details can be found in APPENDIX A - PLL CALCULATION.

7 IMPLEMENTATION DESCRIPTION

The DS3 Desynchronizer reference design is a cost effective, small, low power solution to desynchronize 12 channels of DS3 signals in one circuit. The main design goals were low power consumption, and a compact layout.

The board area is square in shape and less than 4"x4". This includes all necessary portions of the design: FPGA, PROM for FPGA, twelve RF2703 quadrature upconverter circuits and the crystal oscillator.

7.1 DS3 Desynchronizer Schematics

The schematic contains ten pages. The first page is the top level and shows the design hierarchy.

7.1.1 Block Diagram, Page 1

The first page of the schematics shows the connection between major blocks in the design. There are five blocks : FPGA block, Modulator block, DS3_LIU block, Power block and Connector block.

Signal flow is easy to follow from the schematics. The DS3 signals can be inserted to the board via the LIU. The LIU recovers the clock from the DS3 signal and then samples the DS3 signal using this recovered clock. Three DS3 data and three DS3 clocks from the LIUs are delivered to the SPECTRA-155 board through the connector block as DS3TDAT[3:1] and DS3TCLK[3:1].

DS3 data passes through the FPGA based desynchronizer from the SPECTRA-155 board to the LIU. The purpose of the DS3 Desynchronizer reference design is to show how 12 DS3 channels can be desynchronized, but the SPECTRA-155 board supplies only three DS3 channels, so each DS3 data and DS3 clock from the SPECTRA-155 board is copied four times, using four buffer circuits, to create 12 channels of DS3 signals. This generates the DS3RDAT[12:1] and DS3RCLK[12:1] signals that pass from the connector block to the FPGA block. We can test all twelve channels of the desynchronizer board using only one SPECTRA-155 board.

The system clock (51.84 MHz RXC signal or 44.928 MHz drop side clock) is also passed from the SPECTRA-155 reference design board. The RXC signal is not present on the SPECTRA-155 connector so the SPECTRA-155 reference design board needs to be reworked. RXC is necessary for the FPGA

implementation, it is the main clock for the Desynchronizer FPGA. Specifics of the SPECTRA-155 rework are detailed in Appendix B.

The three LIUs receive DS3 data and clocks from the FPGA. Any three data and clock signals can be selected using a set of jumpers. The twelve sets of data and clocks are designated on the top level schematics as DS3DATO[12:1] and DS3TCLK[12:1].

The Modulator block serves to create twelve desynchronized clocks. The twelve sets of sine and cosine signals are sent to the modulator block as DACOUTI[12:1] and DACOUTQ[12:1]. Again, these are the twelve pairs of single ended sine and cosine signals that are in quadrature and will produce twelve 44.736 MHz clocks through the upconversion process in the RF2703 modulator/demodulators.

The power block supplies power to the board. The FPGA is a 2.5 V device that is 3.3 V I/O tolerant. The core of the device requires a 2.5 V power supply whereas the I/O blocks of the FPGA require 3.3 V. The DS3 Desynchronizer board is powered through the SPECTRA-155 reference design board connector. There are two voltage regulators on the DS3 Desynchronizer board to generate 2.5 V and 3.3 V. Also, there is the possibility to power a DS3 Desynchronizer board standalone through the power terminals with a 5 V power supply.

7.1.2 FPGA Block, Page 2

This page shows the FPGA connections to the rest of the circuitry on the board. The FPGA symbol is split into three parts for easier handling. Please refer to the Virtex data sheet for details about the Virtex family I/O blocks. In our case, we use the LVTTL mode for all eight I/O blocks. Part one of the symbol contains pins of I/O blocks 4, 5, 6 and 7, while part two of the symbol contains the pins for the I/O blocks 0, 1, 2 and 3. Part 3 of the symbol contains special purpose pins.

The Virtex M0, M1 and M2 pins set the configuration mode for the FPGA. SW1 can be set to program the FPGA either in master serial mode or slave serial mode. The third part of the Virtex symbol connects to the configuration PROM. It is possible to configure the FPGA from the configuration PROM XC1701L or through the XCHECKER port, J1. When configuring the FPGA using the XCHECKER, the configuration PROM should be uninstalled, and M0, M1, M2 set to slave serial mode ([111]). When using the configuration PROM, the FPGA should be in Master Serial mode, with M0, M1 and M2 low ([000]).

The Virtex I/O blocks 6 and 7 are used to receive 12 DS3 data and clock signals from the SPECTRA-155. These signals are buffered and source resistance matching is used to reduce multiple reflections on the transmission lines. The

desynchronized clocks and data are send to three LIUs through I/O blocks 4 and 5. The source resistors are used in this case because the clock and data signals are switched through the set of six headers to go to the three LIUs. I/O blocks 0, 1, 2 and 3 are used for I and Q signals named DACOUTI and DACOUTQ respectively. The quadrature signals are fed into the RF2703 upconverter. The local oscillator (LO) inputs of the RF2703s are connected to the FPGA MCLKOUT signal. MCLKOUT is an 89 MHz signal and board capacitance with a 1.5 kΩ series resistor will convert the square-wave clock into a sinusoidal signal. The XTFILTRA and XTFILTRB signals are attached to the I/O blocks 0, 1, 2 and 3. The purpose of these signals is explained later in section 7.1.5.

7.1.3 Test Points, Page 3

This page designates some test points connected to the FPGA. These points can be used to connect probe signals from the FPGA to monitor the performance of the FPGA. The switch array SW2 can be used to set control signals on the FPGA and it is present only for testing purposes. Ground and power supply test points are provided to aid in testing.

7.1.4 FPGA Power Supply, Page 4

Most hardware on the DS3 Desynchronizer reference design operates at 3.3V with the exception of the core supply on the Virtex FPGA which requires 2.5V. An external 5V supply from the SPECTRA-155 board or a power supply is fed into a 3.3V regulator (U22) and a 2.5V regulator (U23) to provide power to the DS3 board.

Y1 is a 44.731 MHz crystal oscillator. This signal can be selected as the Virtex clock using J6. Inside the chip the DLL (Delay Locked Loop) block multiplies the clock to twice this frequency, as required by the RF2703s.

An external signal generator can also be used to generate the 44.731 MHz clock. For this type of operation a sinusoidal signal can be supplied via the SMA J4 connector to the MC100EPT23D chip which will convert this signal to TTL. It is possible to use TTL, ECL or PECL signal generators. With this configuration it is recommended to substitute R12 with a 0.1 µF capacitor. R10, R11 and R12 constitute the T-pad and their values can be chosen appropriately if there are problems matching loads with the signal generator.

7.1.5 Modulator Block, Pages 5, 6 and 7

Pages 5, 6 and 7 show the 12 RF2703 quadrature Single Sideband Modulator circuits.

The LO pin is fed with the 89.462MHz signal. The amplitude of the signal required is between 40 mV and 200 mV peak to peak. Large amplitude LO signals will reduce the LO suppression and lower sideband suppression. The 89 MHz signal and board capacitance with a 1.5 kΩ series resistor will convert the square-wave clock into a sinusoidal signal. As long as the signal is between 40mVpp and 200mVpp both LO and lower sideband suppression will be approximately 30dBc.

The two quadrature signals, I and Q, are taken as digital signals from the Virtex FPGA. The sequence of TTL ones and zeros at system clock rate is averaged in a low-pass filter. For good LO and lower sideband suppression, AC coupling of I and Q inputs on the RF2703 is required. The device has an internal resistance of 1260 Ω. This internal resistance along with an AC coupling capacitor forms a high-pass filter in series with the low-pass filter. Cutoff frequencies of the low-pass and high-pass filters are chosen to give approximately 200 mV amplitude signal at the I and Q pins of the chip in the frequency range from 1000 Hz to 9000 Hz. Output amplitude from the up-conversion process in the RF2703 is in the range from 50 mV to 100 mV. This signal needs to be amplified to TTL levels, and can be accomplished using an inverter that is self-biased using feedback. The inverter can be built in the FPGA but it is not clear whether the Virtex inverter implementation will result in reliable operation. There was no possibility to try this in reasonable time before the schematics for the DS3 desynchronizer were finalized. As a backup, there are two additional 74HC540s in the arrangement depicted on the schematics. The external filter can be used by soldering a jumper resistor to connect the XTFLTRA, XTFLTRB signals of each modulator circuit to the FPGA. This 74HC540 TTL octal buffer chip can produce a perfect TTL signal synchronized to the upconverted output upper side-band signal of the RF2703 chip. If the Virtex implementation is operating properly then the two 74HC540s, U2 and U7, need not be populated.

7.1.6 Line Interface Block, Page 8

This page shows standard connections to the TDK 78P2241 LIU. There are three LIUs on the board. The jitter meter can be interfaced through BNC connectors. For more information about operation of this chip consult the 78P2241 data sheets.

7.1.7 LIU Interface MUX,Page 9

This page contains six 10 pin headers used to decode the desynchronized signals that are sent to the LIUs. The FPGA desynchronizes twelve DS3 channels but because there are only three LIUs on the board we need to select three out of these twelve DS3 channels to feed to the LIUs.

Two jumpers per header are required to select a particular DS3 channel.

To select a specific data or clock signal, connect two jumpers per header. J11, J13 and J15 are headers that connect DS3 CLK signals and J7, J12 and J14 connect DS3 data from the Virtex FPGA to the LIU. Table 1 below outlines the correct jumper settings for decoding the DS3 signals.

Table 1 Jumper Setting for Selecting DS3 Clocks to LIU

Selected Signal Name	Connect to LIU	Jumper	Pins	Pins
DS3CLK(1)	U24	J11 (TCLKA)	2-3	5-6
DS3CLK(4)			3-4	5-6
DS3CLK(7)			6-7	8-9
DS3CLK(10)			6-7	9-10
DS3CLK(2)	U25	J13 (TCLKB)	2-3	5-6
DS3CLK(5)			3-4	5-6
DS3CLK(8)			6-7	8-9
DS3CLK(11)			6-7	9-10
DS3CLK(3)	U26	J15 (TCLKC)	2-3	5-6
DS3CLK(6)			3-4	5-6
DS3CLK(9)			6-7	8-9
DS3CLK(12)			6-7	9-10
DS3DATO(1)	U24	J7 (DATOA)	2-3	5-6
DS3DATO(2)			3-4	5-6
DS3DATO(3)			6-7	8-9
DS3DATO(4)			6-7	9-10
DS3DATO(5)	U25	J12 (DATOB)	2-3	5-6
DS3DATO(6)			3-4	5-6
DS3DATO(7)			6-7	8-9
DS3DATO(8)			6-7	9-10
DS3DATO(9)	U26	J14 (DATOC)	2-3	5-6
DS3DATO(10)			3-4	5-6

DS3DATO(11)			6-7	8-9
DS3DATO(12)			6-7	9-10

7.1.8 Connector Block, Page 10

Page 10 of the schematics shows connector P1 that connects the DS3 Desynchronizer Reference Design Board to the SPECTRA-155 Reference Design Board. DS3 data and clock from the SPECTRA-155 board are buffered in TTL buffers U15, U19, U20 and U21. This arrangement allows testing of all twelve DS3 desynchronizers using one SPECTRA-155 board, although a single SPECTRA-155 board supplies only three DS3 channels. Each of the three DS3 channels from the SPECTRA-155 is copied four times and fed to the Virtex FPGA.

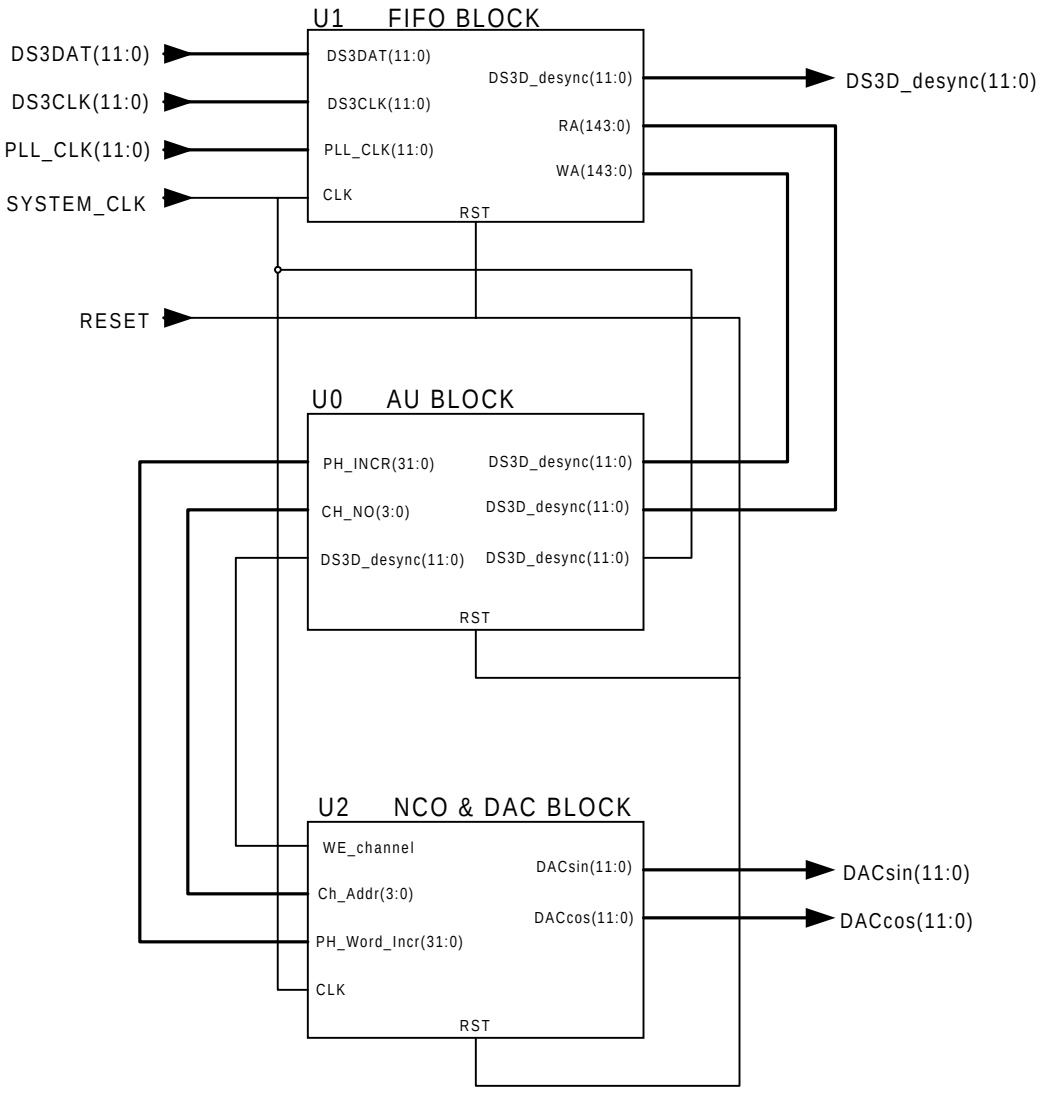
Header J8 can be used to connect a 51.84 MHz clock from the Spectra board if a jumper is set between pins 2 and 4, or a differential signal can be accepted via balun T8 if J8 pins 6 and 8 are connected with a jumper.

An on board 51.84MHz VCXO can be used for self-testing of the board. A jumper between pins 3 and 4 should be set on header J8 to operate in VCXO mode.

7.2 DS3 Desynchronizer FPGA

A block diagram of the main blocks in the FPGA is shown below in Figure 5.

Figure 5 - Block Diagram of the DS3 Desynchronizer FPGA



The main blocks are the FIFO block, AU block and NCO & DAC block. The FIFO block utilizes the block RAM feature of the Virtex family. In the XCV150 there are 12 designated 4 kbit blocks of RAM organized as a FIFO. Each DS3 channel is assigned to one FIFO. Write and read addresses for each FIFO are 12 bits long

as there are 4096 bits in the dual port synchronous FIFO. The write and read addresses of the twelve DS3 channel FIFOs are organized as two long arrays each 144 bits long. These two arrays are inputs for the AU block. The AU block performs operations on the read and write FIFO addresses to obtain the difference between those addresses. The pointer difference generates an error signal used to lock the PLL. The AU block filters the FIFO address difference and calculates a phase word. One phase word is associated with each DS3 channel. The phase word for a specific DS3 channel indicates the frequency that can be used to clock DS3 data out of the FIFO. There is a separate clock associated with each DS3 channel. These 12 clocks are designated in the block diagram as DS3DesyncClk(11:0).

The Phase Words are loaded into the NCO & DAC block. The NCO block accumulates the phase word values and generates a sinusoidal waveform using a lookup table that has stored amplitudes of a sine waveform. DAC circuitry converts the current amplitude from digital to analog. The NCO & DAC circuitry creates a complex modulation frequency (sine and cosine waveform) that is then upconverted to 44.736 MHz in the RF 2703 quadrature modulator/demodulator circuit.

Special care was taken to achieve a synchronous design, so all twelve block RAM cicruits are clocked with one system clock supplied through the global buffer. Otherwise, we would need 24 clocks supplied by global clocks if we want to clock all DS3 signals with DS3 clocks in and out of the FIFO. Since the Virtex family has only 4 global clocks, this is not possible. The DS3 clocks from the SPECTRA-155 are used as clock enable signals for writing to the FIFO. For clocking the DS3 signals out of FIFO, the system clock is used to clock data from the 4096 bit FIFO to another small FIFO implemented in one CLB. This small 8 bit FIFO and some additional logic switch from the global system clock to the DS3 frequency.

All other blocks are designed using the global system clock. This simplifies the design and routing.

7.2.1 FIFO Block

The FIFO block consists of three parts. The main part of the FIFO block is a 4096 bits deep by 1 bit wide RAM block. The second part is the FIFO write address generation consisting of a 12 bit counter running at system clock rate. The count is increased every time the DS3 clock from the SPECTRA is high, and at the same time data is written into the FIFO. The third part of the FIFO block consists of a FIFO read address generation circuit and a small 8 bit synchronization FIFO.

The synchronization FIFO is a dual port synchronous FIFO that is being written at system clock rate, and read out using the DS3 desynchronized clock at 44.736 MHz. The write rate is larger than the read rate so the 8 bit synchronization FIFO will overflow unless there is a feedback mechanism to control writing into the synchronization FIFO. The read and write addresses of the synchronization FIFO are compared and if the FIFO fill level is higher than 4 bits, writes to the FIFO will be stopped until the fill level drops. This is done to minimize the amount of circuitry that is not using the system global clock.

7.2.2 Arithmetic Unit (AU) operation

Most of the FPGA runs synchronously from one single system clock. Circuits that operate at a slower speed than system clock also use the system clock; the slower rate of operation is achieved using clock enable inputs (CE) for relevant flip-flops (FF).

One row in a SONET/SDH frame has a 72 kHz rate, a product of the 8kHz frame rate and the 9 rows per frame. The DS3 signal FIFO write and read addresses are sampled and processed at 72 kHz. Sampling of the FIFO addresses can be done at a slower rate but in order to minimize aliasing we use the highest possible rate at which the reading of the FIFO write and read address difference is constant if the PLL is lock. All processing for the specific DS3 channel is accomplished at the 72 kHz rate. The operations that are required to process one DS3 channel are relatively simple and can be sequenced one after the other using the same basic circuitry. Operations are:

- Subtract the read FIFO address from the write FIFO address and store it for further use in RAM.
- Add the FIFO address difference to the accumulated FIFO address difference that is also stored in RAM, and after the addition store the new value in the RAM for further use.
- Scale the new accumulated (integrated) value of the FIFO difference by taking only the portion of the accumulated value and adding it to the current FIFO difference.
- Scale the product of the previous operation. This can be done by using a portion of bits that form the value after the value.
- Add obtained value to a phase value that results in 5000 Hz sine waveform to get new phase increment.

All operations listed above require:

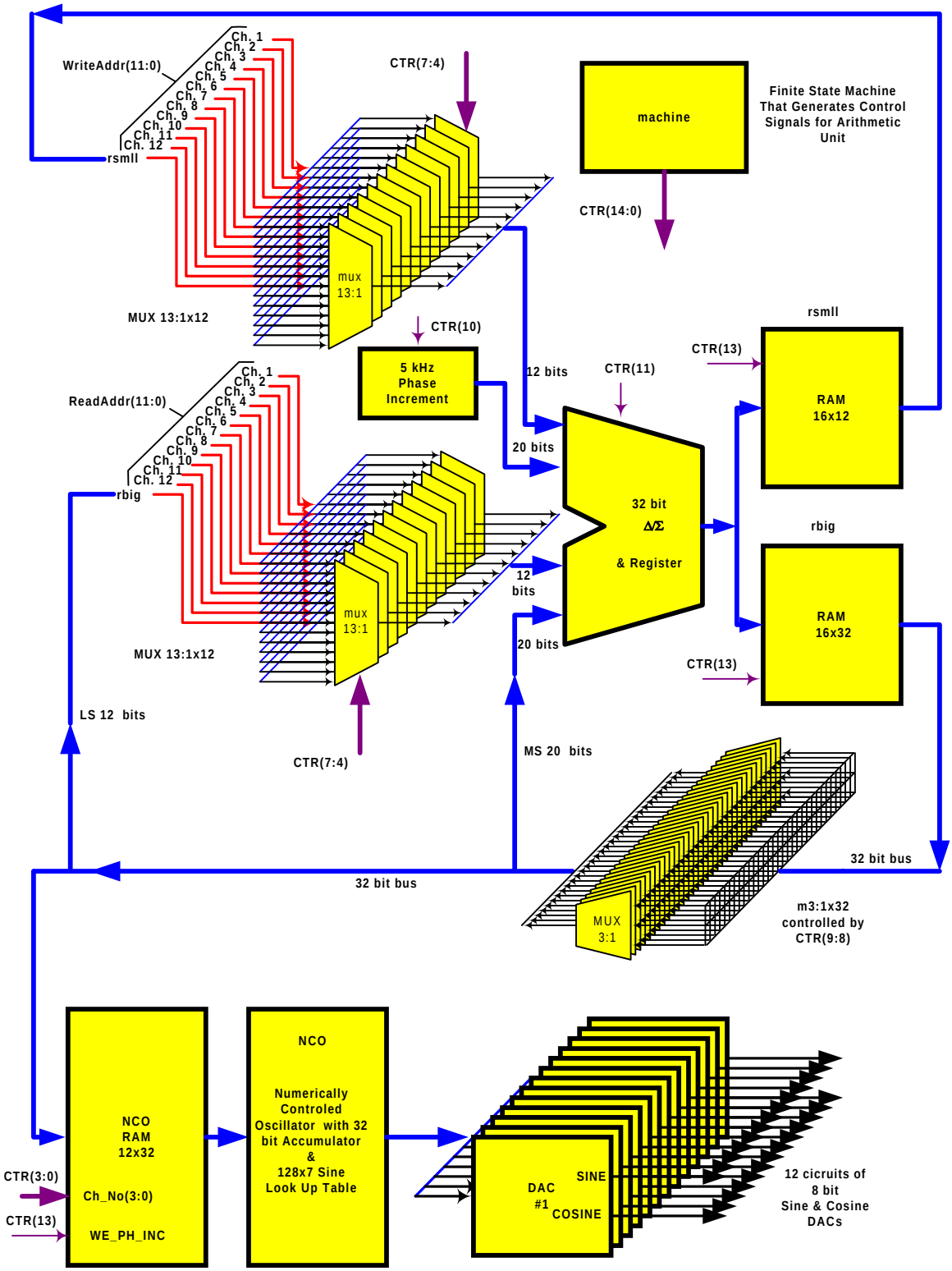
- an add or subtract circuit,
- memory to store the current FIFO read and write address difference,
- memory to store the accumulated FIFO read and write address difference,
- a multiplexer circuit to perform two scaling operations (dividing and multiplying by 2^n).

Above operations for one channel can be performed in 13 steps. The DS3 Desynchronizer FPGA AU can operate at 13*72 kHz or 936 kHz to finish these 13 steps. The 936 kHz rate is very slow in comparison to the rates achievable in modern FPGAs. In fact, signal processing for all twelve DS3 channels can be done using the same ALU. This will bring operational frequency to 12.96 MHz or 11.232 MHz. The 12.96 MHz frequency can be obtained dividing the global 51.84 MHz clock by four, or in the case that system clock is 44.928 MHz, the 11.232 MHz clock is obtained by dividing 44.928 MHz by four.

The ALU consists of two input multiplexer circuits, an add-subtract circuit, a register, two single port synchronous RAM circuits and a scaling multiplexer circuit. The Multiplexer circuit brings 13 signals into one and is 12 bits wide. It is designated in Figure 6 as MUX 13:1x12. The add-subtract circuit is 32 bits wide and operation is controlled by the add-subtract input, as shown in Figure 6. The register is used to latch the output of the add-subtract operation. One single port 16x12 synchronous RAM (designated “rsmll” in Figure 6) is used to store the write and read FIFO address difference for each DS3 channel. A single port 16x32 synchronous RAM (designated “rbig” in Figure 6) is used to store the integrator branch value of the lead-lag loop filter. The multiplexer circuit, M3:1x32, in Figure 6, is used for scaling the output of the integrator branch to set the damping factor of the phase lock loop. In other instances it is used to scale the loop gain to give the desired loop bandwidth.

The first 12 bits that are fed to the add-subtract circuit always pass through the MUX 13:1x12 multiplexer circuits. This multiplexer circuit will select one of 12 DS3 channel FIFO addresses or the input from “rsmll” or “rbig”. The other 20 bits are supplied directly to the add-subtract circuit. The “inc_5khz” circuit output is all zeros if CTR(10) is zero, if CTR(10) is one the output will generate a 5 kHz signal at the output of DAC circuit. Circuit “M3_1x32” in Figure 6 selects either the accumulated value of the FIFO address difference stored in “rbig” when CTR(9:8) is “00”, or the same value divided by 2^{22} if CTR(9:8) is “01”. In the case that CTR(9:8) is “10” the output of the final filtering action is multiplied by 2^8 and this signal is latched into the NCO for further processing.

Figure 6 - Top Level AU Block Diagram



The heart of the AU operation is a controller circuit designated as “machine” in Figure 6.

The steps required to process one DS3 channel are shown in Figure 7. The process requires thirteen states with two no-operation states that can be utilized for future expansion. The state machine will finish an entire cycle for one channel before incrementing to the next channel.

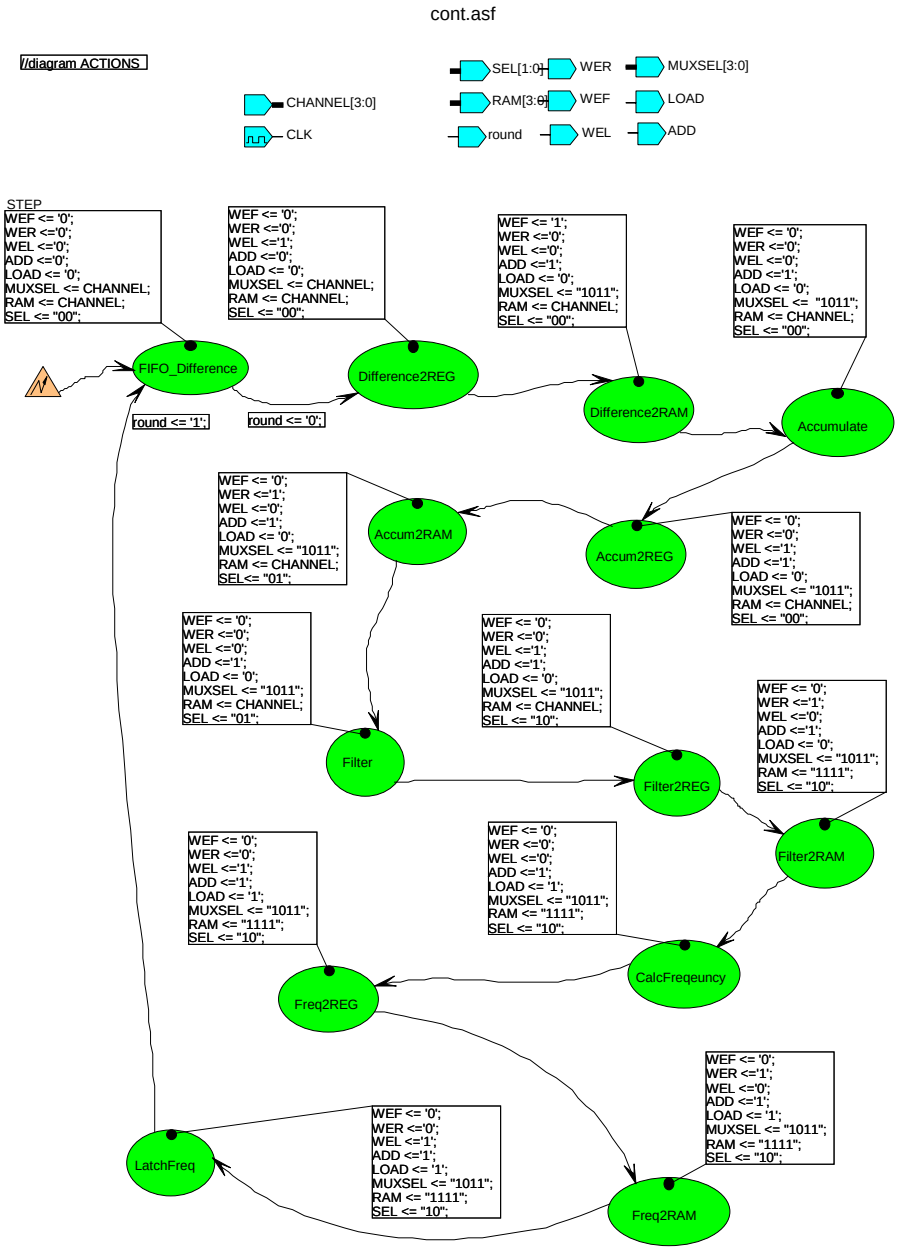
Inputs to the state machine are:

- CLK – the clock.
- and CHANNEL(3:0) – channel number.

Outputs of the state machine are:

- MUXSEL(3:0) – selects input to the ALU,
- RAM - RAM address where results of AU is stored,
- WEL – write enable to latch following ALU,
- WER- write enable for the 16x12 RAM where current FIFO address difference is stored,
- WEF- write enable for the 16x32 RAM where accumulated FIFO address difference is stored,
- ADD – if 1, AU adds input numbers, otherwise subtracts,
- SEL(1:0) – selects scaling multiplexer output M3:1x32,
- LOAD – write enable to store the result of AU operation to NCO,
- Round – to account for extra cycles up to 15.

Figure 7 - AU Block State Diagram



The operation of the controller for the AU (arithmetic Logic Unit) can be explained with the state diagram. The state machine passes through each of the 13 states for each DS3 channel. Upon reset the machine will start from the FIFO_DIFFERNCE state.

The function of each state is outlined below:

FIFO_DIFFERENCE

Two multiplexer circuits are set to select the current channel 12 bit read and write FIFO addresses. These two addresses are subtracted in the 32 bit add-subtract circuit. The add-subtract input bits 32 down to 13 are filled with zeros for this operation. At the same time, the RAM address points to the integrator branch value for the current channel.

DIFFERENCE2REG

The clock enable of the 32 bit register is set to latch the FIFO write and read address difference.

DIFFERENCE2RAM

Latches the FIFO address difference from the register to the “rsmll” RAM. It also selects the accumulated value of the FIFO difference from “rbig” through the multiplexer “M3:1x32” into the AU input B (Figure 6).

ACCUMULATE

Sets the input select multiplexer circuits to select value thirteen. The write select multiplex circuit selects the current FIFO address difference that is stored in RAM during the DIFFERENCE2RAM state. The read select multiplexer circuit selects the least significant 12 bits of the scaled integrator value latched during the DIFFERENCE2RAM state. The add-subtract circuit is set to add during this state.

ACCUM2REG

Used to store the new integrator value into the 32 bit register.

ACCUM2RAM

Stores the latched value now in “rbig” RAM in the proper address location.

FILTER

Adds the current FIFO difference from “rsmll” to the scaled integrator value from “rbig”.

FILTER2REG

Used to load the new accumulated FIFO address difference into the 32 bit register.

FILTER2RAM

Stores the new accumulated FIFO address difference into “rbig” at address 15.

CALCFREQUENCY

Adds the calculated value during filter operation from “rbig” address 15 scaled through “M3:1x32” with the binary representation of a 5 kHz phase increment.

FREQ2REG

Stores the product of CALCFREQUENCY into a 32 bit register.

FREQ2RAM

Transfers the value from the register through “rbig” address 15 and through “M3:1x32” so it can be latched into the NCO circuit.

LATCHFREQ

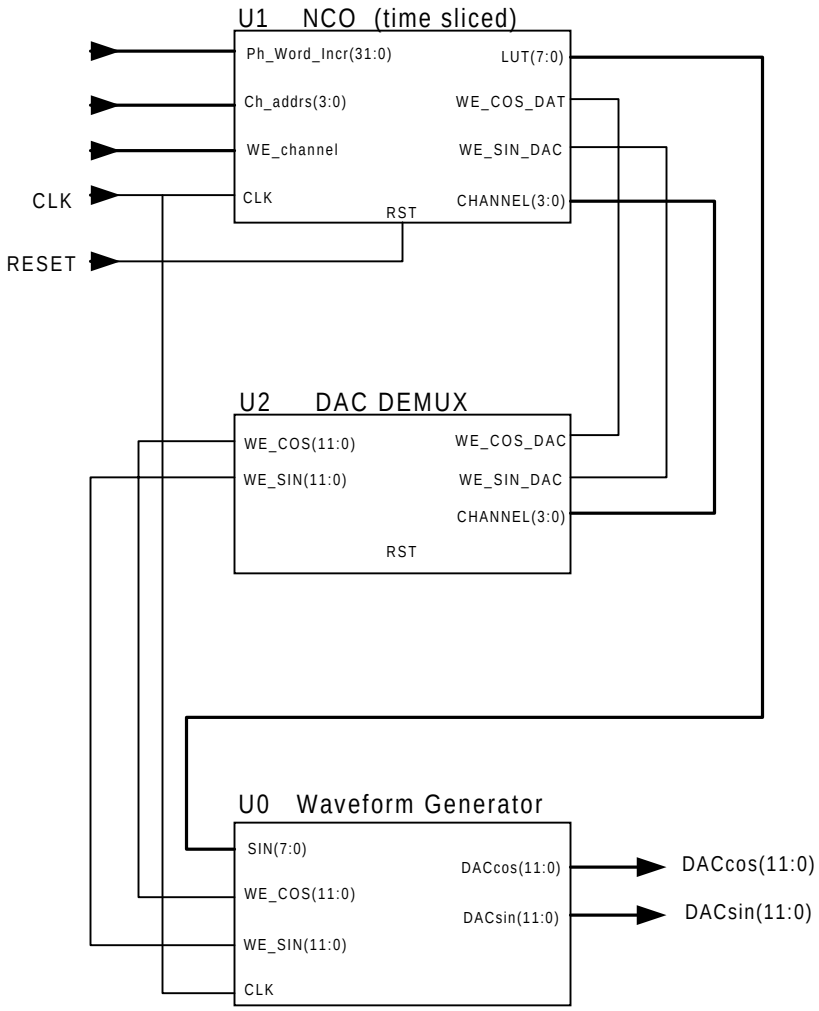
Latches the new phase increment into the NCO.

7.2.3 NCO and DACs Block

agram of the NCO & DAC circuit.

below shows the block diagram of the NCO & DAC circuit.

Figure 8. NCO & DAC Block Diagram



This NCO block is responsible for generating twelve different complex modulating frequencies that are up-converted in the RF2703 circuit using the fixed 44.731MHz local oscillator clock. These twelve frequencies correspond to the desynchronized DS3 clocks.

The AU unit computes desired frequencies and latches them in dual port RAM as 32 bit words. These 32 bit words are the values of phase increments that are accumulated in the NCO accumulator to produce the desired modulation frequency for each channel. These modulation frequencies are changing very slowly and each is updated at a 72 kHz rate. Because of the twelve channels, the dual port Phase Increment RAM is written to at 864 kHz.

The operation of the NCO is explained below for one frequency. All 12 channels are time multiplexed. It is easy to understand how the NCO generates all twelve frequencies once it is clear how it produces one frequency.

The 32 bit adder circuit takes, at the input A, the phase word from the Phase Increment RAM. This word determines how much the phase advance will be for the generated sinusoidal signal in one accumulation period. The other input to the adder is from a dual port 32 bit wide RAM. This RAM contains the current phase of all 12 clocks. Once the new phase of the signal is calculated and stored in the current phase RAM, the circuit will generate the current sinusoidal amplitude using a lookup table. At its 128 addresses this LUT contains the values of sinusoid amplitude coded as seven bits. Each address in respect to the previous one represents a 90°/128 increment of phase. Stepping through every address of this LUT will produce amplitudes that can be converted to one quarter cycle. Stepping through every second address will result in a one quarter cycle sine waveform but at twice the rate. Changing the sign of the address bits will point to an address that holds the amplitude value during the second quarter of the cycle, or first quarter of the cosine. Third and fourth quarters of the sine waveform are generated by inverting amplitude bits, the difference being that for the fourth quarter the address bits will be inverted as well. Similar operations allow the generation of a cosine waveform at the same time the sine waveform is being generated.

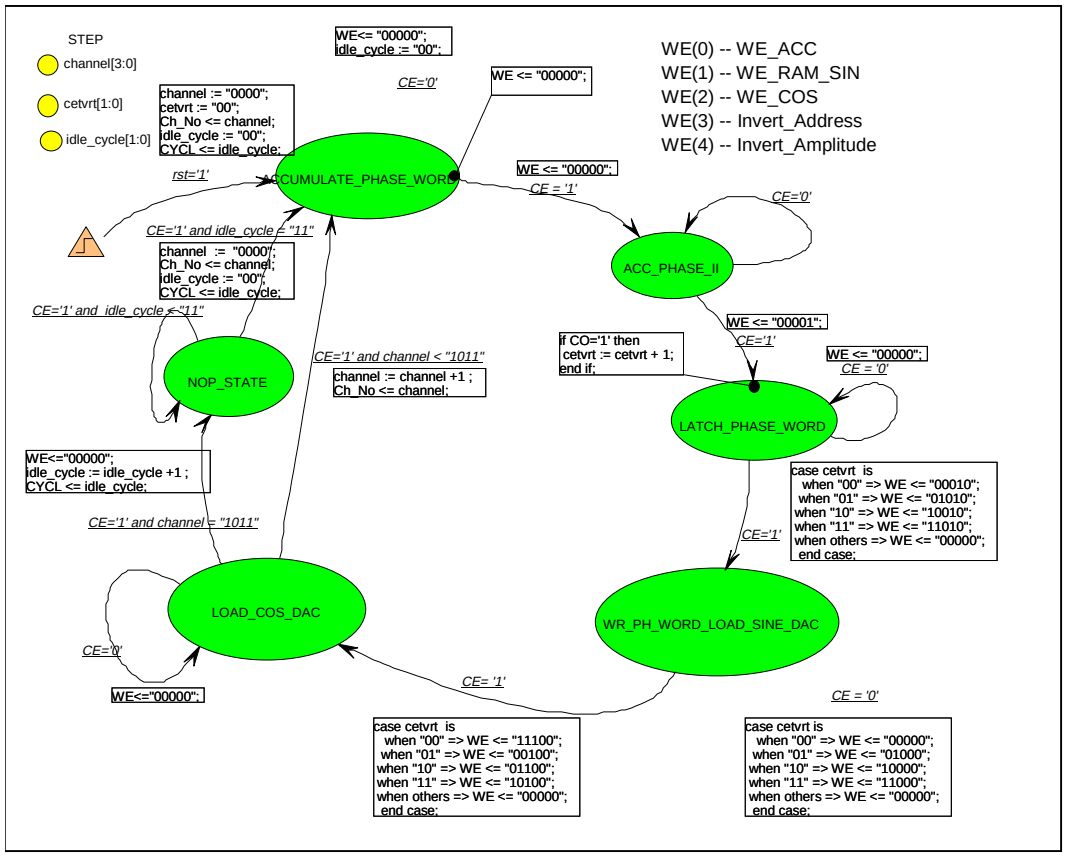
The rate of the change of the value for generating one sine or cosine waveform is tied to the length of the accumulator used by the DAC circuitry that is generating the sine and cosine waveforms. We have chosen an 8 bit accumulator for the DAC, so the update of the DAC value is at 202.5 kHz (51.84MHz/256) in the case that the system clock is 51.84 MHz. If system clock is 44.928 MHz than the update of the DAC value is at 175.5 kHz . To service all twelve channels using the same NCO circuitry the Finite State Machine (FSM) controls generation of the phase values. The phase values are then taken by 24 DAC circuits that generate 12 sine and 12 cosine waveforms.

The NCO FSM outlined below in Figure 9 has six states. Each operation is performed at system clock rate divided by four to ease the time specifications for the FSM circuit. The number of clock cycles for this operation is 256/4 = 64. Processing one phase word needs four steps: ACUMULATE_PHASE_WORD, LATCH_PHASE_WORD, WRITE_PHASE_WORD & LOAD_SINE_DAC and LOAD_COSINE_DAC.

The ACUMULATE_PHASE_WORD state involves adding 32 bits so it is beneficial to assign two cycles to this step. With a 5 state cycle for the state

machine, all 12 channels are processed in 60 cycles. The NOP_STATE is used to synchronize the state machine to 64 total cycles, as discussed above.

Figure 9. NCO State Diagram.



ACCUMULATE_PHASE_WORD

The phase word increment is taken from the phase word increment RAM and added to the current phase word value from the phase value RAM. This is a two cycle operation, and a ripple carry adder can be used.

LATCH_PHASE_WORD

Latches the added values in REG so we decouple the combinatorial logic of the adder and phase value RAM values.

WRITE_PHASE_WORD & LOAD_SINE_DAC

Writes the latched value of the phase into the phase value RAM. At the same time we can load the value of the sinusoidal word from the LUT into the sine

DAC. The signal from REGISTER to both RAM and DAC registers has 77 nsec to propagate.

LOAD_COSINE_DAC

Loads the phase value from the accumulator REG to cosine register.

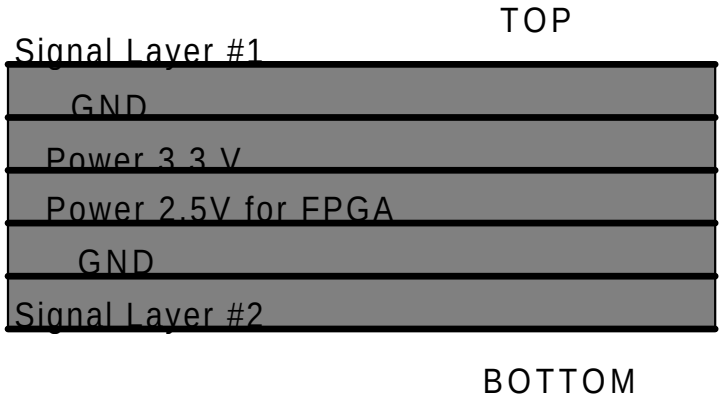
NOP_STATE

This state is used to synchronize the DAC to the process of calculating values for the DACs. It is four cycles long and is entered when the channel count exceeds 12.

7.3 LAYOUT CONSIDERATIONS

The PCB has six layers stacked as shown below in Figure 10.

Figure 10 - PCB Layers



Because the board contains some sensitive analog circuits special care should be taken in layout. There are signals that are almost 40 dB different in level so a ground ring should be established around the quadrature modulator circuits to serve as an electrostatic shield.

In the case of the twelve upconverters we should be careful because the mutual coupling of different 44.736 MHz clocks is translated into jitter at the output. Also, a high level TTL signal from the FPGA can couple to the low level signals.

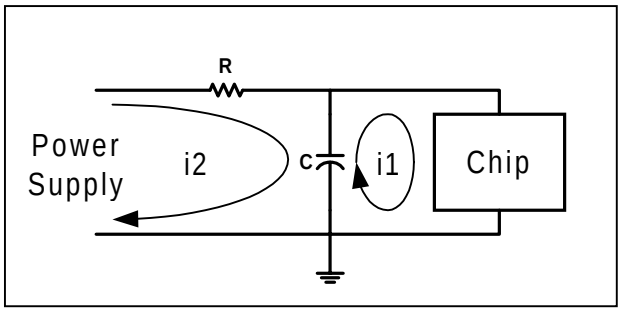
The FPGA, configuration PROM, 44.731 MHz crystal oscillator and twelve quadrature modulators occupy less than 4”x4” square shaped area. This makes it easier to adopt this portion of the circuit into designs.

Although the lines on the board are short, most of them have at least source matching. This reduces ringing due to multiple reflections on the lines.

All chips on the board receive power through a series resistor. This resistor serves to limit in-rush current. During the debugging phase the power supply series resistor provides a simple, fast method of detecting a faulty IC. The resistors can also be used to estimate power supply current for each IC.

Another benefit of using series resistors in the power supply is reduced EMI and noise generated by the board. Referring to Figure 11 below, the instantaneous switching current (i1) is flowing locally to the IC fed by the bypass capacitor (C). This current can have very fast rise times but due to its small loop area, this current loop is not an effective radiator. The capacitor C discharges as it supplies current i1 to the IC and capacitor C is recharged from the power supply using current i2. If there was no series resistor R, then there would be nothing to restrict the rise and fall times of the charging current, i2. In addition, this current has a large loop area, therefore it will radiate more. By using the series resistor R, the edge rates, and thereby the high frequency content, of the i2 recharging current is limited. This reduces the radiated EMI caused by the flow of current i2. This arrangement also reduces high frequency noise on the ground plane.

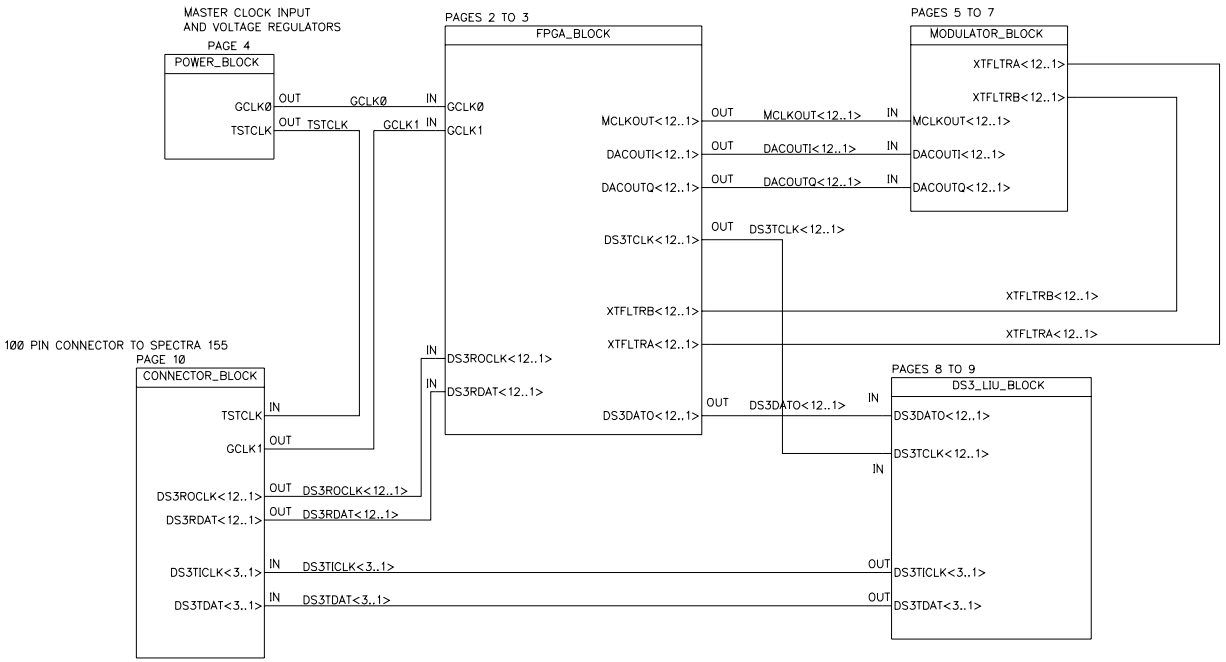
Figure 11 - Supply Line Series Resistor Current Flow



The position of the power supply sources, the regulators for 3.3 V and 2.5 V, is such that the flow of return currents the for analog quadrature modulators will not pass across the area of digital driver circuits. The reason for using two regulators is so the board can be powered by the SPECTRA-155 reference design.

8 SCHEMATICS

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



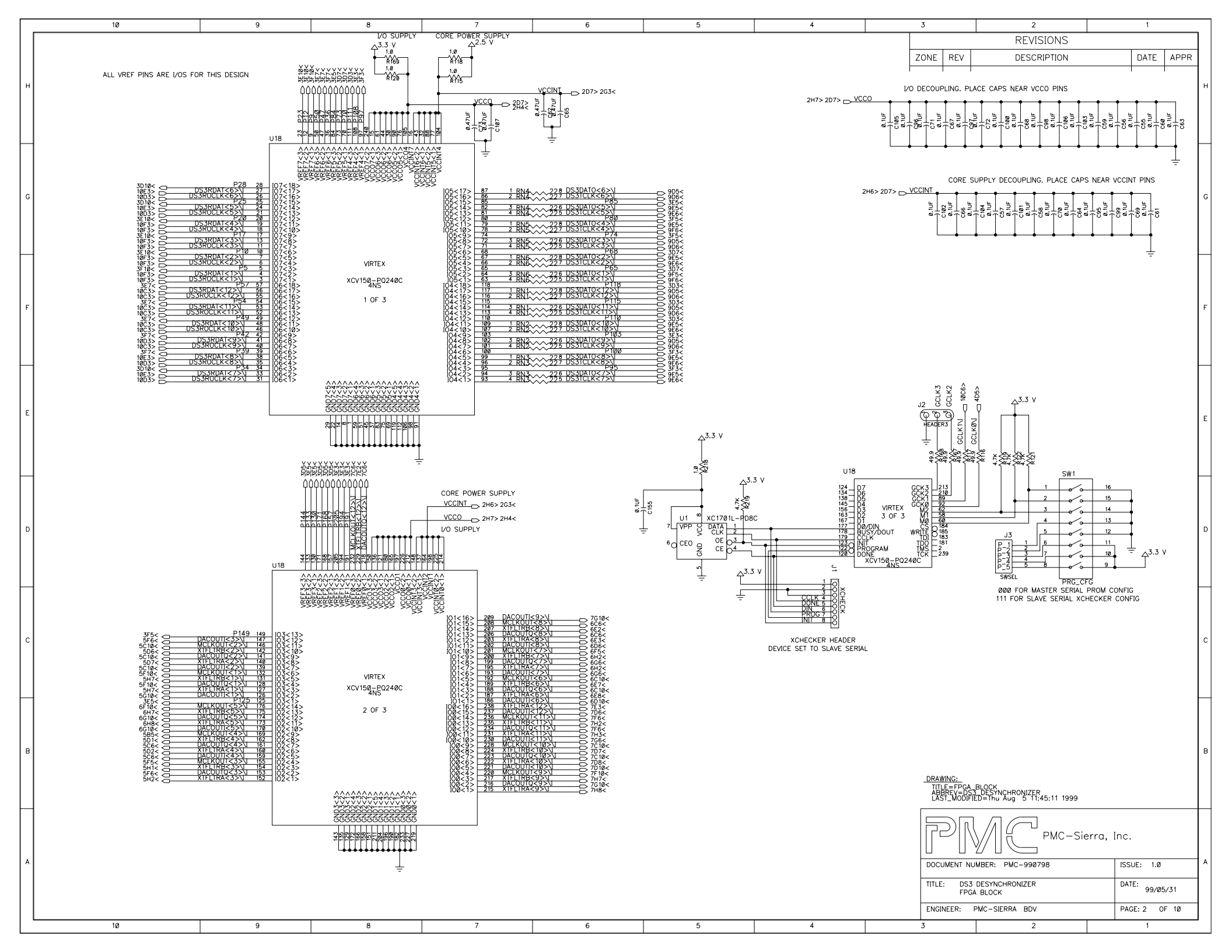
SIGNAL DESCRIPTION:

XTFLTRA/B: EXTERNAL COMPONENT CONNECTIONS TO AMPLIFY (HARD LIMIT) MODULATED OUTPUT SIGNALS FROM SSB MODULATORS
DS3DCLK: EXTERNALLY DESYNCHRONIZED CLOCK SIGNAL
DACOUTI/Q: I AND Q DAC OUTPUTS TO SSB MODULATOR
MCLKOUT: CLOCK SIGNAL FOR LOCAL OSCILLATOR INPUTS OF SSB MODULATOR
DS3DATO: DATA STREAM TO BE OUTPUT THROUGH LIU
DS3TICLK: TRANSMIT CLOCK INPUT TO SPECTRA-155
DS3TDAT: TRANSMIT DATA STREAM INPUT TO SPECTRA-155
GCLK: GLOBAL CLOCK INPUTS FOR LOCAL OSCILLATOR. SPLIT IN FPGA FOR ALL 12 CHANNELS.
DS3ROCLK: RECEIVE CLOCK FROM SPECTRA-155 TO DESYNCH CIRCUIT
DS3RDAT: RECEIVE DATA STREAM FROM SPECTRA-155 TO DESYNCH CIRCUIT
TSTCLK: EXTERNAL 51.84 MHZ CLOCK SOURCE FOR TESTING

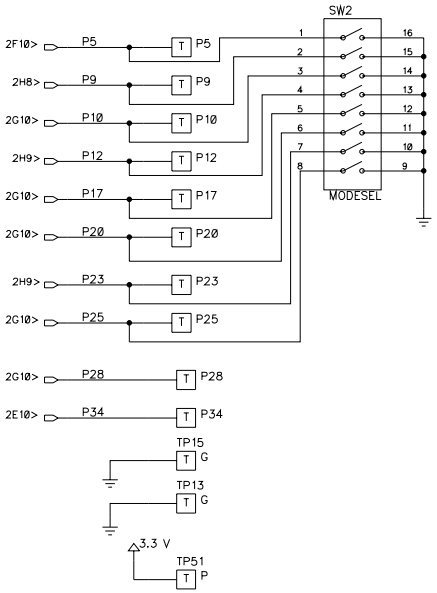
DRAWING:
TITLE=DS3_DESYNC_R1
ABBREV=DS3_DESYNCHRONIZER
LAST_MODIFIED=Thu Aug 5 11:39:13 1999

PMC-Sierra, Inc.

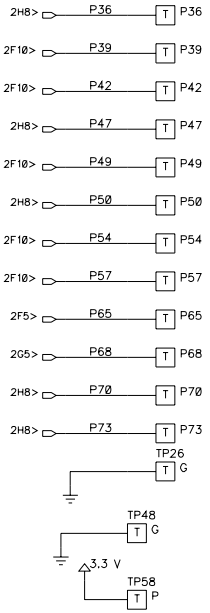
DOCUMENT NUMBER: PMC-990798	ISSUE: 1.0
TITLE: DS3 DESYNCHRONIZER BLOCK DIAGRAM	DATE: 99/05/31
ENGINEER: PMC-SIERRA BDV	PAGE: 1 OF 10

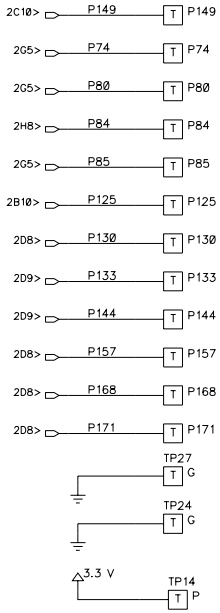

REVISIONS
ZONE | REV | DESCRIPTION | DATE | APPR
ALL VREF PINS ARE I/OS FOR THIS DESIGN
I/O SUPPLY
CORE POWER SUPPLY
3.3 V
2.5 V
VCCINT
VCCO
I/O DECOUPLING. PLACE CAPS NEAR VCCO PINS
CORE SUPPLY DECOUPLING. PLACE CAPS NEAR VCCINT PINS
U18
VIRTEX
XCV150-PQ240C
4NS
1 OF 3
2 OF 3
3 OF 3
U1
XC1701L-PD8C
J2
HEADER3
J3
SW1
SWSEL
PRG_CFG
000 FOR MASTER SERIAL PROM CONFIG
111 FOR SLAVE SERIAL XCHECKER CONFIG
XCHECKER HEADER
DEVICE SET TO SLAVE SERIAL
DRAWING:
TITLE=FPGA_BLOCK
ABBREV=DS3_DESYNCHRONIZER
LAST_MODIFIED=Thu Aug 5 11:45:11 1999
PMC-Sierra, Inc.
DOCUMENT NUMBER: PMC-990798
ISSUE: 1.0
TITLE: DS3 DESYNCHRONIZER FPGA BLOCK
DATE: 99/05/31
ENGINEER: PMC-SIERRA BDV
PAGE: 2 OF 10

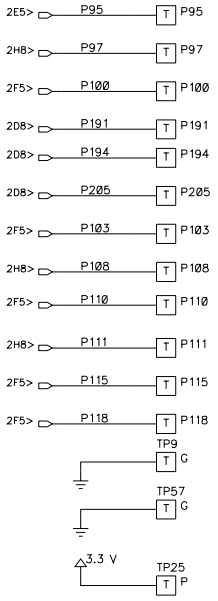
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



DO NOT POPULATE ON PCB





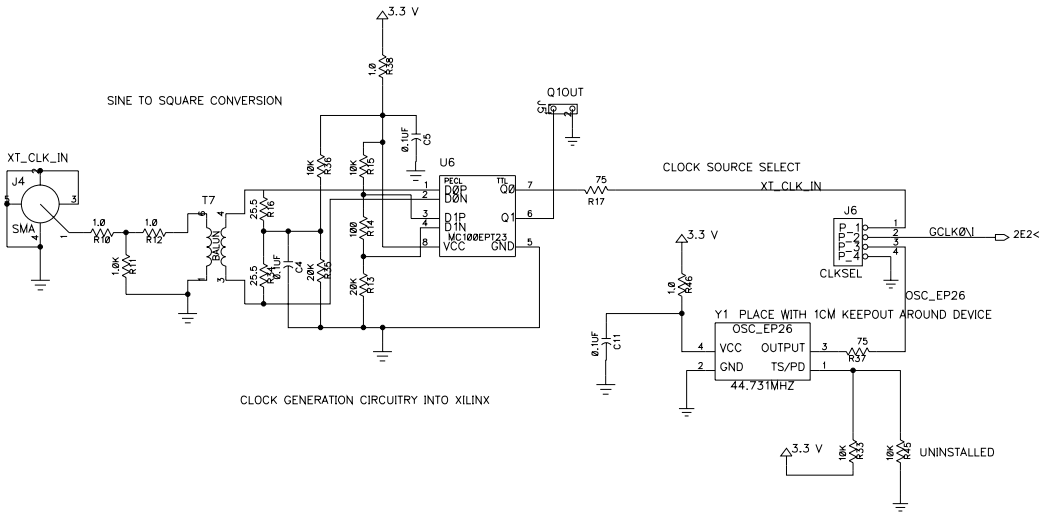


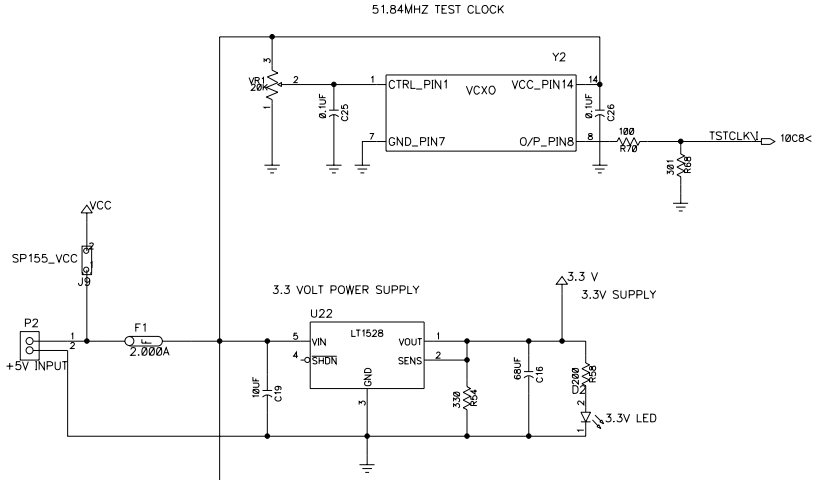
DRAWING:
TITLE=TEST_POINTS
ABBREV=DS3_DESYNCHRONIZER
LAST_MODIFIED=Thu Aug 5 11:45:13 1999

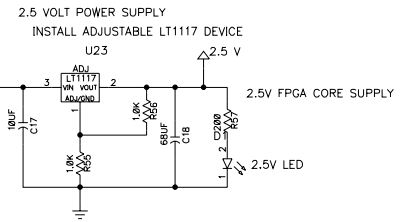
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-990798	ISSUE: 1.0
TITLE: DS3 DESYNCHRONIZER TEST POINTS	DATE: 99/05/31
ENGINEER: PMC-SIERRA BDV	PAGE: 3 OF 10

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR





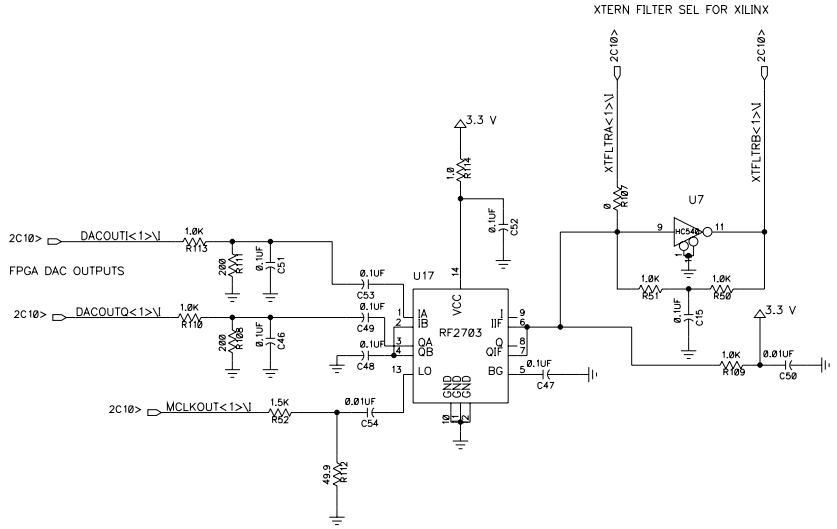


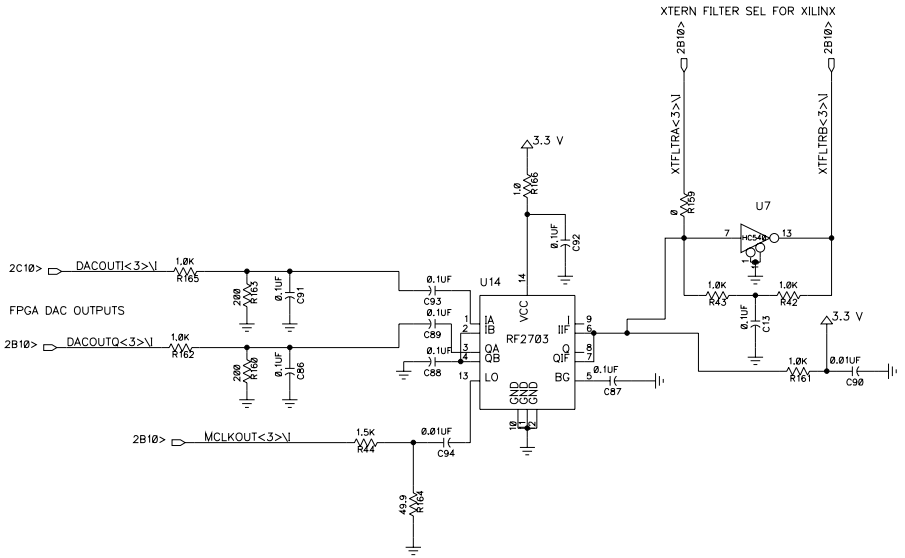
DRAWING:
TITLE=POWER_BLOCK
ABBREV=DS3_DESYNCRONIZER
LAST_MODIFIED=Thu Aug 5 11:45:20 1999

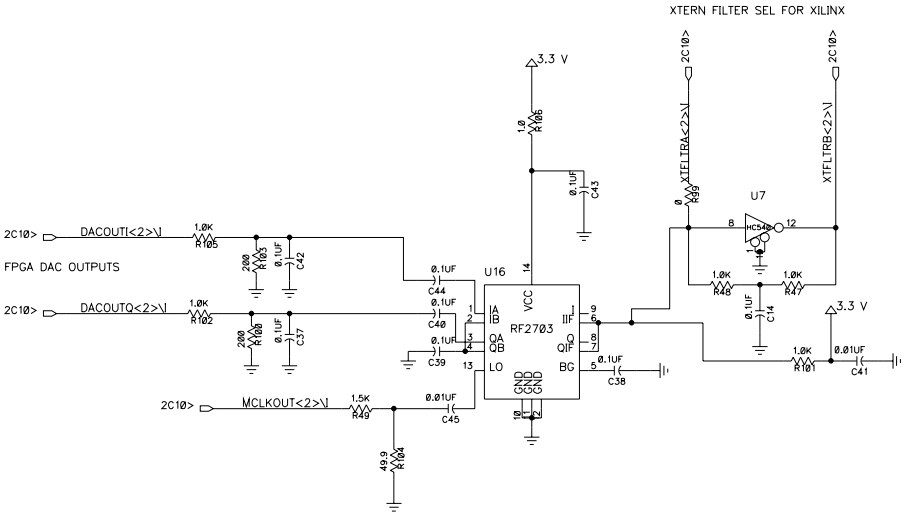
PMC-Sierra, Inc.

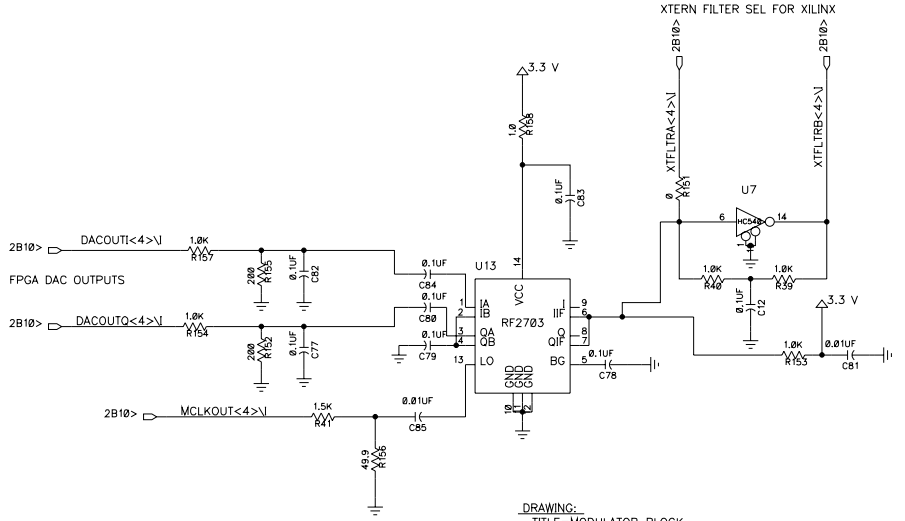
DOCUMENT NUMBER: PMC-990798	ISSUE:
TITLE: DS3 DESYNCHRONIZER FPGA POWER SUPPLY	DATE: 99/06/07
ENGINEER: PMC-SIERRA	PAGE: 4 OF 10

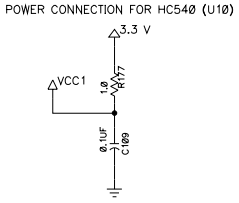
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR









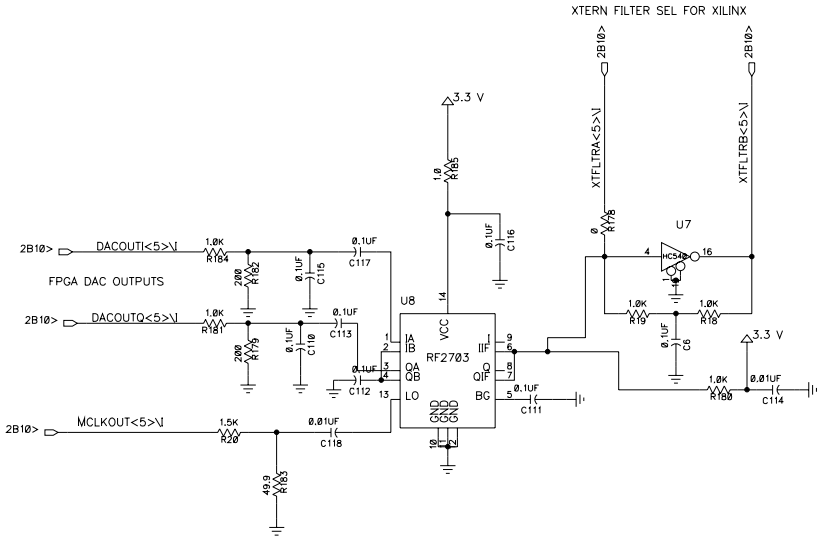


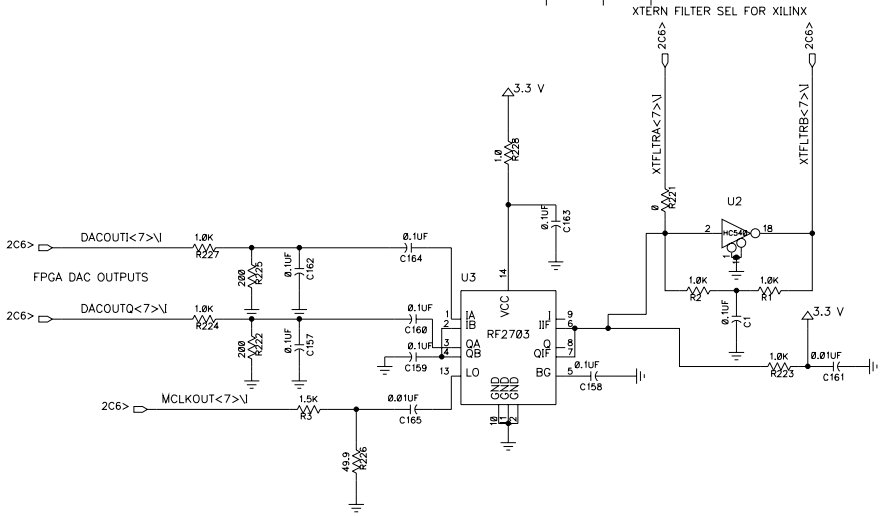
DRAWING:
TITLE=MODULATOR BLOCK
ABBREV=DS3_DESYNCHRONIZER
LAST_MODIFIED=Thu Aug 5 11:45:23 1999

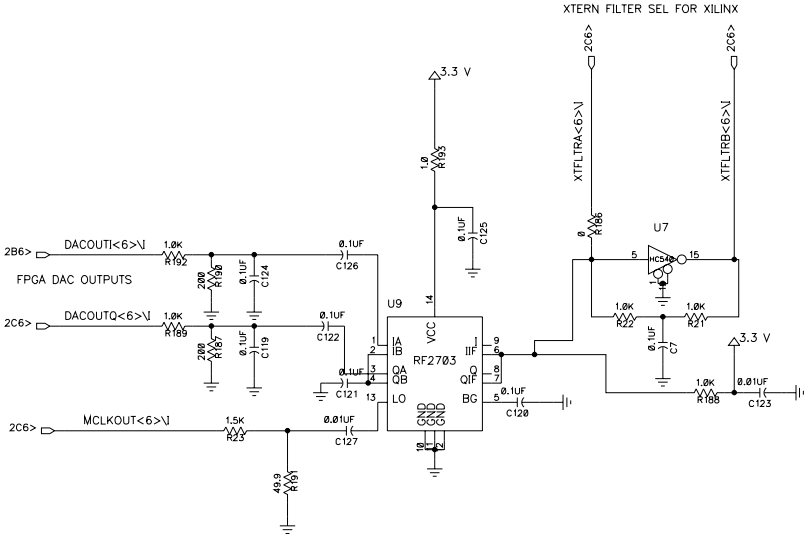
PMC-Sierra, Inc.

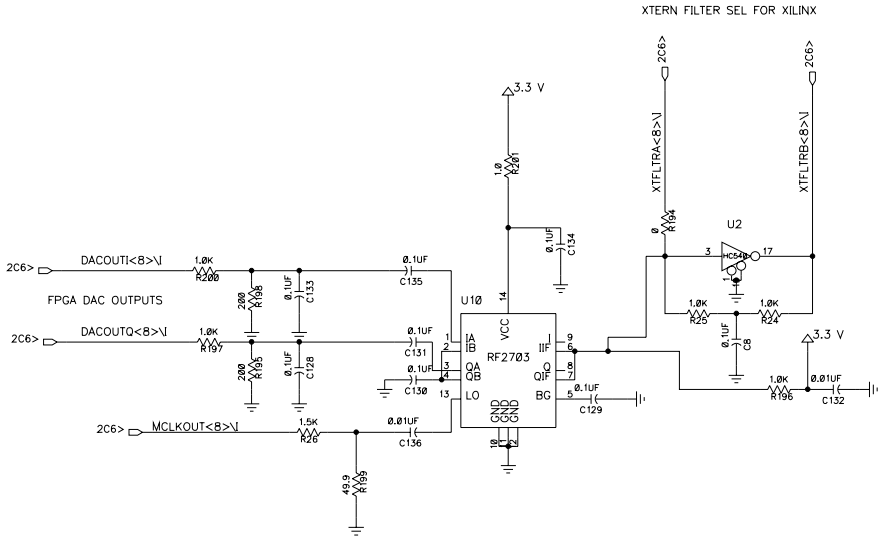
DOCUMENT NUMBER: PMC-990798	ISSUE: 1.0
TITLE: DS3_DESYNCHRONIZER MODULATOR BLOCK	DATE: 99/05/31
ENGINEER: PMC-SIERRA BDV	PAGE: 5 OF 10

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR







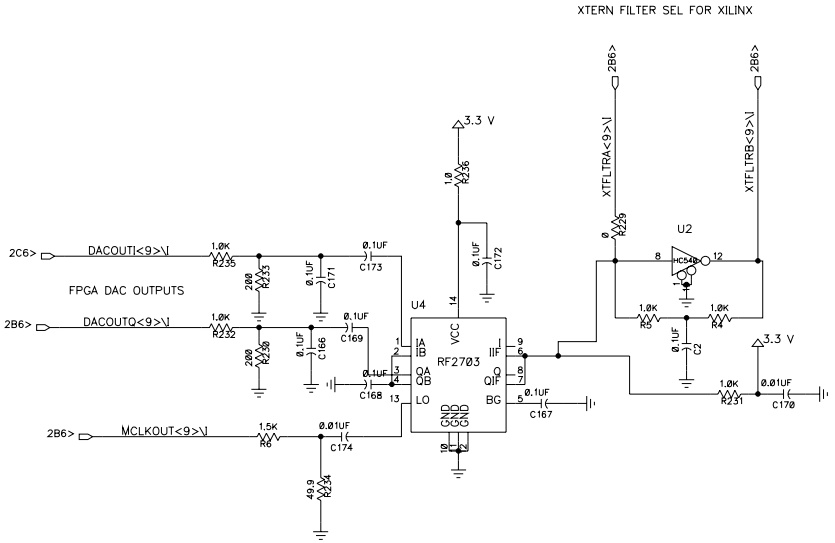


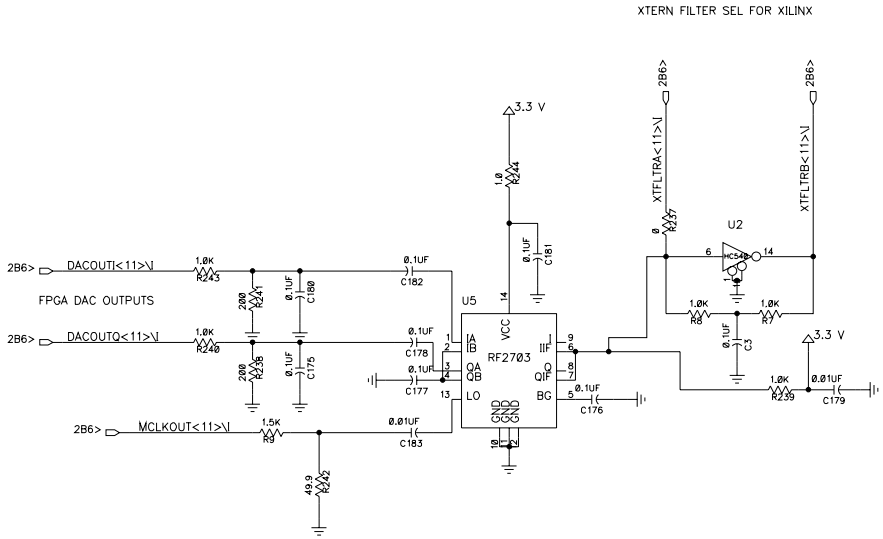
DRAWING:
TITLE=MODULATOR_BLOCK
ABBREV=DS3_DESYNCHRONIZER
LAST_MODIFIED=Thu Aug 5 11:45:26 1999

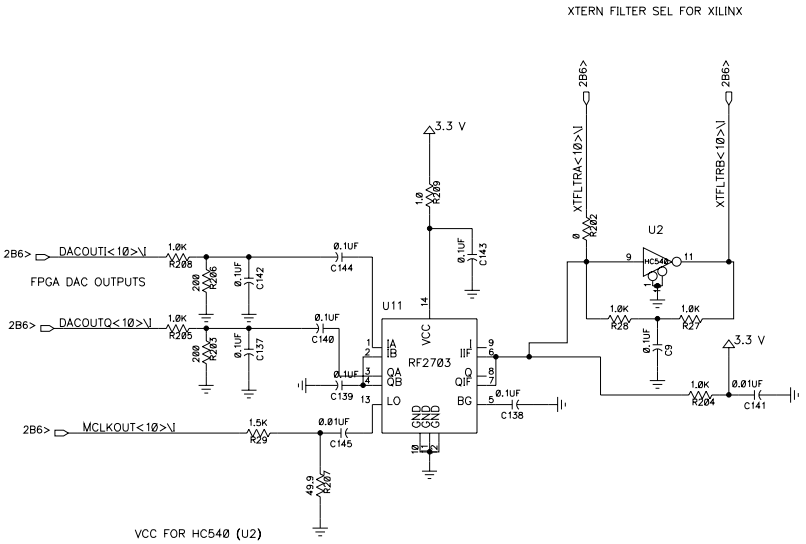
PMC-Sierra, Inc.

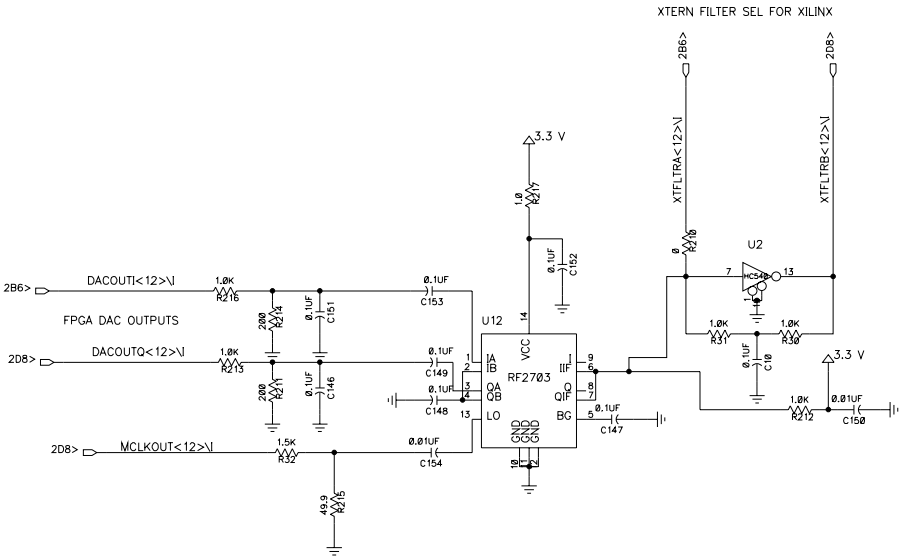
DOCUMENT NUMBER: PMC-990798	ISSUE: 1.0
TITLE: DS3 DESYNCHRONIZER MODULATOR BLOCK	DATE: 99/06/03
ENGINEER: PMC-SIERRA BDV	PAGE: 6 OF 10

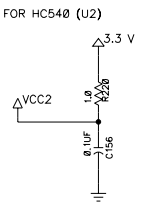
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR









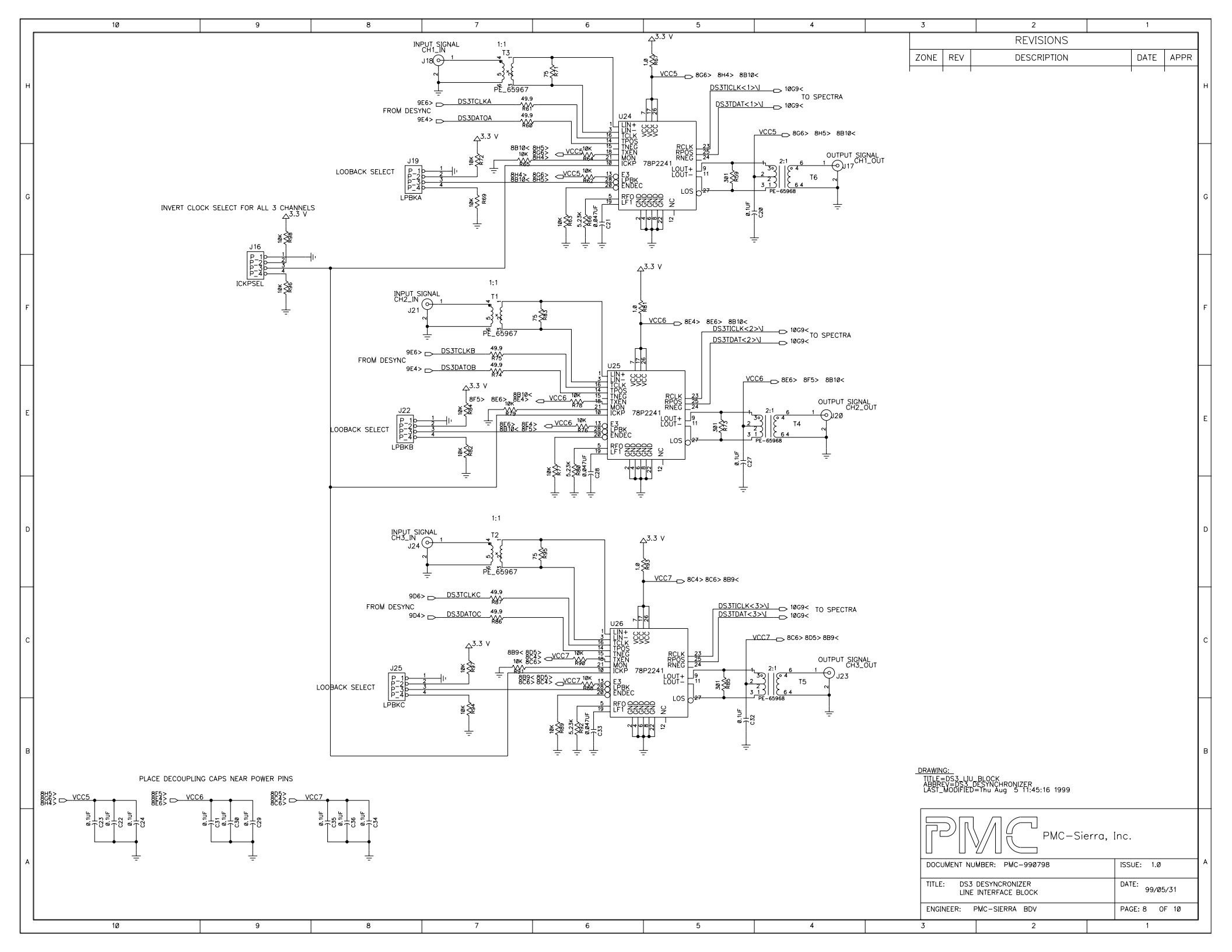


DRAWING:
TITLE=MODULATOR_BLOCK
ABBREV=DS3_DESYNCHRONIZER

LAST_MODIFIED=Thu Aug 5 11:45:30 1999

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-990798	ISSUE: 1.0
TITLE: DS3 DESYNCHRONIZER MODULATOR BLOCK	DATE: 99/06/09
ENGINEER: PMC-SIERRA BDV	PAGE: 7 OF 10



REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

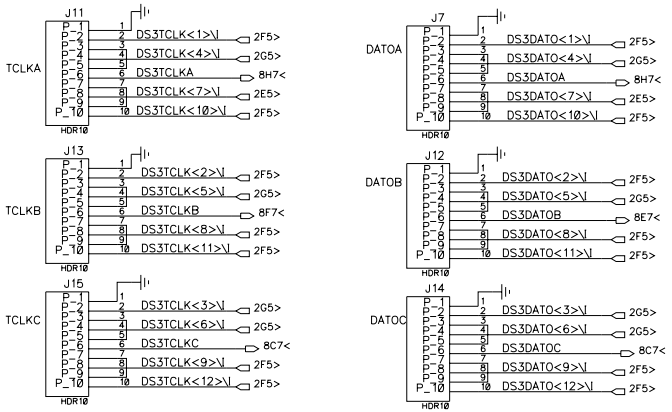
DRAWING:
TITLE=DS3 LIU BLOCK
ABBREV=DS3 DESYNCHRONIZER
LAST_MODIFIED=Thu Aug 5 11:45:16 1999

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-990798	ISSUE: 1.0
TITLE: DS3 DESYNCRONIZER LINE INTERFACE BLOCK	DATE: 99/05/31
ENGINEER: PMC-SIERRA BDV	PAGE: 8 OF 10

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

JUMPER MUXES FOR LIU SIGNALS



DRAWING:
TITLE=LIU INTERFACE MUX
ABBREV=DS3_DESYNCHRONIZER

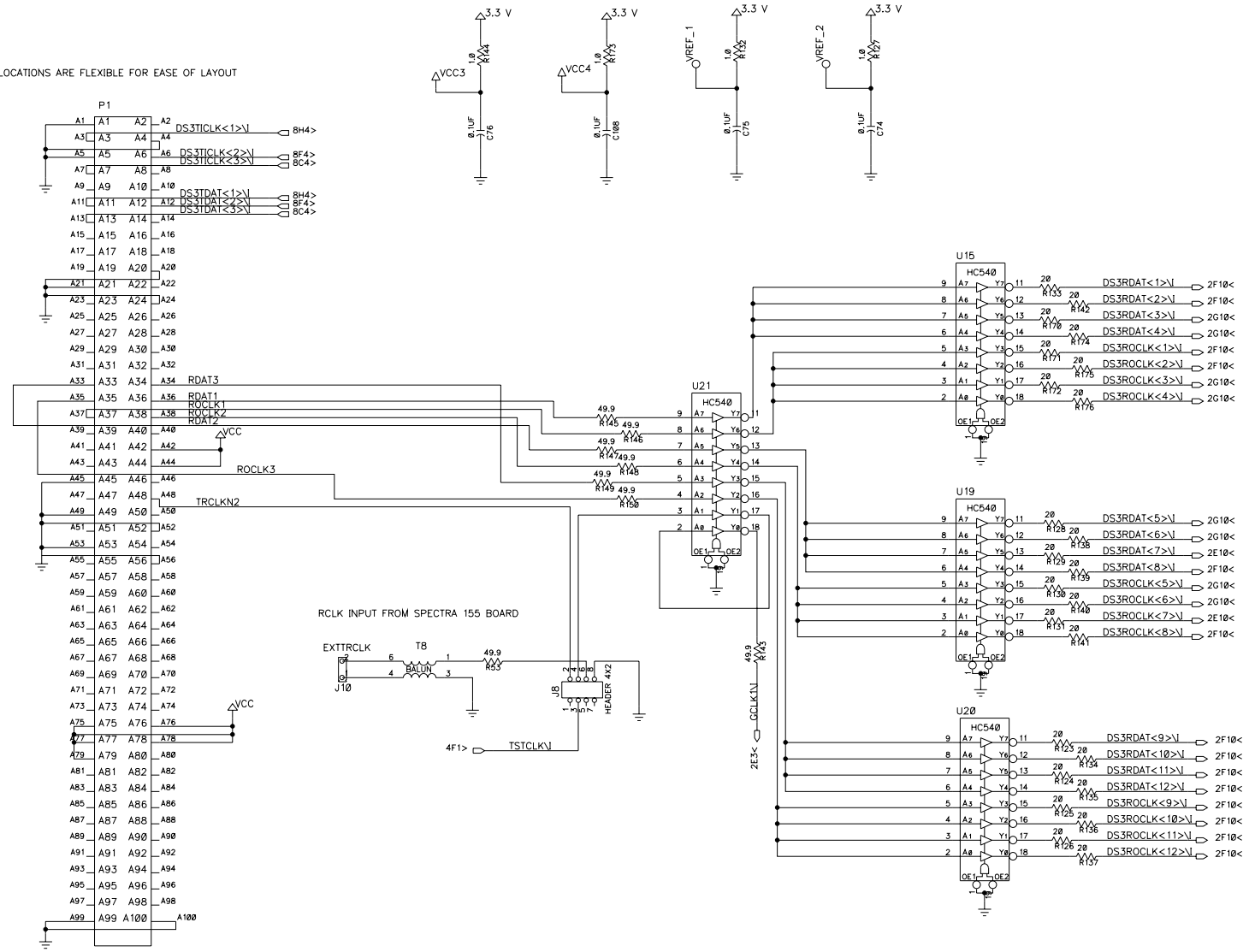
LAST_MODIFIED=Thu Aug 5 11:45:18 1999

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-990798	ISSUE: 1.0
TITLE: DS3 DESYNCHRONIZER LIU INTERFACE MUX	DATE: 99/06/10
ENGINEER: PMC-SIERRA BDV	PAGE: 9 OF 10

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

PIN LOCATIONS ARE FLEXIBLE FOR EASE OF LAYOUT



DRAWING:
TITLE=CONNECTOR_BLOCK
ABBREV=DS3_DESYNCHRONIZER

LAST_MODIFIED=Thu Aug 5 11:45:33 1999

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-990798	ISSUE: 1.0
TITLE: DS3 DESYNCHRONIZER CONNECTOR BLOCK	DATE: 99/06/10
ENGINEER: PMC-SIERRA BDV	PAGE: 10 OF 10

9 BILL OF MATERIALS

Table 2. Major Components List

Ref. No.	Component Description	Package Type	Quantity
U1	Xilinx configuration PROM XC1701L_PD8C	DIP8	1
U2, U7, U15, U19 U20, U21	Motorola Semiconductor octal tristate buffer 74HC540A	SOIC20W	6
U3-U5, U8-U14, U16, U17	RF Micro Devices single sideband modulator RF2703	SO14-NB	12
U6	Motorola Semiconductor ECL to TTL Converter MC100EPT23D	SOIC8	1
U18	Xilinx Virtex FPGA XCV150-4PQ240	PQFP240	1
U22	Linear Technology 3.3V regulator LT1528CQ	TO-263	1
U23	Linear Technology adjustable regulator LT1117CST	SOT223	1
U24-26	TDK Semiconductor E3/DS3/STS-1 Transceiver 78P2241	PLCC28	3
Y1	Ecliptek oscillator EP2645TTS-44.731M	SMT	1
T1-T3	Pulse Engineering transformer PE65967	LS-1	3
T4-T6	Pulse Engineering transformer PE65968	LS-1	3

10 APPENDIX A - PLL CALCULATION

DIGITAL PLL for DS3 Desynchronizer Unit

June-29-99

Loop with perfect integrator

$i := 1 .. 10000$

$fs := 72 \cdot 10^3$

$T := \frac{1}{fs}$

Sampling period $T = 1.388888888910^{-5}$

Lead_lag Filter Characteristic

$s_i := i \cdot 2 \cdot \pi \cdot .001 \cdot i$

$z_i := \frac{1}{1 - s_i \cdot T}$

$Ka := \frac{1}{1}$ $Kb := \frac{1}{2^{22}}$

$GPZ_i := Ka + \frac{Kb \cdot z_i}{z_i - 1}$ $\psi_i := Im\left(\ln\left(GPZ_i\right)\right)$

$z_i := \frac{1}{1 - s_i \cdot T}$

$Size\_of\_phase\_accumulator := 2^{32}$

$Size\_of\_DAC\_accumulator := 2^8$

$FrDAC1 := 51.84 \cdot 10^6$ **System Clock Frequency**

$FrDAC2 := 44.928 \cdot 10^6$

$G := 2^{16}$ **G is the gain implemented in a AU block in XILINX.**

$$Fnco := \frac{FrDAC2}{Size\_of\_DAC\_accumulator} \qquad Fnco = 1.755 \cdot 10^5$$

$$Tnco := \frac{1}{Fnco} \qquad znco_i := \frac{1}{1 - s_i \cdot Tnco}$$

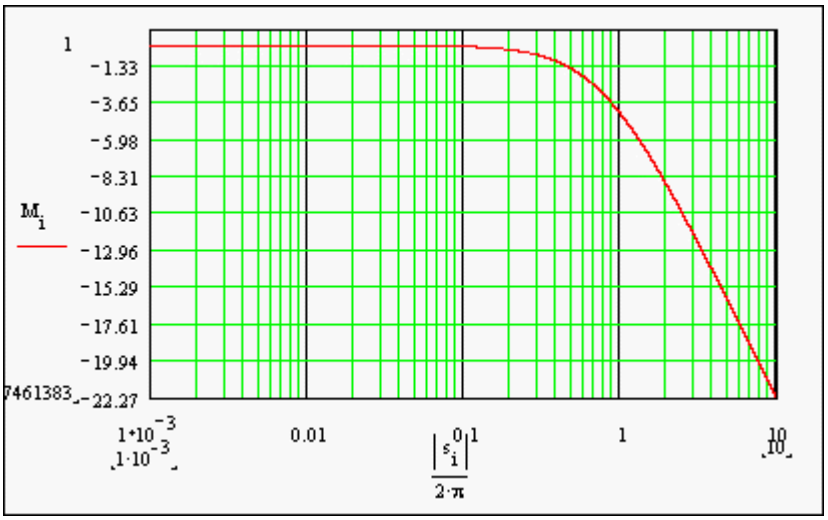
$$Kvco := \frac{2 \cdot \pi \cdot Fnco}{4 \cdot Size\_of\_phase\_accumulator}$$ **rad/bit of FIFO difference**

$$Kv_i := \frac{Tnco}{znco_i - 1}$$ **To take into account descrete change of frequency at interval Tnco**

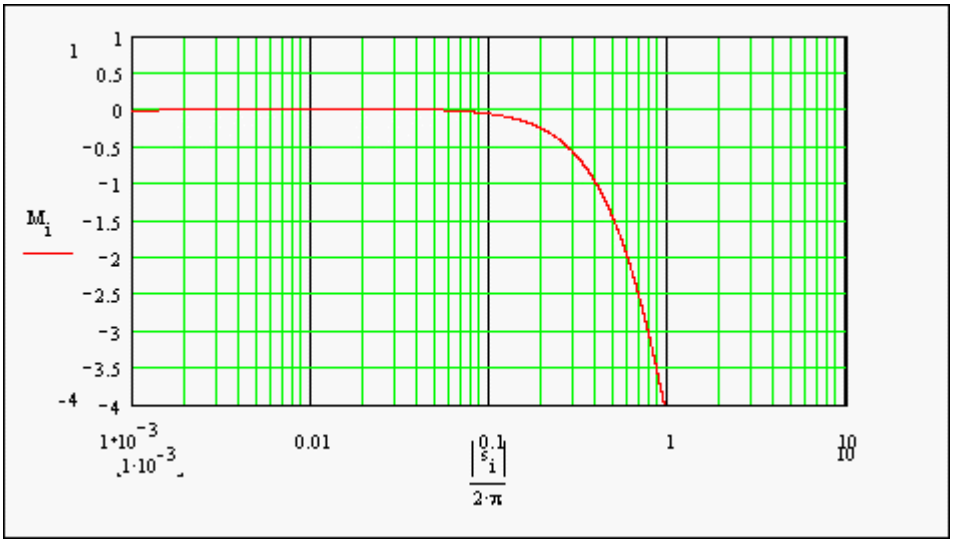
$$CL_i := \frac{GPZ_i \cdot Kv_i \cdot Kvco \cdot G}{1 + GPZ_i \cdot Kv_i \cdot Kvco \cdot G}$$

$$M_i := 20 \cdot \log\left(\left| CL_i \right|\right) \qquad \Theta_i := Im\left(\ln\left(CL_i\right)\right)$$

Closed Loop Transfer Function



Close-up of the Closed Loop Transfer Function



11 APPENDIX B – SINE LUT CREATION

Calculation of LUT for SINE waveform generation

We shall define several usefull functions first

$$\text{quant}(x, N, MIN, MAX) := \left| \begin{array}{l} st \leftarrow \dfrac{(MAX - MIN)}{2^N} \\ i \leftarrow 0 \\ \text{while } x \geq MIN + st \cdot i \\ \quad i \leftarrow i + 1 \\ i - 1 \end{array} \right.$$

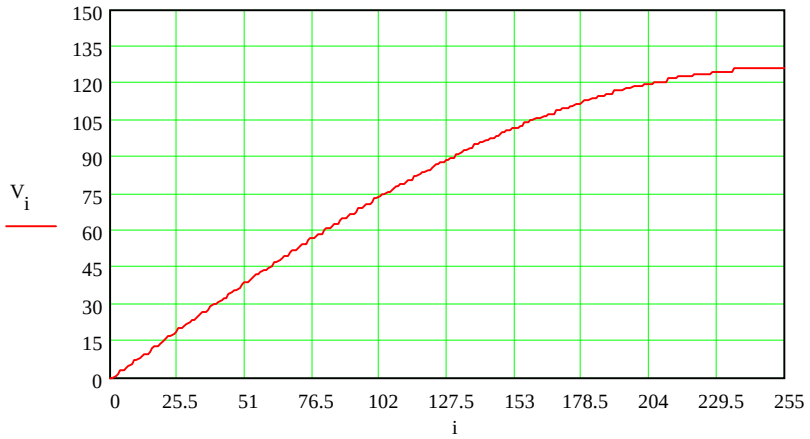
QUANT function takes input x and quantize it to N bits with output value ranging from MIN to MAX

SIN_ROM function takes input phase and quantizes it to M bits. Then converts this quantized phase to quantized amplitude of the sinusoidal signal.

$$\text{sin\_rom}(\text{phase}, N, M) := \left[\left| \begin{array}{l} \text{radph} \leftarrow \dfrac{\pi}{2} \cdot \dfrac{\text{quant}\left(\text{phase}, M, 0, 2^M\right)}{2^M} \\ \text{SIN} \leftarrow \sin(\text{radph}) \cdot \left(2^N - 1\right) \\ \text{quant}\left(\text{SIN}, N, 0, 2^N\right) \end{array} \right. \right]$$

$$i := 0 .. 2^8 - 1$$

$$V_i := \text{sin\_rom}(i, 7, 8)$$



NUM2BIN function converts the decimal numerical value to binary.

$$nc(num) := \begin{cases} 1 & \text{if } num \geq 0 \\ 0 & \text{otherwise} \end{cases}$$

$$num2bin(num, N) := \left| \begin{array}{l} s \leftarrow 2^{N-1} \\ \text{for } i \in 0..N-1 \\ \quad \left| \begin{array}{l} s \leftarrow 2^{(N-1-i)} \\ X \leftarrow num - s \\ V_i \leftarrow nc(X) \\ num \leftarrow num - s \cdot V_i \end{array} \right. \\ V \end{array} \right.$$

Print binary values to file "SINROM.dt"

$$ZT := \left| \begin{array}{l} \text{for } i \in 0..63 \\ \quad Z_i \leftarrow num2bin(i, 7) \\ Z \end{array} \right.$$

$$XX := ZT$$

$$WRITEPRN("SINROM.dt") := XX$$

12 APPENDIX C – INTERFACING TO THE SPECTRA-155 REFERENCE DESIGN

On the SPECTRA-155 reference board lift pins 10 and 11 of U34. Solder wire from test point RXC to lifted pins 10 and 11 of U34.

NOTES

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