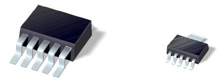


ULTRALOW-NOISE, HIGH PSRR, FAST RF 1-A LOW-DROPOUT LINEAR REGULATORS

FEATURES

- 1-A Low-Dropout Regulator With EN
- Available in 1.8-V, 2.5-V, 2.8-V, 3-V, 3.3-V, and Adjustable
- High PSRR (53 dB at 10 kHz)
- Ultralow Noise (40 µV)
- Fast Start-Up Time (50 µs)
- Stable With a 1-µF Ceramic Capacitor
- Excellent Load/Line Transient
- Very Low Dropout Voltage (250 mV at Full Load, TPS79630)
- 5-Pin SOT223-5 and 5-Pin DDPAKPackage

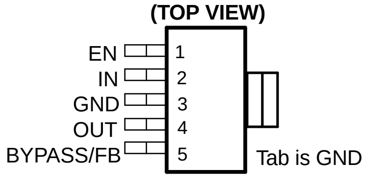
APPLICATIONS

- Powering Noise-Sensitive Circuitry
  – - RF
  – - Audio
  – - VCOs
- DSP/FPGA/Microprocessor Supplies
- Post Regulator for Switching Supplies

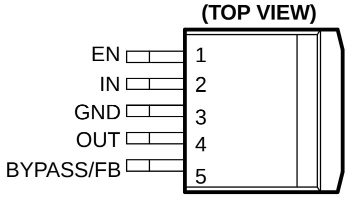
DESCRIPTION

The TPS796xx family of low-dropout (LDO) low-power linear voltage regulators features high power supply rejection ratio (PSRR), ultralow noise, fast start-up, and excellent line and load transient responses in small outline, SOT223-5 and 5-pin DDPAK packages. Each device in the family is stable with a small 1-µF ceramic capacitor on the output. The family uses an advanced, proprietary BiCMOS fabrication process to yield extremely low dropout voltages (e.g., 250 mV at 1 A). Each device achieves fast start-up times (approximately 50 µs with a 0.001 µF bypass capacitor) while consuming very low quiescent current (265 µA typical). Moreover, when the device is placed in standby mode, the supply current is reduced to less than 1 µA. The TPS79630 exhibits approximately 40 μV_{RMS} of output voltage noise with a 0.1 µF bypass capacitor. Applications with analog components that are noise sensitive, such as portable RF electronics, benefit from the high PSRR, low noise features, and the fast response time.

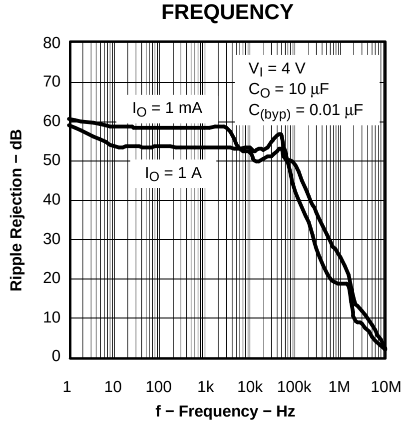
DCQ PACKAGE
SOT223-5
(TOP VIEW)



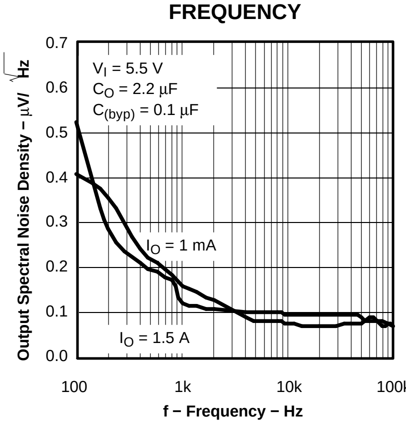
KTT (DDPAK) PACKAGE
(TOP VIEW)



TPS79630
RIPPLE REJECTION
vs
FREQUENCY



TPS79630
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY



AVAILABLE OPTIONS

T_J	voltage	package	part number	SYMBOL
-40°C to 125°C	1.2 to 5.5 V	SOT223-5	TPS79601DCQ[1]	PS79601
		DDPAK	TPS79601KTT[1]	TPS79601
	1.8 V	SOT223-5	TPS79618DCQ[1]	PS79618
		DDPAK	TPS79618KTT[1]	TPS79618
	2.5 V	SOT223-5	TPS79625DCQ[1]	PS79625
		DDPAK	TPS79625KTT[1]	TPS79625
	2.8 V	SOT223-5	TPS79628DCQ[1]	PS79628
		DDPAK	TPS79628KTT[1]	TPS79628
	3 V	SOT223-5	TPS79630DCQ[1]	PS79630
		DDPAK	TPS79630KTT[1]	TPS79630
	3.3 V	SOT223-5	TPS79633DCQ[1]	PS79633
		DDPAK	TPS79633KTT[1]	TPS79633

(1) Add **R** for DCQ devices in tape and reel (quantity =2500). Add **T** for KTT devices in tube (quantity = 50). Add **R** for KTT devices in tape and reel (quantity = 500).

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)[1][2]

	UNIT
Input voltage range	-0.3 V to 6 V
Voltage range at EN	-0.3 V to V_I + 0.3 V
Voltage on OUT	6 V
Peak output current	Internally limited
ESD rating, HBM	2 kV
ESD rating, CDM	500 V
Continuous total power dissipation	See Dissipation Rating Table
Operating junction temperature range, T_J	-40°C to 150°C
Storage temperature range, T_{stg}	-65°C to 150°C

(1) Stresses beyond those listed under„ absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under„ recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

PACKAGE DISSIPATION RATINGS

PACKAGE	BOARD	$R_{\Theta JC}$	$R_{\Theta JA}$
DDPAK	High K (see Note [1])	2 °C/W	23 °C/W
SOT223	Low K (see Note [2])	15 °C/W	53 °C/W

(1) The JEDEC high K (2s2p) board design used to derive this data was a 3-inch x 3-inch (7,5-cm x 7,5-cm), multilayer board with 1 ounce internal power and ground planes and 2 ounce copper traces on top and bottom of the board.
(2) The JEDEC low K (1s) board design used to derive this data was a 3-inch x 3-inch (7,5-cm x 7,5-cm), two-layer board with 2 ounce copper traces on top of the board.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range EN = V_I, T_J = -40 to 125 °C, $V_I = V_{O(typ)}$ + 1 V, I_O= 1 mA, C_o = 10 µF, $C_{(byp)}$ = 0.01 µF (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_I Input voltage (see Note 4)		2.7		5.5	V
I_O Continuous output current (see Note 5)		0		1	A
T_J Operating junction temperature		40		125	°C

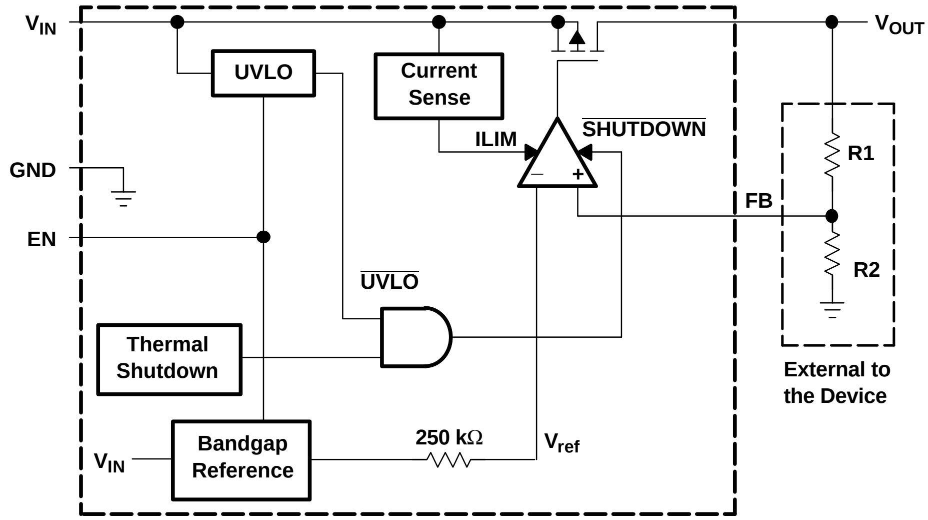
ELECTRICAL CHARACTERISTICS (continued)

over recommended operating free-air temperature range EN = V_I, T_J = -40 to 125 °C, $V_I = V_{O(typ)}$ + 1 V, I_O= 1 mA, C_o = 10 μF, $C_{(byp)}$ = 0.01 μF (unless otherwise noted)

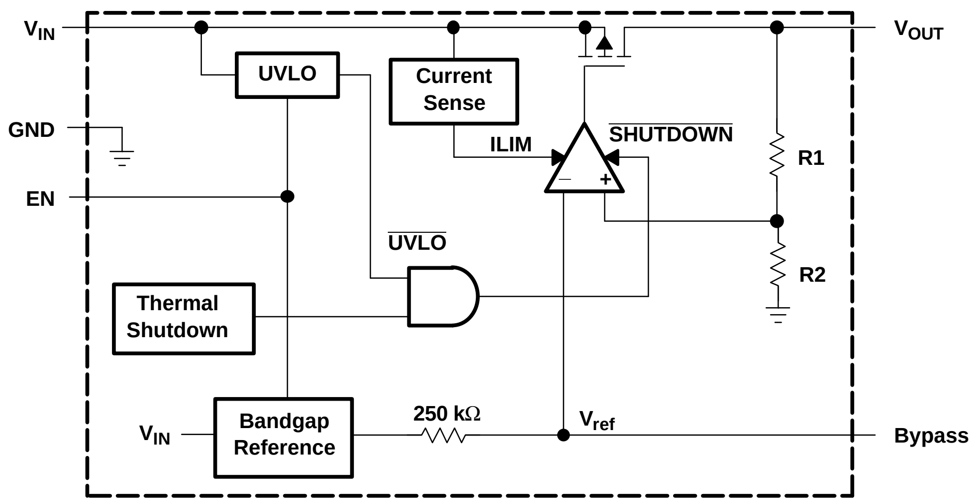
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output voltage	TPS79601	T_J = 25°C			V_O		V
		0 μA< I_O < 1 A,(see Note 6)	1.22 V ≤ V_O≤ 5.5 V,	0.98 V_O		1.02 V_O	
	TPS79618	T_J = 25°C			1.8		V
		0 μA< I_O < 1 A,	2.8 V < V_I < 5.5 V	1.764		1.831	
	TPS79625	T_J = 25°C			2.5		V
		0 μA< I_O < 1 A,	3.5 V < V_I < 5.5 V	2.45		2.55	
	TPS79628	T_J = 25°C			2.8		
		0 μA< I_O < 1 A,	3.8 V < V_I < 5.5 V	2.744		2.856	
	TPS79630	T_J = 25°C			3		
		0 μA< I_O < 1 A,	4 V < V_I < 5.5 V	2.94		3.06	
	TPS79633	T_J = 25°C			3.3		
		0 μA< I_O < 1 A,	4.3 V < V_I < 5.5 V	3.234		3.366	
Quiescent current (GND current)		0 μA< I_O < 1 A,	T_J = 25°C		265		μA
		0 μA< I_O < 1 A				385	
Load regulation		0 μA< I_O < 1 A,	T_J = 25°C		5		mV
Output voltage line regulation ($\Delta V_O/V_O$) (see Note 7)		V_O + 1 V < V_I≤ 5.5 V,	T_J = 25°C		0.05		%/V
		V_O + 1 V < V_I≤ 5.5 V,				0.12	
Output noise voltage (TPS79630)		BW = 100 Hz to 100 kHz,I_O = 1 A, T_J = 25°C	$C_{(byp)}$ = 0.001 μF		54		μV_{RMS}
			$C_{(byp)}$ = 0.0047 μF		46		
			$C_{(byp)}$ = 0.01 μF		41		
			$C_{(byp)}$ = 0.1 μF		40		
Time, start-up (TPS79630)		R_L = 3 Ω, C_o=1 μF, T_J = 25°C	$C_{(byp)}$ = 0.001 μF		50		μs
			$C_{(byp)}$ = 0.0047 μF		75		
			$C_{(byp)}$ = 0.01 μF		110		
Output current limit		V_O =0 V,	See Note 6	2.4		3.5	A
Standby current		EN = 0 V, 2.7 V < V_I < 5.5 V			0.07	1	μA
High level enable input voltage		2.7 V < V_I < 5.5 V		2			V
Low level enable input voltage		2.7 V < V_I < 5.5 V				0.7	V
Input current (EN)		EN = 0		1		1	μA
Input current (FB)		FB = 1.8 V				1	μA
Power supply ripple rejection	TPS79630	f = 100 Hz, T_J = 25°C,	I_O = 10 mA		59		dB
		f = 100 Hz, T_J = 25°C,	I_O = 1 A		54		
		f = 10 kHz, T_J = 25°C,	I_O = 1 A		53		
		f = 100 kHz, T_J = 25°C,	I_O = 1 A		42		
Dropout voltage (see Note (1))	TPS79628	I_O = 1 A,	T_J = 25°C		270		mV
		I_O = 1 A				365	
	TPS79630	I_O = 1 A,	T_J = 25°C		250		
		I_O = 1 A				345	
	TPS79633	I_O = 1 A,	T_J = 25°C		220		
		I_O = 1 A				325	

(1) V_{IN} voltage equals V_O(typ) - 100 mV; The TPS79625 and TPS79618 dropout voltage is limited by the input voltage range limitations.

FUNCTIONAL BLOCK DIAGRAM—ADJUSTABLE VERSION



FUNCTIONAL BLOCK DIAGRAM—FIXED VERSION



Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	ADJ	FIXED		
BYPASS	NA	5		An external bypass capacitor, connected to this terminal, in conjunction with an internal resistor, creates a low-pass filter to further reduce regulator noise.
EN	1	1	I	The EN terminal is an input which enables or shuts down the device. When EN goes to a logic high, the device will be enabled. When the device goes to a logic low, the device is in shutdown mode.
FB	5	N/A	I	This terminal is the feedback input voltage for the adjustable device.
GND	3	3		Regulator ground
V_{IN}	2	2	I	The V_{IN} terminal is the input to the device.
V_{OUT}	4	4	O	The V_{OUT} terminal is the regulated output of the device.

TYPICAL CHARACTERISTICS

**TPS79630
OUTPUT VOLTAGE
vs
OUTPUT CURRENT**

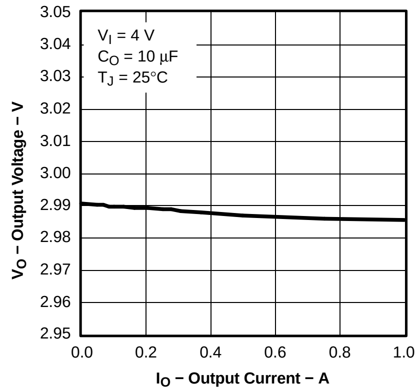


Figure 1.

**TPS79628
OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE**

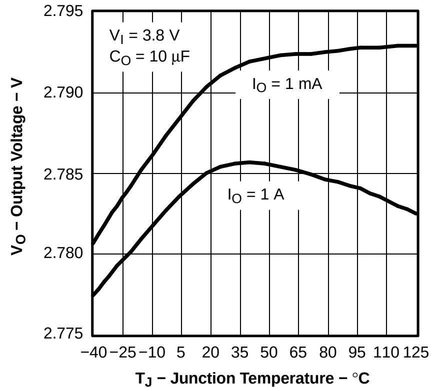


Figure 2.

**TPS79628
GROUND CURRENT
vs
JUNCTION TEMPERATURE**

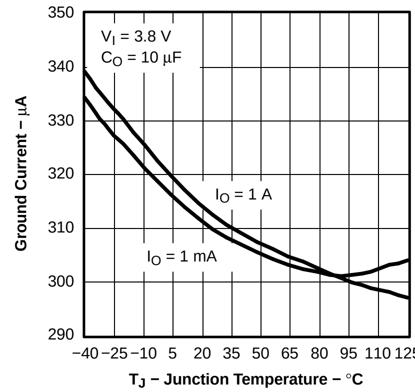


Figure 3.

**TPS79630
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY**

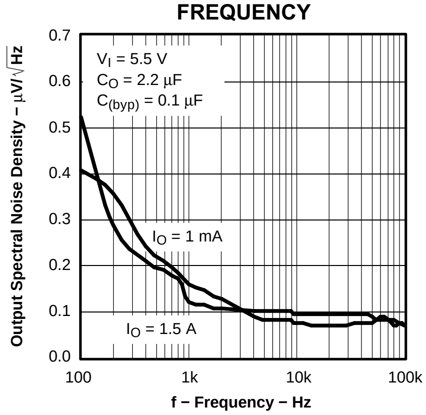


Figure 4.

**TPS79630
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY**

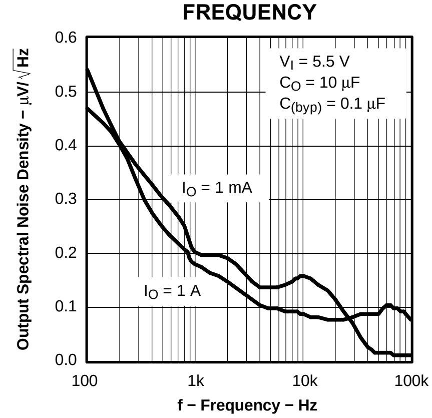


Figure 5.

**TPS79630
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY**

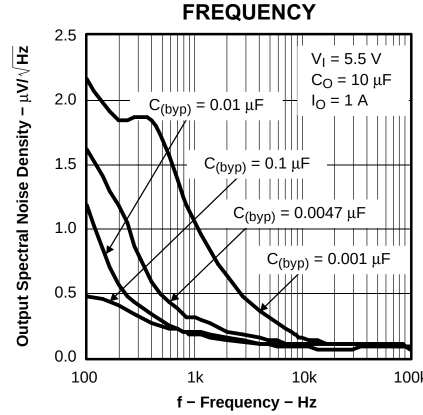


Figure 6.

**TPS79630
ROOT MEAN SQUARED OUTPUT
NOISE
vs
BYPASS CAPACITANCE**

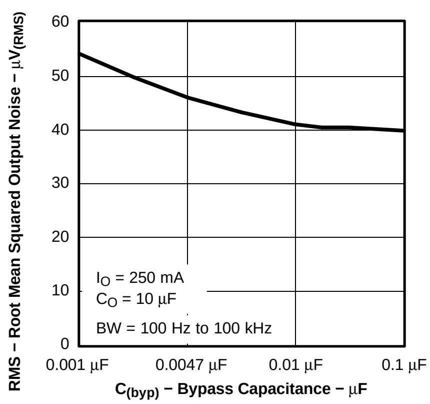


Figure 7.

**TPS79628
DROPOUT VOLTAGE
vs
JUNCTION TEMPERATURE**

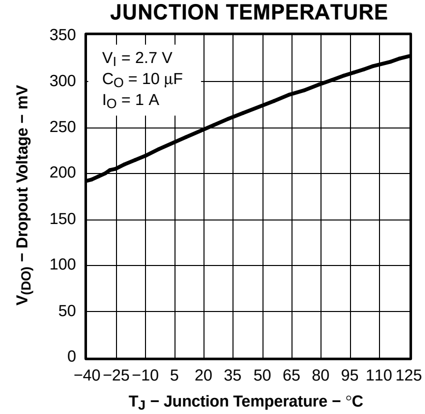


Figure 8.

**TPS79630
RIPPLE REJECTION
vs
FREQUENCY**

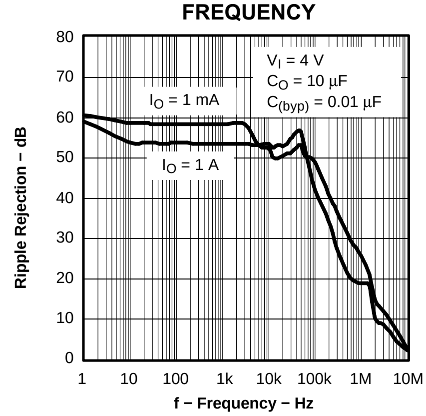


Figure 9.

TYPICAL CHARACTERISTICS (continued)

TPS79630
RIPPLE REJECTION
vs
FREQUENCY

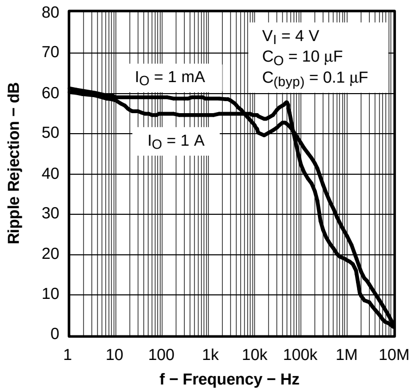


Figure 10.

TPS79630
RIPPLE REJECTION
vs
FREQUENCY

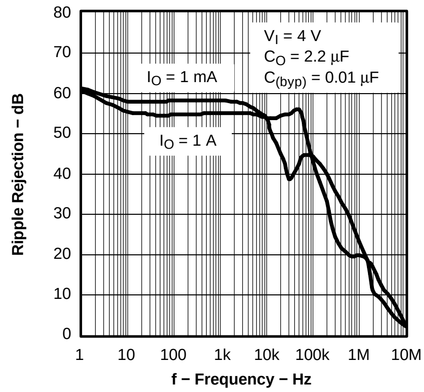


Figure 11.

START-UP TIME

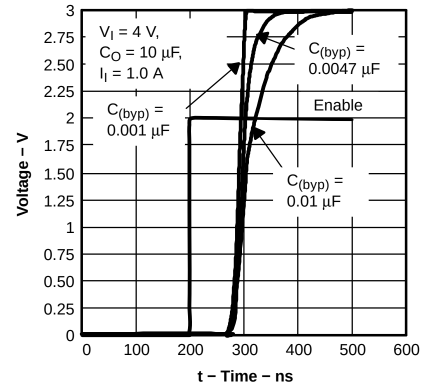


Figure 12.

TPS79618
LINE TRANSIENT RESPONSE

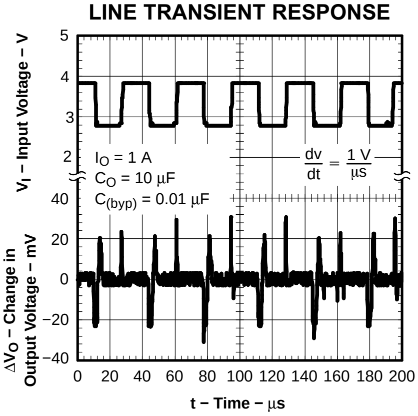


Figure 13.

TPS79630
LINE TRANSIENT RESPONSE

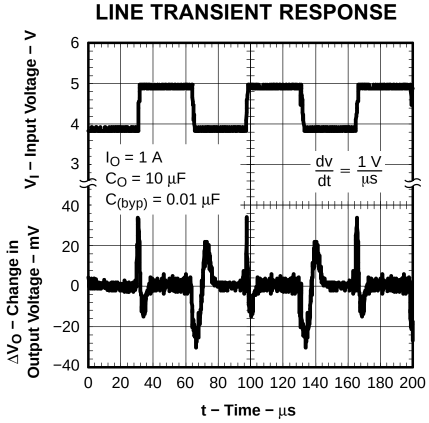


Figure 14.

TPS79628
LOAD TRANSIENT RESPONSE

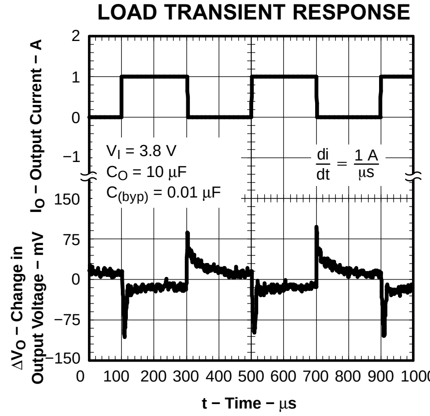


Figure 15.

TPS79625
POWER UP/POWER DOWN

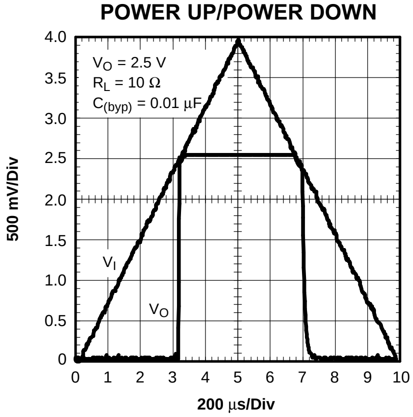


Figure 16.

TPS79630
DC DROPOUT VOLTAGE
vs
OUTPUT CURRENT

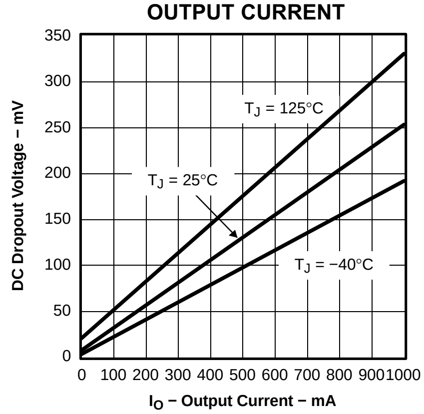


Figure 17.

TPS79601
DROPOUT VOLTAGE
vs
INPUT VOLTAGE

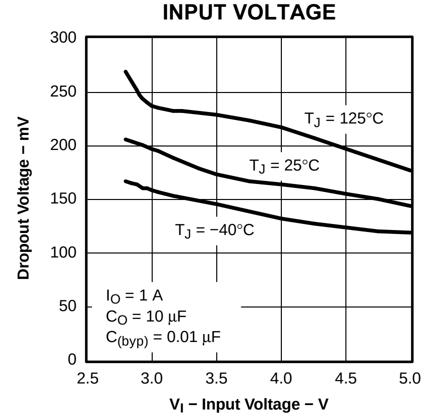


Figure 18.

TYPICAL CHARACTERISTICS (continued)

MINIMUM REQUIRED INPUT VOLTAGE vs OUTPUT VOLTAGE

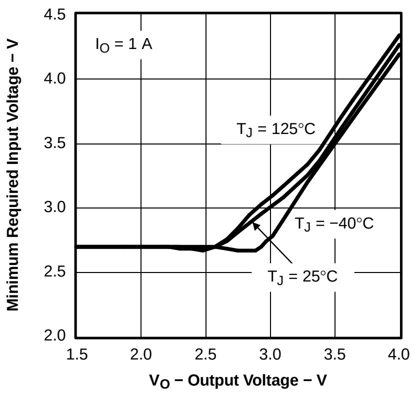


Figure 19.

TPS79630 TYPICAL REGIONS OF STABILITY EQUIVALENT SERIES RESISTANCE (ESR) vs OUTPUT CURRENT

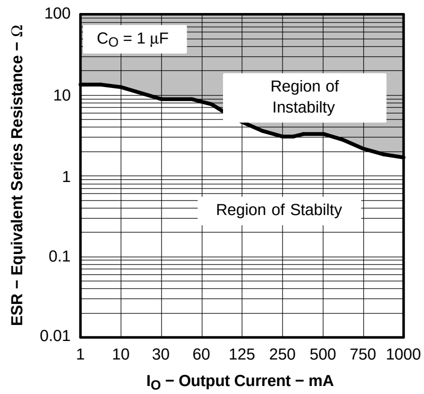


Figure 20.

TPS79630 TYPICAL REGIONS OF STABILITY EQUIVALENT SERIES RESISTANCE (ESR) vs OUTPUT CURRENT

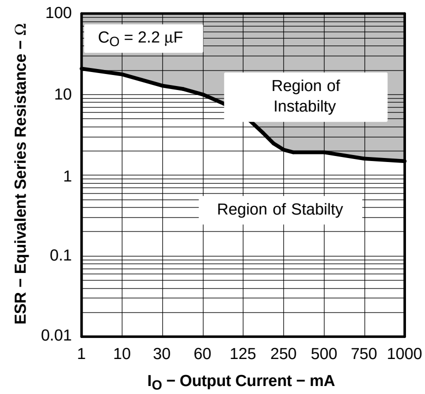


Figure 21.

TPS79630 TYPICAL REGIONS OF STABILITY EQUIVALENT SERIES RESISTANCE (ESR) vs OUTPUT CURRENT

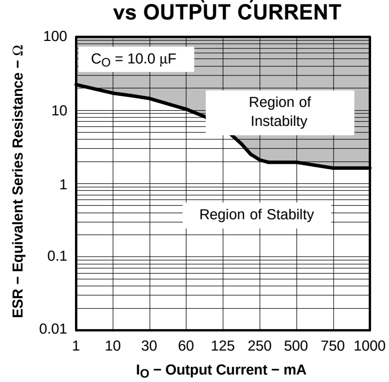


Figure 22.

APPLICATION INFORMATION

The TPS796xx family of low-dropout (LDO) regulators has been optimized for use in noise-sensitive battery-operated equipment. The device features extremely low dropout voltages, high PSRR, ultralow output noise, low quiescent current (265 μA typically), and enable input to reduce supply currents to less than 1 μA when the regulator is turned off.

A typical application circuit is shown in Figure 23.

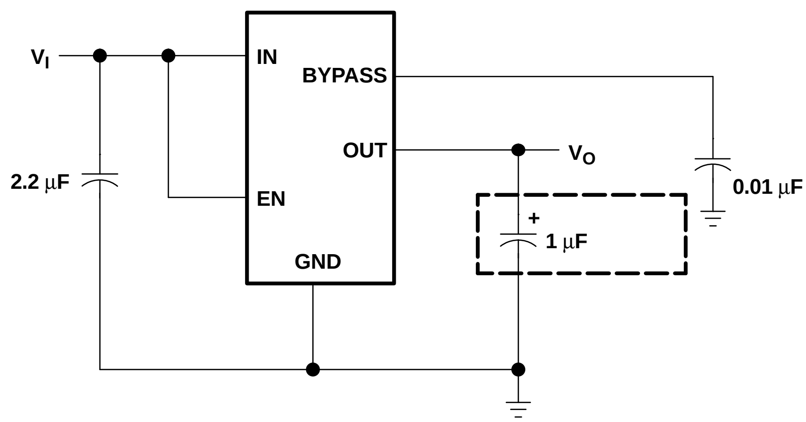


Figure 23. Typical Application Circuit

External Capacitor Requirements

A 2.2-μF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS796xx, is required for stability and improves transient response, noise rejection, and ripple rejection. A higher-value electrolytic input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

Like all low dropout regulators, the TPS796xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 1 μF. Any 1 μF or larger ceramic capacitor is suitable.

The internal voltage reference is a key source of noise in an LDO regulator. The TPS796xx has a BYPASS pin which is connected to the voltage reference through a 250-kΩ internal resistor. The 250-kΩ internal resistor, in conjunction with an external bypass capacitor connected to the BYPASS pin, creates a low pass filter to reduce the voltage reference noise and, therefore, the noise at the regulator output. In order for the regulator to operate properly, the current flow out of the BYPASS pin must be at a minimum, because any leakage current creates an IR drop across the internal resistor thus creating an output error. Therefore, the bypass capacitor must have minimal leakage current.

For example, the TPS79630 exhibits 40 μV_{RMS} of output voltage noise using a 0.1-μF ceramic bypass capacitor and a 10-μF ceramic output capacitor. Note that the output starts up slower as the bypass capacitance increases due to the RC time constant at the bypass pin that is created by the internal 250-kΩ resistor and external capacitor.

Board Layout Recommendation to Improve PSRR and Noise Performance

To improve ac measurements like PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the ground pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the ground pin of the device.

APPLICATION INFORMATION (continued)

Regulator Mounting

The tab of the SOT223-5 package is electrically connected to ground. For best thermal performance, the tab of the surface-mount version should be soldered directly to a circuit-board copper area. Increasing the copper area improves heat dissipation.

Although the tab of the SOT223-5 is electrically grounded, it is not intended to carry any current. The copper pad that acts as a heat sink should be isolated from the rest of the circuit to prevent current flow through the device from the tab to the ground pin. Solder pad footprint recommendations for the devices are presented in an application bulletin *Solder Pad Recommendations for Surface-Mount Devices*, literature number AB-132, available from the TI web site (www.ti.com).

Programming the TPS79601 Adjustable LDO Regulator

The output voltage of the TPS79601 adjustable regulator is programmed using an external resistor divider as shown in Figure 29. The output voltage is calculated using:

$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right)$$

where
V_{ref} = 1.2246 V typ (the internal reference voltage)

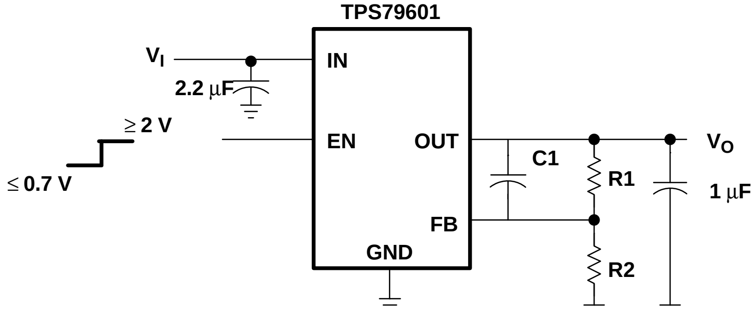
Resistors R1 and R2 should be chosen for approximately 40-μA divider current. Lower value resistors can be used for improved noise performance, but the device wastes more power. Higher values should be avoided, as leakage current at FB increases the output voltage error. The recommended design procedure is to choose R2 = 30.1 kΩ to set the divider current at 40 μA, C1 = 15 pF for stability, and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2$$

In order to improve the stability of the adjustable version, it is suggested that a small compensation capacitor be placed between OUT and FB. The approximate value of this capacitor can be calculated as:

$$C1 = \frac{(3 \times 10^{-7}) \times (R1 + R2)}{(R1 \times R2)}$$

The suggested value of this capacitor for several resistor ratios is shown in the table below. If this capacitor is not used (such as in a unity-gain configuration) then the minimum recommended output capacitor is 2.2 μF instead of 1 μF.



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	C1
1.8 V	14.0 kΩ	30.1 kΩ	33 pF
3.6 V	57.9 kΩ	30.1 kΩ	15 pF

Figure 24. TPS79601 Adjustable LDO Regulator Programming

APPLICATION INFORMATION (continued)

Regulator Protection

The TPS796xx PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS796xx features internal current limiting and thermal protection. During normal operation, the TPS796xx limits output current to approximately 2.8 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds approximately 165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below approximately 140°C, regulator operation resumes.

THERMAL INFORMATION

The amount of heat that an LDO linear regulator generates is directly proportional to the amount of power it dissipates during operation. All integrated circuits have a maximum allowable junction temperature ($T_J$max) above which normal operation is not assured. A system designer must design the operating environment so that the operating junction temperature (T_J) does not exceed the maximum junction temperature ($T_J$max). The two main environmental variables that a designer can use to improve thermal performance are air flow and external heatsinks. The purpose of this information is to aid the designer in determining the proper operating environment for a linear regulator that is operating at a specific power level.

In general, the maximum expected power ($P_{D(max)}$) consumed by a linear regulator is computed as:

$$P_D max = \left(V_{I(avg)} - V_{O(avg)}\right) \times I_{O(avg)} + V_{I(avg)} \times I_{(Q)} \qquad (3)$$

where:

- $V_{I(avg)}$ is the average input voltage.
- $V_{O(avg)}$ is the average output voltage.
- $I_{O(avg)}$ is the average output current.
- $I_{(Q)}$ is the quiescent current.

For most TI LDO regulators, the quiescent current is insignificant compared to the average output current; therefore, the term $V_{I(avg)}$ x $I_{(Q)}$ can be neglected. The operating junction temperature is computed by adding the ambient temperature (T_A) and the increase in temperature due to the regulator's power dissipation. The temperature rise is computed by multiplying the maximum expected power dissipation by the sum of the thermal resistances between the junction and the case ($R_{\Theta JC}$), the case to heatsink ($R_{\Theta CS}$), and the heatsink to ambient ($R_{\Theta SA}$). Thermal resistances are measures of how effectively an object dissipates heat. Typically, the larger the device, the more surface area available for power dissipation and the lower the object's thermal resistance.

Figure 25 illustrates these thermal resistances for (a) a SOT223 package mounted in a JEDEC low-K board, and (b) a DDPAK package mounted on a JEDEC high-K board.

THERMAL INFORMATION (continued)

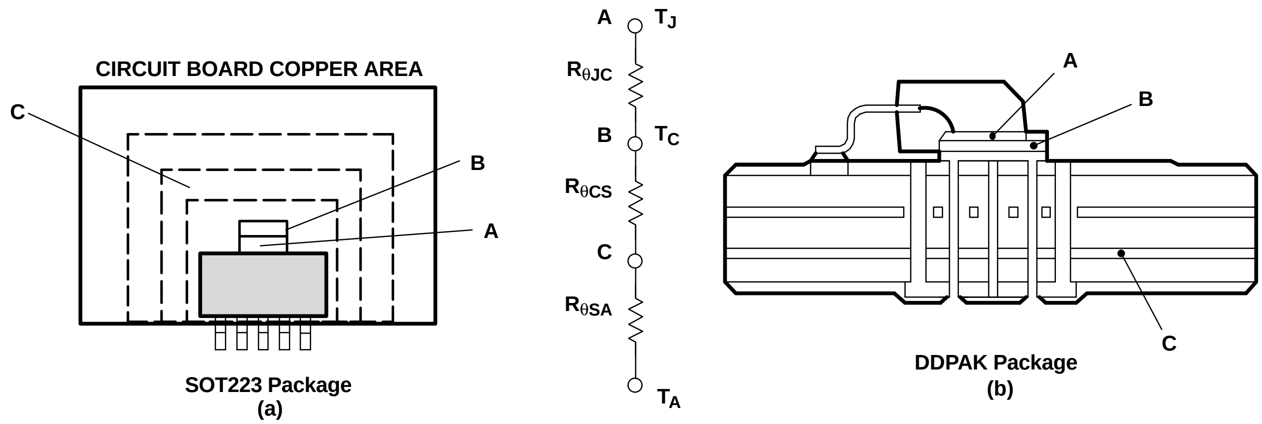


Figure 25. Thermal Resistances

Equation 4 summarizes the computation:

$$T_J = T_A + P_D max \times \left(R_{\theta JC} + R_{\theta CS} + R_{\theta SA}\right) \tag{4}$$

The $R_{\Theta JC}$ is specific to each regulator as determined by its package, lead frame, and die size provided in the regulator's data sheet. The $R_{\Theta SA}$ is a function of the type and size of heatsink. For example, *black body radiator* type heatsinks can have $R_{\Theta CS}$ values ranging from 5°C/W for very large heatsinks to 50°C/W for very small heatsinks. The $R_{\Theta CS}$ is a function of how the package is attached to the heatsink. For example, if a thermal compound is used to attach a heatsink to a SOT223 package, $R_{\Theta CS}$of 1°C/W is reasonable.

Even if no external *black body radiator* type heatsink is attached to the package, the board on which the regulator is mounted provides some heatsinking through the pin solder connections. Some packages, like the DDPAK and SOT223 packages, use a copper plane underneath the package or the circuit board's ground plane for additional heatsinking to improve their thermal performance. Computer aided thermal modeling can be used to compute very accurate approximations of an integrated circuit's thermal performance in different operating environments (e.g., different types of circuit boards, different types and sizes of heatsinks, and different air flows, etc.). Using these models, the three thermal resistances can be combined into one thermal resistance between junction and ambient ($R_{\Theta JA}$). This $R_{\Theta JA}$is valid only for the specific operating environment used in the computer model.

Equation 4 simplifies into equation 5:

$$T_J = T_A + P_D max \times R_{\theta JA} \tag{5}$$

Rearranging equation 5 gives equation 6:

$$R_{\theta JA} = \frac{T_J - T_A}{P_D max} \tag{6}$$

Using equation 5 and the computer model generated curves shown in Figure 26 and Figure 29, a designer can quickly compute the required heatsink thermal resistance/board area for a given ambient temperature, power dissipation, and operating environment.

DDPAK Power Dissipation

The DDPAK package provides an effective means of managing power dissipation in surface mount applications. The DDPAK package dimensions are provided in the *Mechanical Data* section at the end of the data sheet. The addition of a copper plane directly underneath the DDPAK package enhances the thermal performance of the package.

THERMAL INFORMATION (continued)

To illustrate, the TPS72525 in a DDPAK package was chosen. For this example, the average input voltage is 5 V, the output voltage is 2.5 V, the average output current is 1 A, the ambient temperature 55°C, the air flow is 150 LFM, and the operating environment is the same as documented below. Neglecting the quiescent current, the maximum average power is:

$$P_D max = (5 - 2.5)\,V \times 1\,A = 2.5\,W \quad (7)$$

Substituting $T_J$max for T_J into equation 6 gives equation 8:

$$R_{\theta JA} max = (125 - 55)°C/2.5\,W = 28°C/W \quad (8)$$

From Figure 26, DDPAK Thermal Resistance vs Copper Heatsink Area, the ground plane needs to be 1 cm^2 for the part to dissipate 2.5 W. The operating environment used in the computer model to construct Figure 26 consisted of a standard JEDEC High-K board (2S2P) with a 1 oz. internal copper plane and ground plane. The package is soldered to a 2 oz. copper pad. The pad is tied through thermal vias to the 1 oz. ground plane. Figure 27 shows the side view of the operating environment used in the computer model.

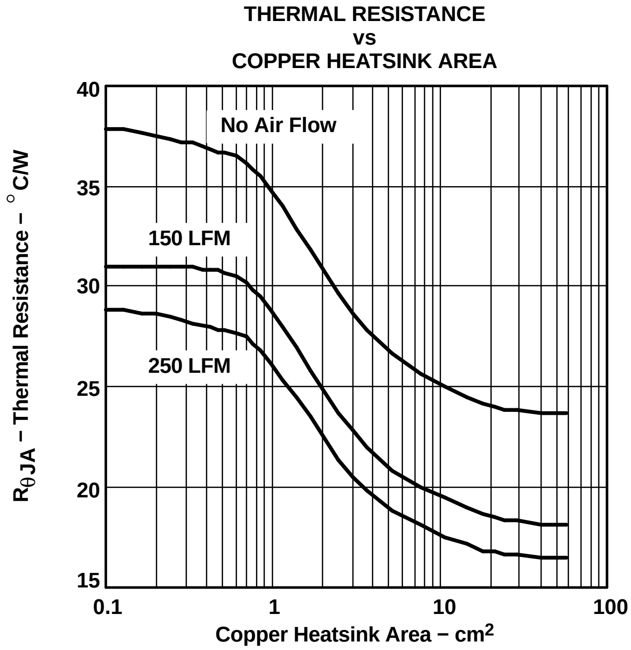


Figure 26. DDPAK Thermal Resistance vs Copper Heatsink Area

THERMAL INFORMATION (continued)

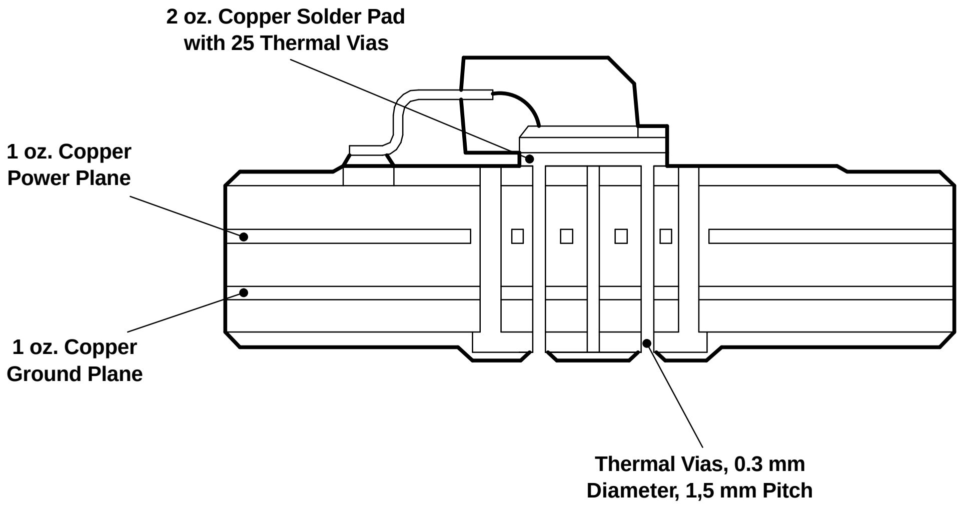


Figure 27. DDPAK Thermal Resistance

From the data in Figure 28 and rearranging equation 6, the maximum power dissipation for a different ground plane area and a specific ambient temperature can be computed.

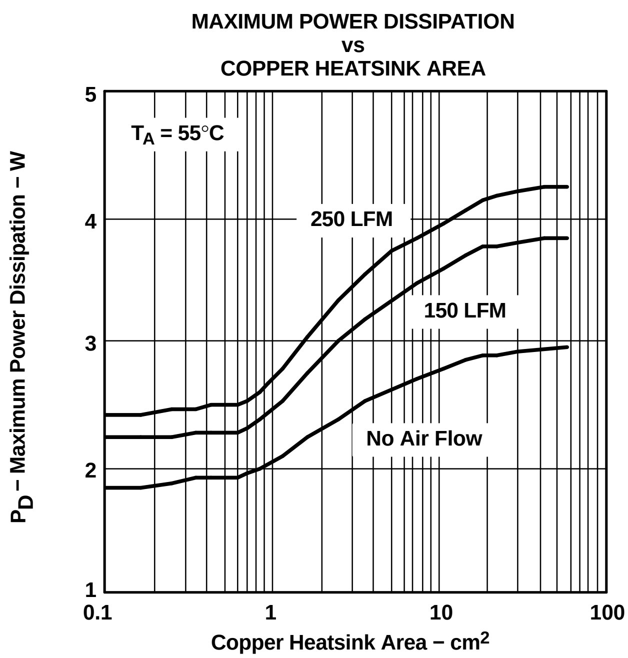


Figure 28. Maximum Power Dissipation vs Copper Heatsink Area

SOT223 Power Dissipation

The SOT223 package provides an effective means of managing power dissipation in surface mount applications. The SOT223 package dimensions are provided in the *Mechanical Data* section at the end of the data sheet. The addition of a copper plane directly underneath the SOT223 package enhances the thermal performance of the package.

THERMAL INFORMATION (continued)

To illustrate, the TPS72525 in a SOT223 package was chosen. For this example, the average input voltage is 3.3 V, the output voltage is 2.5 V, the average output current is 1 A, the ambient temperature 55°C, no air flow is present, and the operating environment is the same as documented below. Neglecting the quiescent current, the maximum average power is:

$$P_D max \ = \ (3.3 \ - \ 2.5)\ V \times 1\ A \ = \ 800\ mW \qquad (9)$$

Substituting $T_J$max for T_J into equation 6 gives equation 10:

$$R_{\theta JA} max \ = \ (125 \ - \ 55)°C/800\ mW \ = \ 87.5°C/W \qquad (10)$$

From Figure 29, $R_{\Theta JA}$ vs PCB Copper Area, the ground plane needs to be 0.55 in^2 for the part to dissipate 800 mW. The operating environment used to construct Figure 29 consisted of a board with 1 oz. copper planes. The package is soldered to a 1 oz. copper pad on the top of the board. The pad is tied through thermal vias to the 1 oz. ground plane.

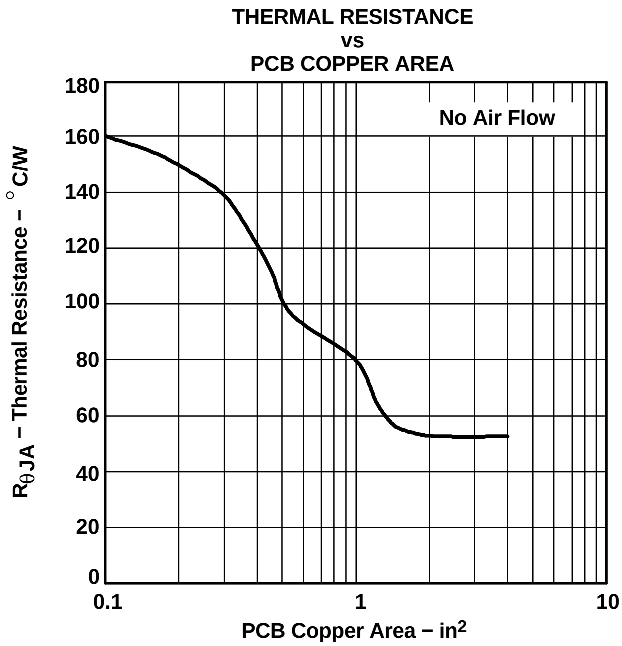


Figure 29. SOT223 Thermal Resistance vs PCB AREA

From the data in Figure 29 and rearranging equation 6, the maximum power dissipation for a different ground plane area and a specific ambient temperature can be computed (see Figure 30).

THERMAL INFORMATION (continued)

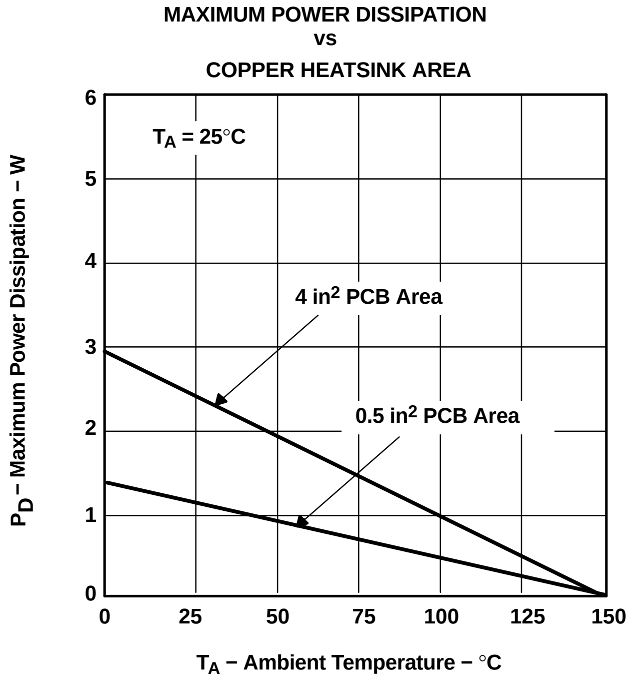


Figure 30. SOT223 Power Dissipation

IMPORTANT NOTICE

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