Wireless Components

ASK Single Conversion Receiver

TDA 5201 Version 1.4

Specification March 2000

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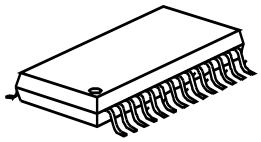
Product Info

General Description

The IC is a very low power consumption single chip ASK Single Conversion Receiver for receive frequencies between 310 and 345MHz. The Receiver offers a high level of integration and needs only a few external components. The device contains a low noise amplifier (LNA), a double balanced mixer, a fully integrated VCO, a PLL synthesiser, a crystal oscillator, a limiter with RSSI generator, a data filter, a data comparator (slicer) and a peak detector. Additionally there is a power down feature to save battery life.

Package



Features

- Low supply current (I_s = 4.6mA typ.)
- Supply voltage range 5V ±10%
- Power down mode with very low supply current (50nA typ)
- Fully integrated VCO and PLL Synthesiser
- RF input sensitivity < –110dBm
- Selectable frequency ranges 308-312 MHz and 343-347 MHz
- Selectable reference frequency
- Limiter with RSSI generation, operating at 10.7MHz
- 2nd order low pass data filter with external capacitors
- Data slicer with self-adjusting threshold

Application

- Keyless Entry Systems
- Remote Control Systems
- Fire Alarm Systems
- Low Bitrate Communication Systems

Ordering Information

Type	Ordering Code	Package
TDA 5201	Q67037-A1118	P-TSSOP-28-1
available on tape and reel		

1 Table of Contents

2 Product Description

Contents of this Chapter

2.1 Overview

The IC is a very low power consumption single chip ASK Superheterodyne Receiver (SHR) for the frequency bands 315 and 345MHz. The SHR offers a high level of integration and needs only a few external components. The device contains a low noise amplifier (LNA), a double balanced mixer, a fully integrated VCO, a PLL synthesiser, a crystal oscillator, a limiter with RSSI generator, a data filter, a data comparator (slicer) and a peak detector. Additionally there is a power down feature to save battery life.

2.2 Application

- Keyless Entry Systems
- Remote Control Systems
- Fire Alarm Systems
- Low Bitrate Communication Systems

2.3 Features

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- Selectable reference frequency
- Limiter with RSSI generation, operating at 10.7MHz
- 2nd order low pass data filter with external capacitors
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2.4 Package Outlines

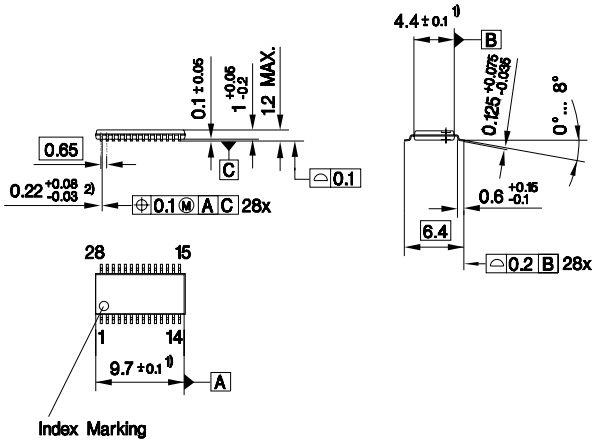
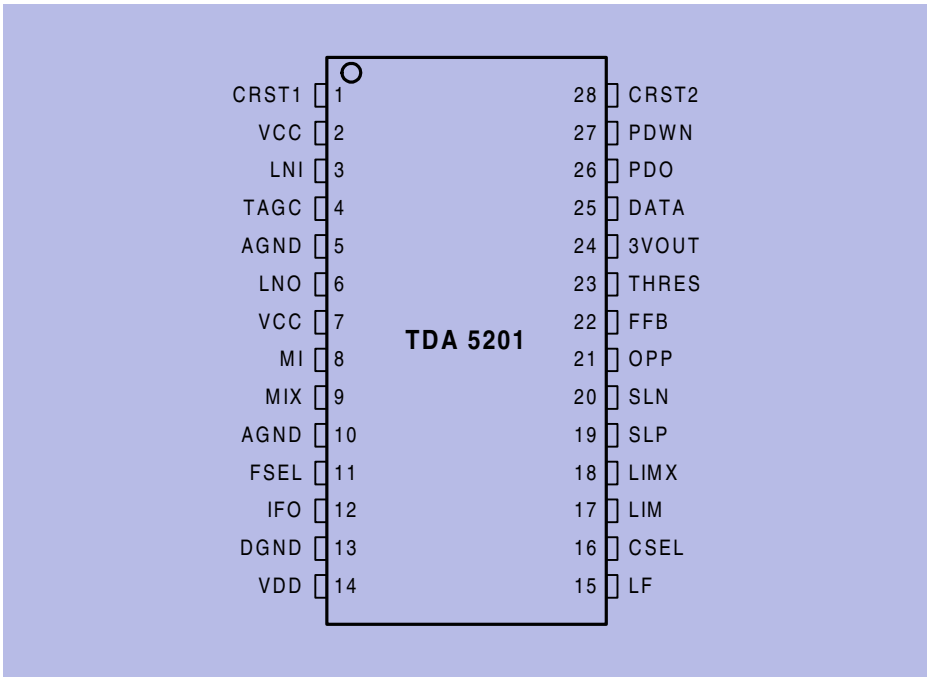


Figure 2-1 P-TSSOP-28-1 package outlines

3 Functional Description

Contents of this Chapter

3.1 Pin Configuration

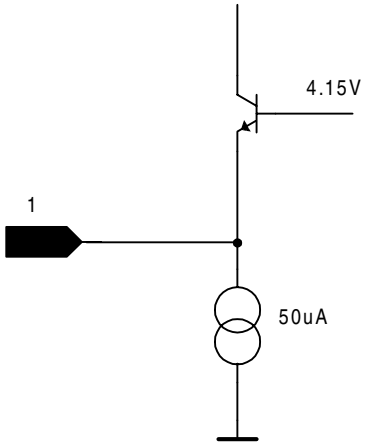
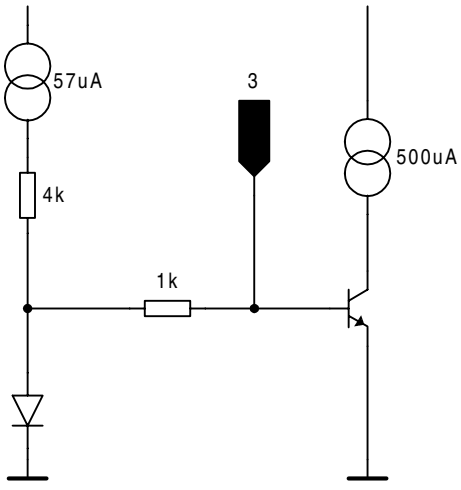


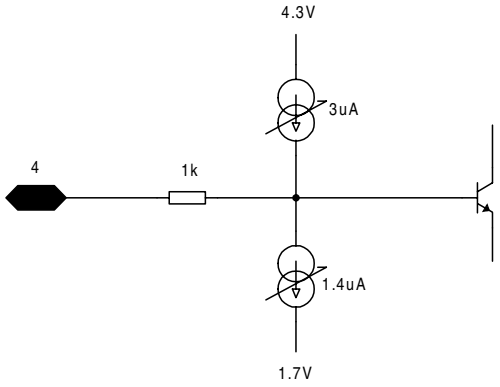
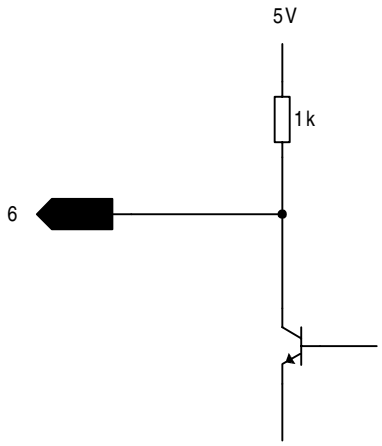
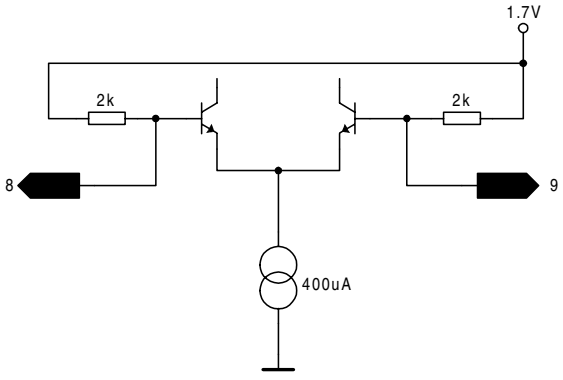
Pin_Configuration_5201_V1.4.wmf

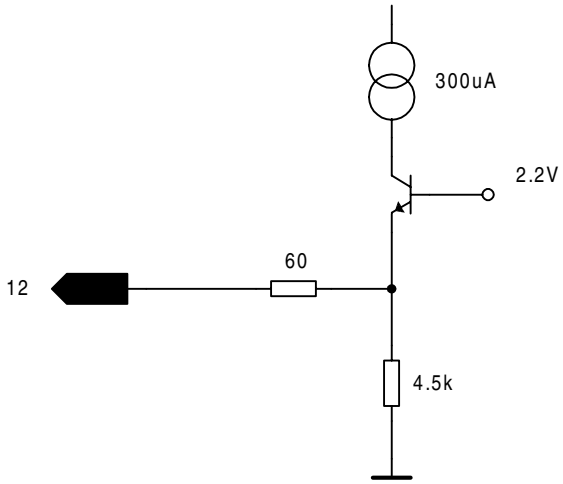
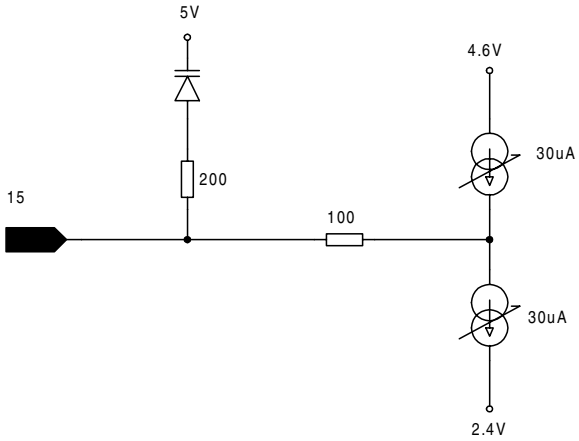
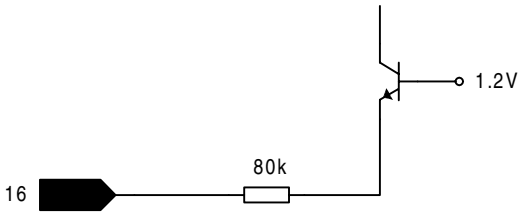
Figure 3-1 IC Pin Configuration

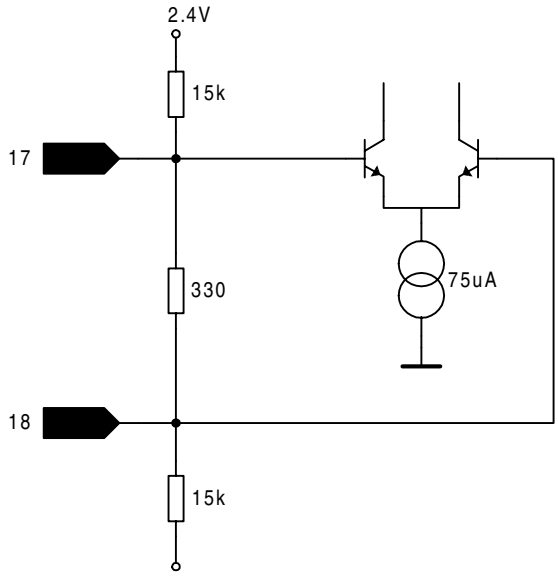
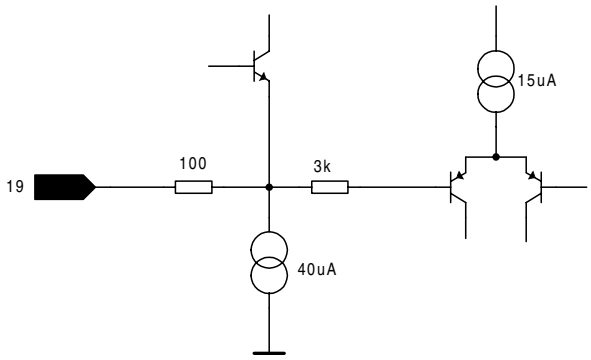
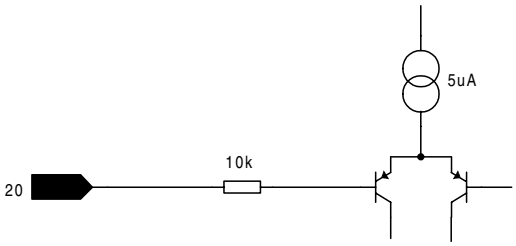
3.2 Pin Definition and Function

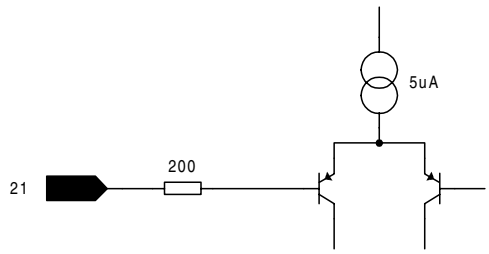
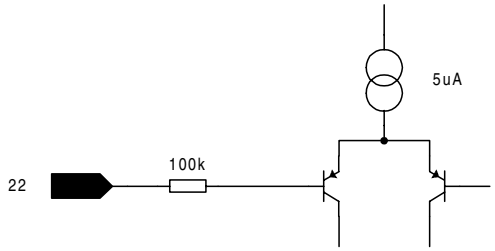
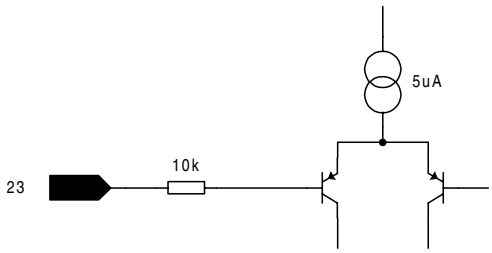
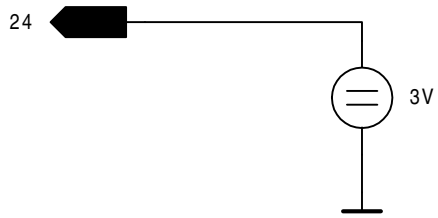
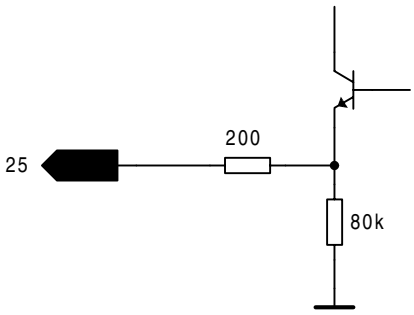
Table 3-1 Pin Definition and Function

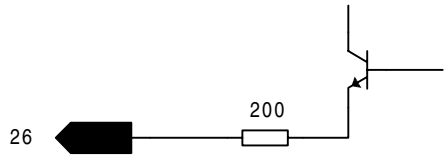
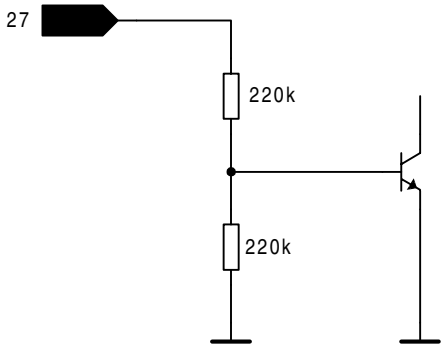
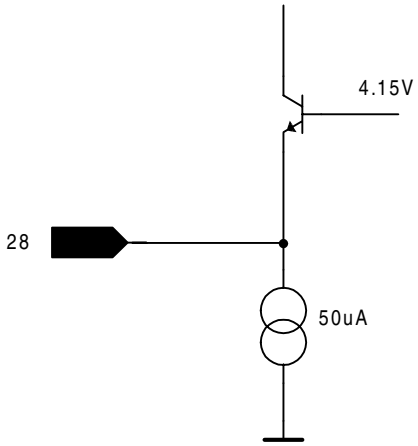
Pin No.	Symbol	Equivalent I/O-Schematic	Function
1	CRST1		External Crystal Connector 1
2	VCC		5V Supply
3	LNI		LNA Input

4	TAGC		AGC Time Constant Control
5	AGND		Analogue Ground Return
6	LNO		LNA Output
7	VCC		5V Supply
8	MI		Mixer Input
9	MIX		Complementary Mixer Input
10	AGND		Analogue Ground Return
11	FSEL		not applicable - has to be left open

12	IFO		10.7 MHz IF Mixer Output
13	DGND		Digital Ground Return
14	VDD		5V Supply (PLL Counter Circuitry)
15	LF		PLL Filter Access Point
16	CSEL		5.xx or 10.xx MHz Quartz Selector

17	LIM		Limiter Input
18	LIMX		Complementary Limiter Input
19	SLP		Data Slicer Positive Input
20	SLN		Data Slicer Negative Input

21	OPP		OpAmp Noninverting Input
22	FFB		Data Filter Feedback Pin
23	THRES		AGC Threshold Input
24	3VOUT		3V Reference Output
25	DATA		Data Output

26	PDO		Peak Detector Output
27	PDWN		Power Down Input
28	CRST2		External Crystal Connector 2

3.3 Functional Block Diagram

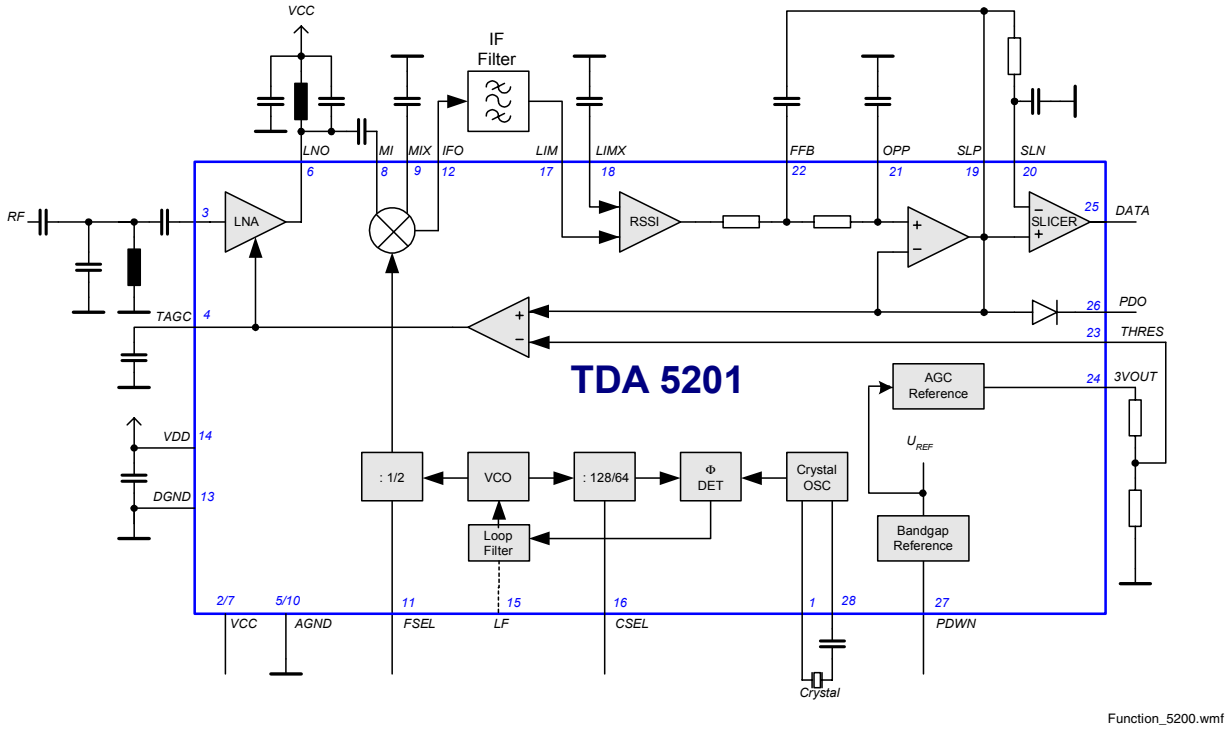


Figure 3-2 Main Block Diagram

3.4 Functional Blocks

3.4.1 Low Noise Amplifier (LNA)

The LNA is an on-chip cascode amplifier with a voltage gain of 15 to 20dB. The gain figure is determined by the external matching networks situated ahead of LNA and between the LNA output **LNO** (Pin 6) and the Mixer Inputs **MI** and **MIX** (Pins 8 and 9). The noise figure of the LNA is approximately 2dB, the current consumption is 500µA. The gain can be reduced by approximately 18dB. The switching point of this AGC action can be determined externally by applying a threshold voltage at the **THRES** pin (Pin 23). This voltage is compared internally with the received signal (RSSI) level generated by the limiter circuitry. In case that the RSSI level is higher than the threshold voltage the LNA gain is reduced and vice versa. The threshold voltage can be generated by attaching a voltage divider between the **3VOUT** pin (Pin 24) which provides a temperature stable 3V output generated from the internal bandgap voltage and the **THRES** pin as described in Section 4.1. The time constant of the AGC action can be determined by connecting a capacitor to the **TAGC** pin (Pin 4) and should be chosen along with the appropriate threshold voltage according to the intended operating case and interference scenario to be expected during operation. The optimum choice of AGC time constant and the threshold voltage is described in Section 4.1.

3.4.2 Mixer

The Double Balanced Mixer downconverts the input frequency (RF) in the range of 310 or 345MHz to the intermediate frequency (IF) at 10.7MHz with a voltage gain of approximately 21dB. A low pass filter with a corner frequency of 20MHz is built on chip in order to suppress RF signals to appear at the IF output (**IFO** pin). The IF output is internally consisting of an emitter follower that has a source impedance of approximately 330 Ω to facilitate interfacing the pin directly to a standard 10.7MHz ceramic filter without additional matching circuitry.

3.4.3 PLL Synthesizer

The Phase Locked Loop synthesiser consists of a VCO, an asynchronous divider chain, a phase detector with charge pump and a loop filter and is fully implemented on-chip. The VCO is including spiral inductors and varactor diodes. It's nominal centre frequency is 660MHz. The FSEL pin (Pin 11) has to be left open. No additional components are necessary. The oscillator signal is fed both to the synthesiser divider chain and to the downconverting mixer. The VCO signal is divided by two before it is fed to the mixer. The loop filter is also realised fully on-chip.

3.4.4 Crystal Oscillator

The on-chip crystal oscillator circuitry allows for utilisation of quartzes both in the 5 and 10MHz range as the overall division ratio of the PLL can be switched between 64 and 128 via the **CSEL** (Pin 16) pin according to the following table.

Table 3-2 CSEL Pin Operating States

CSEL	Crystal Frequency
Open	5.xx MHz
Shorted to ground	10.xx MHz

The calculation of the value of the necessary quartz load capacitance is shown in Section 4.3, the quartz frequency calculation is expained in Section 4.4.

3.4.5 Limiter

The Limiter is an AC coupled multistage amplifier with a cumulative gain of approximately 80dB that has a bandpass-characteristic centred around 10.7MHz. It has an input impedance of 330 Ω to allow for easy interfacing to a 10.7MHz ceramic IF filter. The limiter circuit acts as a Receive Signal Strength Indicator (RSSI) generator which produces a DC voltage that is directly proportional to the input signal level as can be seen in Figure 4-2. This signal is used to demodulate the ASK receive signal in the subsequent baseband circuitry and to turn down the LNA gain by approximately 18dB in case the input signal strength is too strong as described in Section 3.4.1 and Section 4.1.

3.4.6 Data Filter

The data filter comprises an OP-Amp with a bandwidth of 100kHz used as a voltage follower and two 100kΩ on-chip resistors. Along with two external capacitors a 2nd order Sallen-Key low pass filter is formed. The selection of the capacitor values is described in Section 4.2.

3.4.7 Data Slicer

The data slicer is a fast comparator with a bandwidth of 100 kHz. This allows for a maximum receive data rate of approximately 120kBaud. The maximum achievable data rate also depends on the IF Filter bandwidth and the local oscillator tolerance values. Both inputs are accessible. The output delivers a digital data signal (CMOS-like levels) for the detector. The self-adjusting threshold on pin 20 its generated by RC-term or peak detector depending on the baseband coding scheme. The data slicer threshold generation alternatives are described in more detail in Section 4.5.

3.4.8 Peak Detector

The peak detector generates a DC voltage which is proportional to the peak value of the receive data signal. An external RC network is necessary. The output can be used as an indicator for the signal strength and also as a reference for the data slicer. The maximum output current is 500µA.

3.4.9 Bandgap Reference Circuitry

A Bandgap Reference Circuit provides a temperature stable reference voltage for the device. A power down mode is available to switch off all subcircuits which is controlled by the PWDN pin (Pin 27) as shown in the following table. The supply current drawn in this case is typically 50nA.

Table 3-3 PDWN Pin Operating States

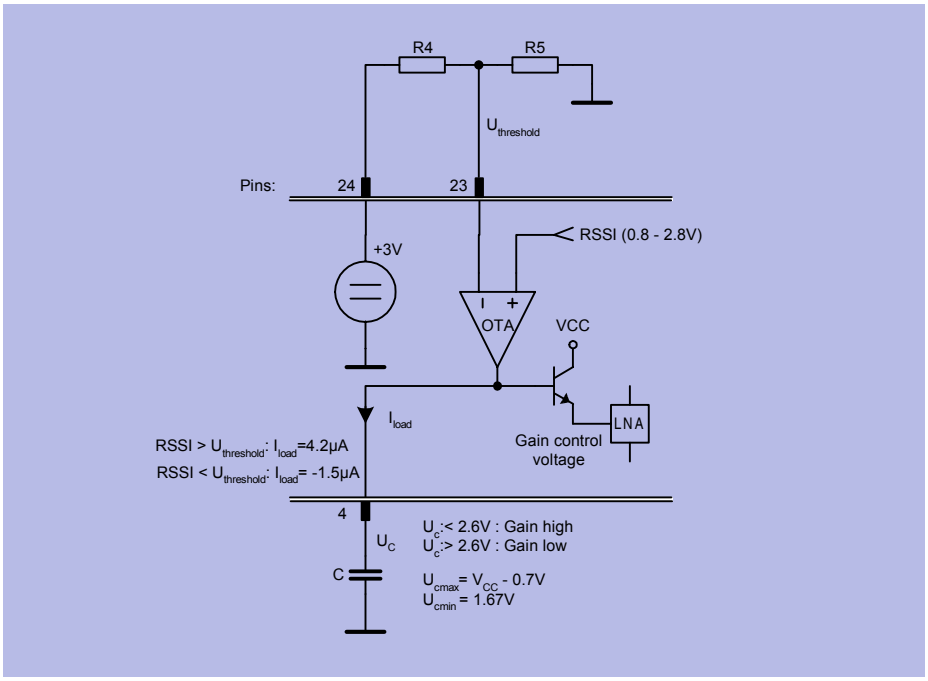
PDWN	Operating State
Open or tied to ground	Powerdown Mode
Tied to Vs	Receiver On

4 Applications

Contents of this Chapter

4.1 Choice of LNA Threshold Voltage and Time Constant

In the following figure the internal circuitry of the LNA automatic gain control is shown.

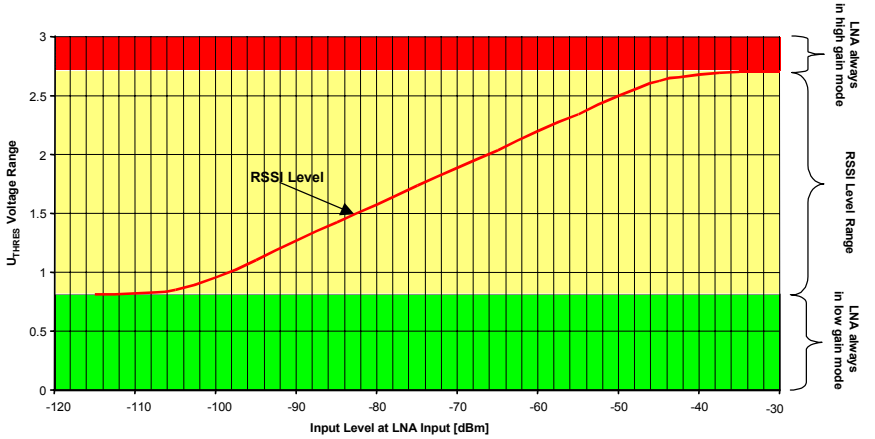


LNA_autom.wmf

Figure 4-1 LNA Automatic Gain Control Circuitry

The LNA automatic gain control circuitry consists of an operational transimpedance amplifier that is used to compare the received signal strength signal (RSSI) generated by the Limiter with an externally provided threshold voltage U_{thres}. As shown in the following figure the threshold voltage can have any value between approximately 0.8 and 2.8V to provide a switching point within the receive signal dynamic range.

This voltage U_{thres} is applied to the **THRES** pin (Pin 23) The threshold voltage can be generated by attaching a voltage divider between the **3VOUT** pin (Pin 24) which provides a temperature stable 3V output generated from the internal bandgap voltage and the **THRES** pin. If the RSSI level generated by the Limiter is higher than U_{thres}, the OTA generates a positive current I_{load}. This yields a voltage rise on the **TAGC** pin (Pin 4). Otherwise, the OTA generates a negative current. These currents do not have the same values in order to achieve a fast-attack and slow-release action of the AGC and are used to charge an external capacitor which finally generates the LNA gain control voltage.



RSSI-AGC.wmf

Figure 4-2 RSSI Level and Permissive AGC Threshold Levels

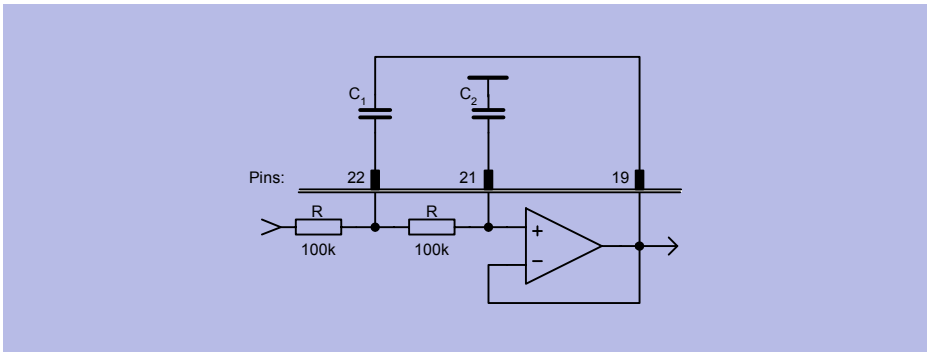
The switching point should be chosen according to the intended operating scenario. The determination of the optimum point is described in the accompanying Application Note, a threshold voltage level of 1.8V is apparently a viable choice. It should be noted that the output of the 3VOUT pin is capable of driving up to 50µA, but that the THRES pin input current is only in the region of 40nA. As the current drawn out of the 3VOUT pin is directly related to the receiver power consumption, the power divider resistors should have high impedance values. R4 can be chosen as 120kΩ, R5 as 180kΩ to yield an overall 3VOUT output current of 10µA.

Note: If the LNA gain shall be kept in either high or low gain mode this has to be accomplished by tying the **THRES** pin to a fixed voltage. In order to achieve high gain mode operation, a voltage higher than 2.8V shall be applied to the **THRES** pin, such as a short to the **3VOLT** pin. In order to achieve low gain mode operation a voltage lower than 0.7V shall be applied to the **THRES**, such as a short to ground.

As stated above the capacitor connected to the **TAGC** pin is generating the gain control voltage of the LNA due to the charging and discharging currents of the OTA and thus is also responsible for the AGC time constant. As the charging and discharging currents are not equal two different time constants will result. The time constant corresponding to the charging process of the capacitor shall be chosen according to the data rate. According to measurements performed at Infineon the capacitor value should be greater than 47nF.

4.2 Data Filter Design

Utilising the on-board voltage follower and the two 100kΩ on-chip resistors a 2nd order Sallen-Key low pass data filter can be constructed by adding 2 external capacitors between pins 19 (SLP) and 22 (FFB) and to pin 21 (OPP) as depicted in the following figure and described in the following formulas[1].



Filter_Design.wmf

Figure 4-3 Data Filter Design

(1) (2)

$$C1 = \frac{2Q\sqrt{b}}{R2\Pi f_{3dB}} \qquad C2 = \frac{\sqrt{b}}{4QR\Pi f_{3dB}}$$

with

$$Q = \frac{\sqrt{b}}{a}$$ (3) the quality factor of the poles

where

in case of a Bessel filter	a = 1.3617, b = 0.618
and thus	Q = 0.577
and in case of a Butterworth filter	a = 1.141, b = 1
and thus	Q = 0.71

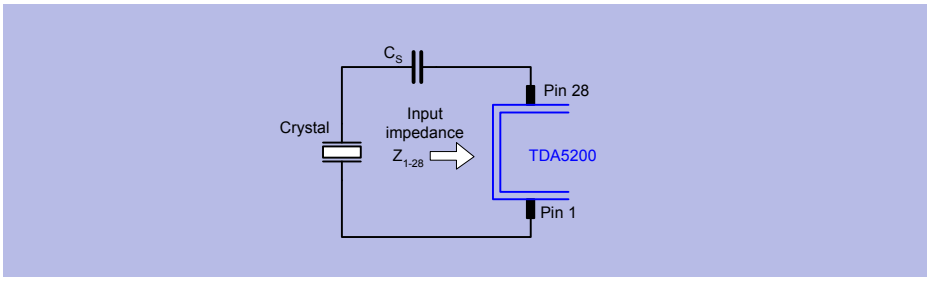
Example: Butterworth filter with f_{3dB} = 5kHz and R = 100kΩ:

C_1 = 450pF, C_2 = 225pF

1. taken from Tietze/Schenk: Halbleiterschaltungstechnik, Springer Berlin, 1999

4.3 Quartz Load Capacitance Calculation

The value of the capacitor necessary to achieve that the quartz oscillator is operating at the intended frequency is determined by the reactive part of the negative resistance of the oscillator circuit as shown in Section 5.1.3 and by the quartz specifications given by the quartz manufacturer.



Quartz_load.wmf

Figure 4-4 Determination of Series Capacitance Value for the Quartz Oscillator

Crystal specified with load capacitance

$$C_S = \frac{1}{\frac{1}{C_l} + 2\pi f X_L}$$

with C_l the load capacitance (refer to the quartz crystal specification).

Examples:

5.1 MHz:	C_L = 12 pF	X_L=580 Ω	C_S = 9.8 pF
10.18 MHz:	C_L = 12 pF	X_L=870 Ω	C_S = 7.2 pF

These values may be obtained by putting two capacitors in series to the quartz, such as 18pF and 22pF in the 5.1MHz case and 18pF and 12pF in the 10.2MHz case.

4.4 Quartz Frequency Calculation

The quartz frequency is calculated by using the following formula:

$f_{QU} = (f_{RF} \pm 10.7) / r$ (1),

with
- f_{RF} .... receive frequency
- f_{LO} .... local oscillator (PLL) frequency ($f_{RF} \pm 10.7$)
- f_{QU} .... quartz oscillator frequency
- r .... ratio of local oscillator (PLL) frequency and quartz frequency as shown in the subsequent table.

Table 4-1 PLL Division Ratio Dependence on States of CSEL

CSEL	Ratio r = (f_{LO}/f_{QU})
open	64
GND	32

Addition of 10.7 is used in case of operation the device at 315 MHz, subtraction in case of operation at 345 MHz. This yields the following frequencies:

CSEL tied to GND:

$$f_{QU} = (315\,MHz + 10.7\,MHz)/32 = 10.1781\,MHz$$

$$f_{QU} = (345\,MHz - 10.7\,MHz)/32 = 10.4469\,MHz$$

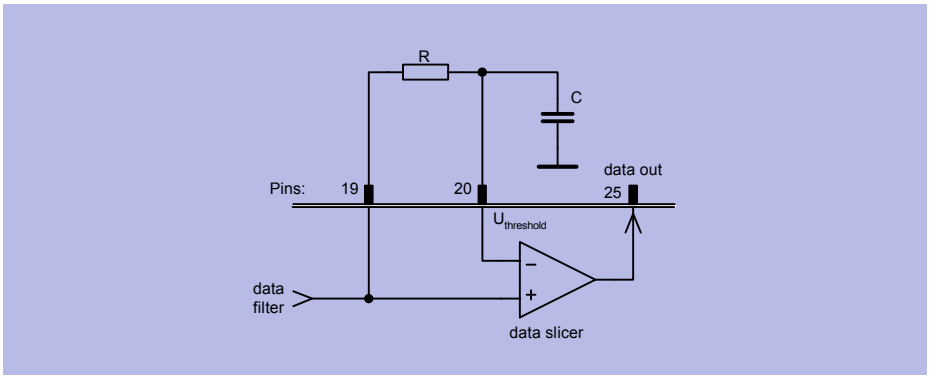
CSEL open:

$$f_{QU} = (315\,MHz + 10.7\,MHz)/64 = 5.0891\,MHz$$

$$f_{QU} = (345\,MHz - 10.7\,MHz)/64 = 5.2234\,MHz$$

4.5 Data Slicer Threshold Generation

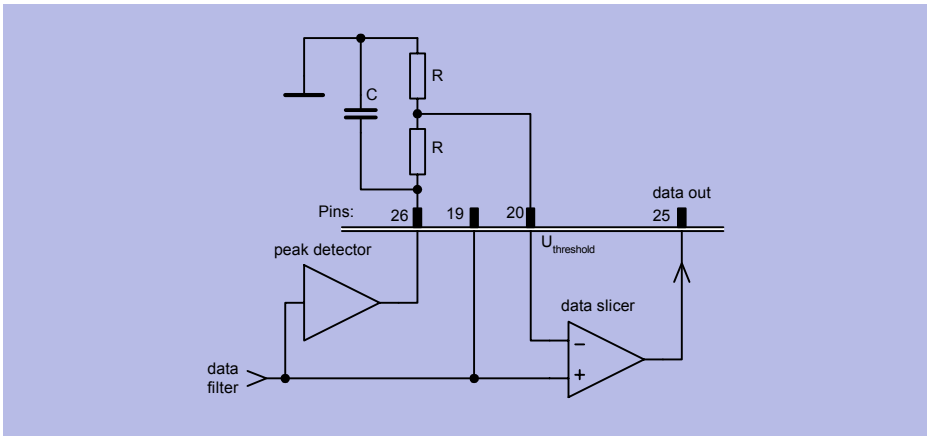
The threshold of the data slicer can be generated in two ways, depending on the signal coding scheme used. In case of a signal coding scheme without DC content such as Manchester coding the threshold can be generated using an external R-C integrator as shown in the following . The cut-off frequency of the R-C integrator has to be lower than the lowest frequency appearing in the data signal. In order to keep distortion low, the minimum value for R is 20kΩ.



Data_slice1.wmf

Figure 4-5 Data Slicer Threshold Generation with External R-C Integrator

Another possibility for threshold generation is to use the peak detector in connection with two resistors and one capacitor as shown in the following figure. The component values are depending on the coding scheme and the protocol used.



Data_slice2.wmf

Figure 4-6 Data Slicer Threshold Generation Utilising the Peak Detector

5 Reference

Contents of this Chapter

5.1 Electrical Data

5.1.1 Absolute Maximum Ratings

WARNING

The maximum ratings may not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC will result.

Table 5-1 Absolute Maximum Ratings, Ambient temperature T_{AMB}=-40°C ... + 85°C

#	Parameter	Symbol	Limit Values		Unit	Remarks
			min	max		
1	Supply Voltage	V_s	-0.3	5.5	V	
2	Junction Temperature	T_j	-40	+150	°C	
3	Storage Temperature	T_s	-40	+125	°C	
4	Thermal Resistance	R_{thJA}		114	K/W	
5	ESD integrity, all pins	V_{ESD}	-1	+1	kV	HBM according to MIL STD 883D, method 3015.7

5.1.2 Operating Range

Within the operating range the IC operates as explained in the circuit description. The AC/DC characteristic limits are not guaranteed.

Supply voltage: VCC = 4.5V .. 5.5V

Table 5-2 Operating Range, Ambient temperature T_{AMB}= -40°C ... + 85°C

#	Parameter	Symbol	Limit Values		Unit	Test Conditions	L	Item
			min	max				
1	Supply Current	I_S		5.2	mA	f_{RF} = 315MHz		
2	Receiver Input Level	RF_{in}	-110	-13	dBm	@ source impedance 50Ω, BER 2E-3, average power level, Manchester encoded datarate 4kBit, 280kHz IF Bandwidth	■	
3	LNI Input Frequency	f_{RF}	310	350	MHz			
4	MI/X Input Frequency	f_{MI}	310	350	MHz			
5	3dB IF Frequency Range	$f_{IF\ -3dB}$	5	23	MHz			
6	Powerdown Mode On	$PWDN_{ON}$	0	0.8	V			
7	Powerdown Mode Off	$PWDN_{OFF}$	2	V_S	V			
8	Gain Control Voltage, LNA high gain state	V_{THRES}	2.8	V_S	V			
9	Gain Control Voltage, LNA low gain state	V_{THRES}	0	0.7V	V			

■ This value is guaranteed by design.

5.1.3 AC/DC Characteristics

AC/DC characteristics involve the spread of values guaranteed within the specified voltage and ambient temperature range. Typical characteristics are the median of the production. The device performance parameters marked with ■ were measured on an Infineon evaluation board as desdribed in Section 5.2

Table 5-3 AC/DC Characteristics with T_A 25 °C, V_{VCC} = 4.5 ... 5.5 V

#	Parameter	Symbol	Limit Values			Unit	Test Conditions	L	Item
			min	typ	max				
Supply									
Supply Current									
1	Supply current, standby mode	$I_{S\ PDWN}$		50	70	nA	Pin 27 (PDWN) open or tied to 0 V		
2	Supply current	I_S		4.6	5	mA			
LNA									
Signal Input LNI (PIN 3), V_{THRES} > 2.8V, high gain mode									
1	Average Power Level at BER = 2E-3 (Sensitivity)	RF_{in}		-112		dBm	Manchester encoded datarate 4kBit, 280kHz IF Bandwidth	■	
2	Input impedance, f_{RF} = 315 MHz	$S_{11\ LNA}$		0.895 / -25.5 deg				■	
3	Input level @ 1dB C.P. f_{RF}=315 MHz	$P1dB_{LNA}$		-14		dBm		■	
4	Input 3rd order intercept point f_{RF} = 315 MHz	$IIP3_{LNA}$		-10		dBm	f_{in} = 315 & 317MHz	■	
5	LO signal feedthrough at antenna port	LO_{LNI}		-119		dBm		■	
Signal Output LNO (PIN 6), V_{THRES} > 2.8V, high gain mode									
1	Gain f_{RF} = 315 MHz	$S_{21\ LNA}$		1.577 / 150.3 deg				■	
2	Output impedance, f_{RF} = 315 MHz	$S_{22\ LNA}$		0.897 / -10.3 deg				■	
3	Voltage Gain Antenna to MI f_{RF} = 315 MHz	G_{AntMI}		21		dB			
4	Noise Figure	NF_{LNA}		2		dB	excluding matching network loss - see Appendix	■	
Signal Input LNI, V_{THRES} = GND, low gain mode									
1	Input impedance, f_{RF} = 315 MHz	$S_{11\ LNA}$		0.918 / -25.2 deg				■	
2	Input level @ 1dB C. P. f_{RF} = 315 MHz	$P1dB_{LNA}$		-7		dBm	matched input	■	

Table 5-3 AC/DC Characteristics with T_A 25 °C, V_{VCC} = 4.5 ... 5.5 V (continued)

	Parameter	Symbol	Limit Values			Unit	Test Conditions	L	Item
			min	typ	max				
Signal Input LNI, V_{THRES} = GND, low gain mode									
3	Input 3rd order intercept point f_{RF} = 315 MHz	$IIP3_{LNA}$		-13		dBm	f_{in} = 315 & 317MHz	■	
Signal Output LNO, V_{THRES} = GND, low gain mode									
1	Gain f_{RF} = 315 MHz	$S_{21\ LNA}$		0.007 / 153.7 deg				■	
2	Output impedance, f_{RF} = 315 MHz	$S_{22\ LNA}$		0.907 / -10.5 deg				■	
3	Voltage Gain Antenna to MI f_{RF} = 315 MHz	G_{AntMI}		2		dB			
Signal 3VOUT (PIN 24)									
1	Output voltage	V_{3VOUT}		3		V			
2	Current out	I_{3VOUT}			50	µA			
Signal THRES (PIN 23)									
1	Input Voltage range	V_{THRES}	0		V_S-1V	V	see chapter 4.1		
2	LNA low gain mode	V_{THRES}	0			V			
3	LNA high gain mode	V_{THRES}	2.8	3	V_S	V	or shorted to Pin 24		
4	Current in	I_{THRES_in}		5		nA			
Signal TAGC (PIN 4)									
1	Current out, LNA low gain state	I_{TAGC_out}		4.2		µA	RSSI > V_{THRES}		
2	Current in, LNA high gain state	I_{TAGC_in}		1.5		µA	RSSI < V_{THRES}		
MIXER									
Signal Input MI/MIX (PINS 8/9)									
1	Input impedance, f_{RF} = 315 MHz	$S_{11\ MIX}$		0.954 / -10.9 deg				■	
2	Input 3rd order intercept point	$IIP3_{MIX}$		-25		dBm		■	
Signal Output IFO (PIN 12)									
1	Output impedance	Z_{IFO}		330		Ω			
2	Conversion Voltage Gain f_{RF}=869 MHz	G_{MIX}		+21		dB			
3	Noise Figure, SSB (~DSB NF+3dB)	NF_{MIX}		13		dB		■	
4	RF to IF isolation	A_{RF-IF}		46		dB		■	

Table 5-3 AC/DC Characteristics with T_A 25 °C, V_{VCC} = 4.5 ... 5.5 V (continued)

	Parameter	Symbol	Limit Values			Unit	Test Conditions	L	Item
			min	typ	max				
LIMITER									
Signal Input LIM/X (PINS 17/18)									
1	Input Impedance	Z_{LIM}	264	330	396	Ω		■	
2	RSSI dynamic range	DR_{RSSI}	60		80	dB			
3	RSSI linearity	LIN_{RSSI}		±1		dB		■	
4	Operating frequency (3dB points)	f_{LIM}	5	10.7	23	MHz		■	
DATA FILTER									
1	Useable bandwidth	$BW_{BB\ FILT}$			100	kHz		■	
2	RSSI Level at Data Filter Output SLP	$RSSI_{low}$	0.9			V	LNA in high gain RF_{IN} ~-103dBm		
3	RSSI Level at Data Filter Output SLP	$RSSI_{high}$			2.8	V	LNA in high gain. RF_{IN} ~-30dBm		
SLICER									
Signal Output DATA (PIN 25)									
1	Useable bandwith	$BW_{BB\ SLIC}$			100	kHz		■	
2	Capacitive loading of output	$C_{max\ SLIC}$			20	pF			
3	LOW output voltage	V_{SLIC_L}		0		V			
4	HIGH output voltage	V_{SLIC_H}			V_S-1V	V			
5	Output current	I_{SLIC_out}			200	µA			
PEAK DETECTOR									
Signal Output PDO (PIN 26)									
1	LOW output voltage	V_{SLIC_L}		0		V			
2	HIGH output voltage	V_{SLIC_H}			V_S-1	V			
3	Load current	I_{load}			500	µA			
4	Leakage current	$I_{leakage}$		700		nA			

Table 5-3 AC/DC Characteristics with T_A 25 °C, V_{VCC} = 4.5 ... 5.5 V (continued)

	Parameter	Symbol	Limit Values			Unit	Test Conditions	L	Item
			min	typ	max				
CRYSTAL OSCILLATOR									
Signals CRSTL1, CRISTL 2, (PINS 1/28)									
1	Operating frequency	f_{CRSTL}	5		11	MHz	fundamental mode, series resonance		
2	Input Impedance @ ~5MHz	$Z_{1\text{-}28}$		-760 +j580		Ω		■	
3	Input Impedance @ ~10MHz	$Z_{1\text{-}28}$		-600 +j870		Ω		■	
4	Serial Capacity @ ~5MHz	$C_{S\ 5}$=C1		9.3		pF			
5	Serial Capacity @ ~10MHz	C_{S10}=C1		6.4		pF			
PLL									
Signal LF (PIN 15)									
1	Tuning voltage relative to V_S	V_{TUNE}	0.4	1.6	2.4	V			
POWER DOWN MODE									
Signal PDWN (PIN 27)									
1	Powerdown Mode On	$PWDN_{ON}$	0		0.8	V			
2	Powerdown Mode Off	$PWDN_{Off}$	2.8		V_S	V			
3	Input bias current PDWN	I_{PDWN}		t.b.d.		µA			
4	Start-up Time until valid IF signal is detected	T_{SU}			1	mS			
PLL DIVIDER									
Signal CSEL (PIN 16)									
1	f_{CRSTL} range 5.xxMHz	V_{CSEL}	1.4		4	V	or open		
2	f_{CRSTL} range 10.xxMHz	V_{CSEL}	0		0.2	V			
3	Input bias current CSEL	I_{CSEL}		5		µA	CSEL tied to GND		

■ Measured only in lab.

5.2 Test Circuit

The device performance parameters marked with ■ in Section 5.1.3 were measured on an Infineon evaluation board. This evaluation board can be obtained together with evaluation boards of the accompanying transmitter device TDA5101 in an evaluation kit that may be ordered on the INFINEON RKE Webpage www.infineon.com/rke

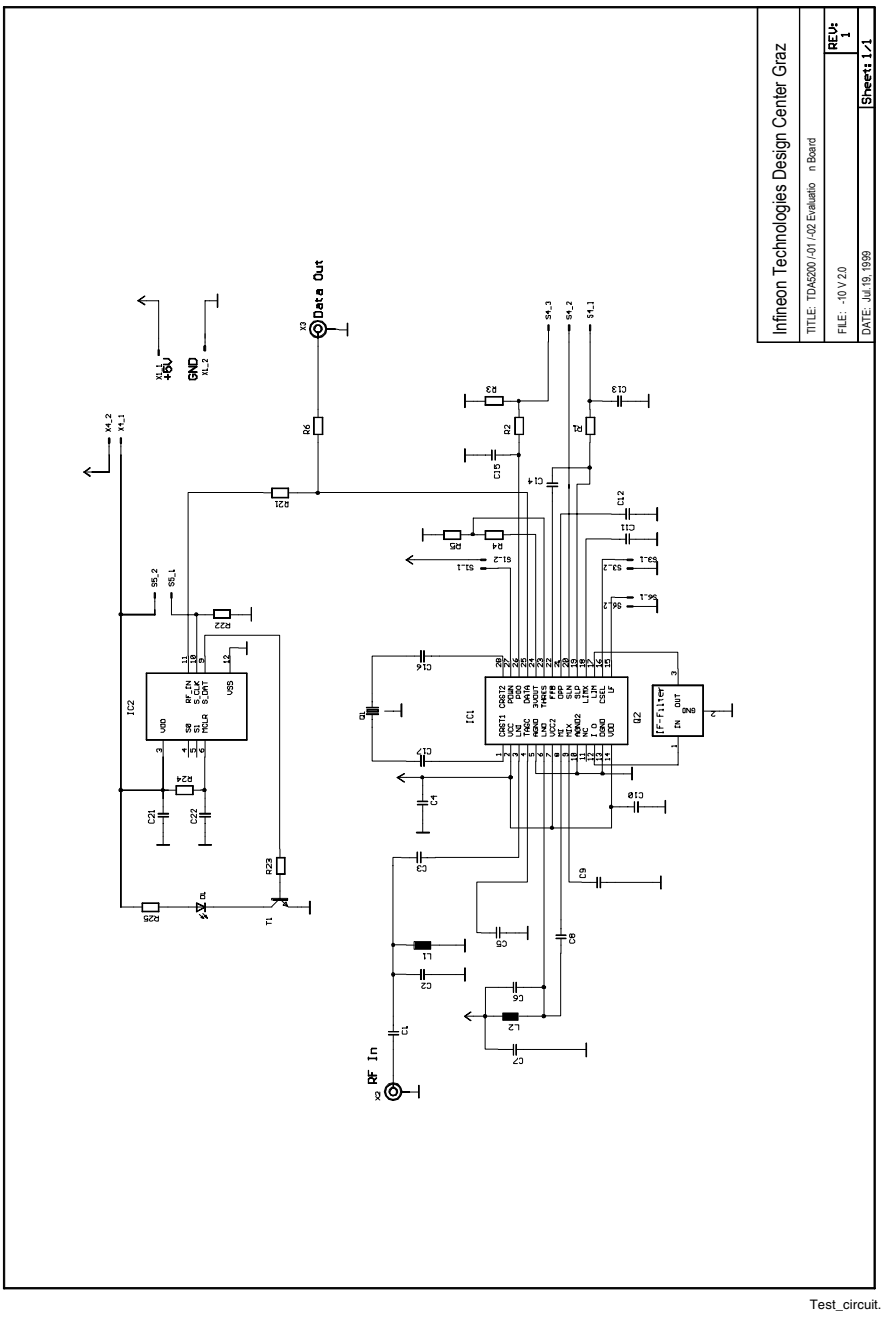


Figure 5-1 Schematic of the Evaluation Board

5.3 Test Board Layouts

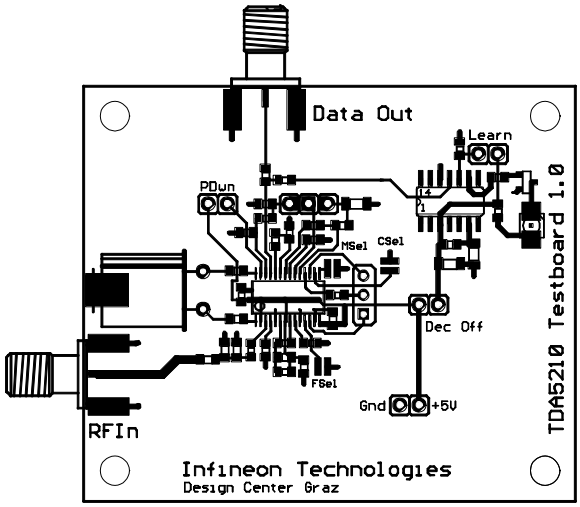


Figure 5-2 Top Side of the Evaluation Board

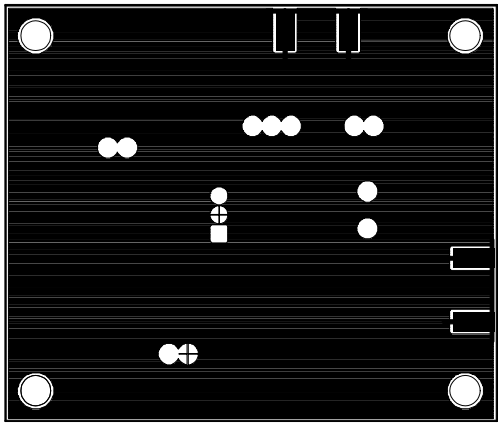


Figure 5-3 Bottom Side of the Evaluation Board

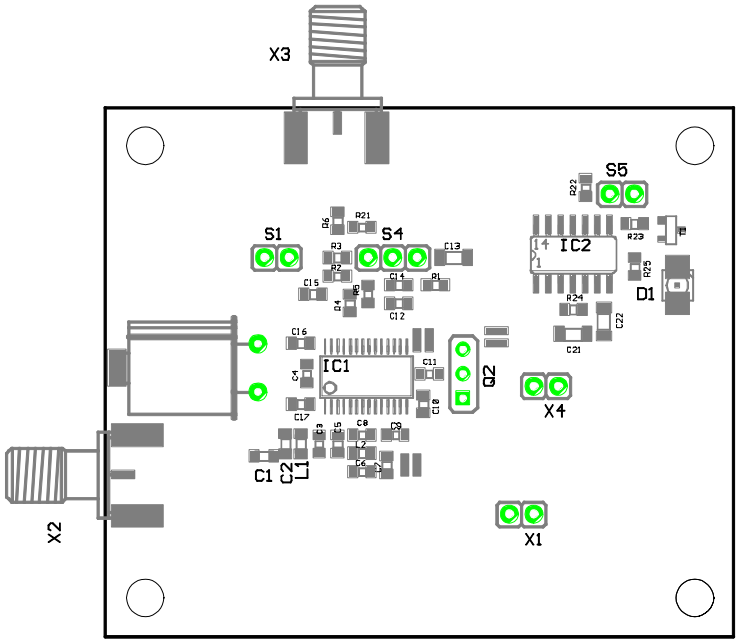


Figure 5-4 Component Placement on the Evaluation Board

5.4 Bill of Materials

The following components are necessary for evaluation of the TDA5201 at 315MHz without use of a Microchip HCS515 decoder.

Table 5-4 Bill of Materials

Ref	Value	Specification
R1	100kΩ	0805, ± 5%
R2	100kΩ	0805, ± 5%
R3	820kΩ	0805, ± 5%
R4	120kΩ	0805, ± 5%
R5	180kΩ	0805, ± 5%
R6	10kΩ	0805, ± 5%
L1	15nH	Toko, PTL2012-F15N0G
L2	12pF	0805,COG, ± 2%
C1	3.3 pF	0805, COG, ± 0.1pF
C2	10pF	0805, COG, ± 0.1pF
C3	6.8pF	0805, COG, ± 0.1pF
C4	100pF	0805, COG, ± 5%
C5	47nF	1206, X7R, ± 10%
C6	15nH	Toko, PTL2012-F15N0G
C7	100pF	0805, COG, ± 5%
C8	33pF	0805, COG, ± 5%
C9	100pF	0805, COG, ± 5%
C10	10nF	0805, X7R, ± 10%
C11	10nF	0805, X7R, ± 10%
C12	220pF	0805, COG, ± 5%
C13	47nF	0805, X7R, ± 10%
C14	470pF	0805, COG, ± 5%
C15	47nF	0805, X7R, ± 10%
C16	18pF	0805, COG, ± 0.1pF
C17	12pF	0805, COG, ± 2%
Q2	(315 + 10.7MHz)/32	HC49/U, fundamental mode, C_L = 12pF, e.g. 434.2 MHz: Jauch Q 10.17813-S11-1323-12-10/20
F1	SFE10.7MA5-A	Murata
X2, X3	142-0701-801	Johnson
X1, X4, S1, S5		2-pole pin connector
S4		3-pole pin connector, or not equipped
IC1	TDA 5201	Infineon

The following components are necessary in addition to the above mentioned ones for evaluation of the TDA5201 in conjunction with a Microchip HCS515 decoder.

Table 5-5 Bill of Materials Addendum

Ref	Value	Specification
R21	22kΩ	0805, ± 5%
R22	100kΩ	0805, ± 5%
R23	22kΩ	0805, ± 5%
R24	820kΩ	0805, ± 5%
R25	560kΩ	0805, ± 5%
C21	100nF	1206, X7R, ± 10%
C22	100nF	1206, X7R, ± 10%
IC2	HCS515	Microchip
T1	BC 847B	Infineon
D1	LS T670-JL	Infineon

5.5 Appendix - Noise Figure and Gain Circles

The following gain and noise figure circles were measured utilizing Microlab Stub Stretchers and a HP8514 network analyser. Maximum gain is shown at point 1 at 18.5 dB, minimum noise figure ist 1.9dB at point 2, step size of circles is 0.5dB.

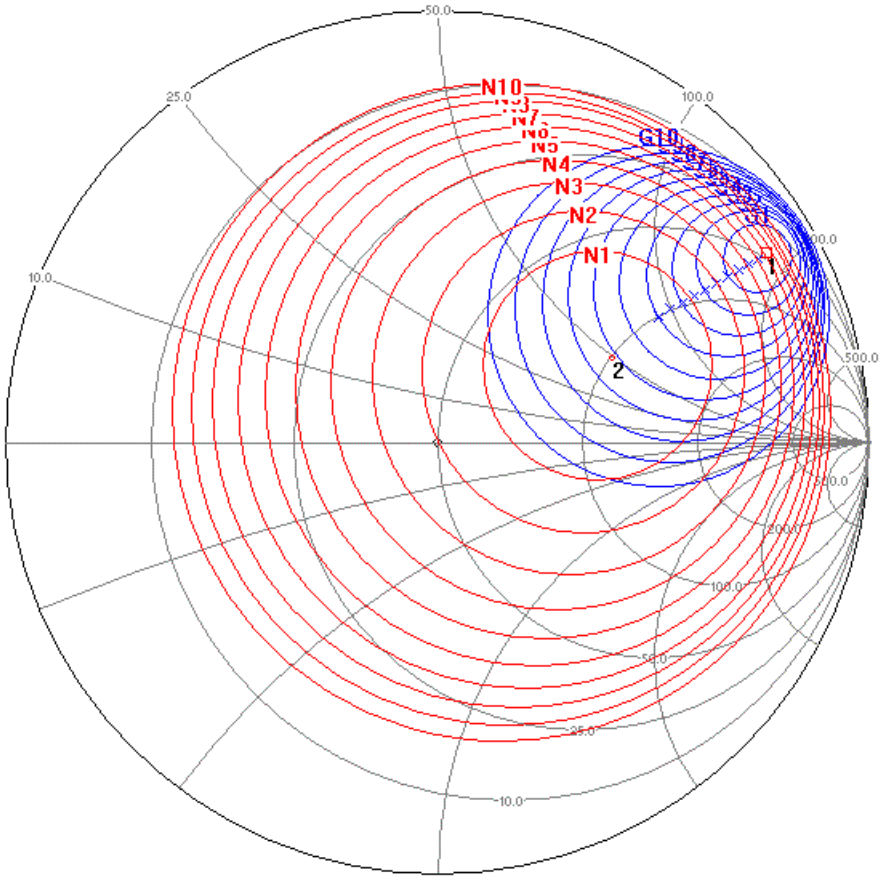


Figure 5-5 Gain and Noise Circles of the TDA5201 at 315 MHz.

List of Figures

List of Tables

List of Tables