S5N8952X
DMT Modem for the ADSL NIC Transceiver

Preliminary Information
(Revision 2.2)

January   2001

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1. Features

- Full Compliant with ANSI **T1.413 Issue-2**, ITU **G.992.1** (G.dmt) and **G.992.2** (G.lite)
- FDM based **DMT** line code
- Data Rate: over **8Mbps** for downstream and **640 Kbps** for upstream
- Reach: **22Kft** (6.7 Km)with **24 AWG** and **18 Kft** (5.5 Km)with **26 AWG**
- Compatible to **PCI V2.2**
- Handles **ATM cells** with **on-chip SAR** and connection memory
- Reed-Solomon **forward error correction** with **interleaver**
- Adaptive frequency and time domain **equalizer**
- **Trellis coding** and **echo cancellation**
- Supports **dual-latency** mode
- **18㎜, 1.8V** CMOS Technology
- Operating Temperature**: 0** °C to **70** °C
- Package Type: **208-LQFP**

2. General Description

The modem consists of two main parts; The **S5N8943**, an analog front-end, provides an analog interface with line drivers and hybrid components to connect the PSTN. The **S5N8952** is a complete ATM-based ADSL modem solution with associated F/W and an Analog Front-End (S5N8951). The S5N8952X provides all the digital functions with DSP such as PCI bus Interface, ATM SAR, ATM TC and (De)Framer, FEC Codec with (De)interleaver, Adaptive QAM Codec, FFT/IFFT, Equalizers, and Digital Filters.

The PCI bus interface of which bus frequency is up to 33MHz, is compilant with PCI specification v2.2, and supports + 3.3V or + 5V PCI interface for NIC applications. The AD/DA interface provides 4.4MHz sample rate with 14-bit resolution. The S5N8952, which consists of DMT modem and on-chip PCI/SAR, is optimized for providing NIC solution for CPE, and uses 17.664MHz as a master clock.
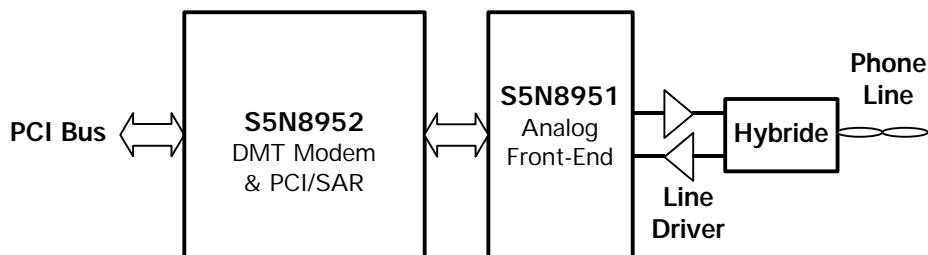

Figure 1: General Block Diagram
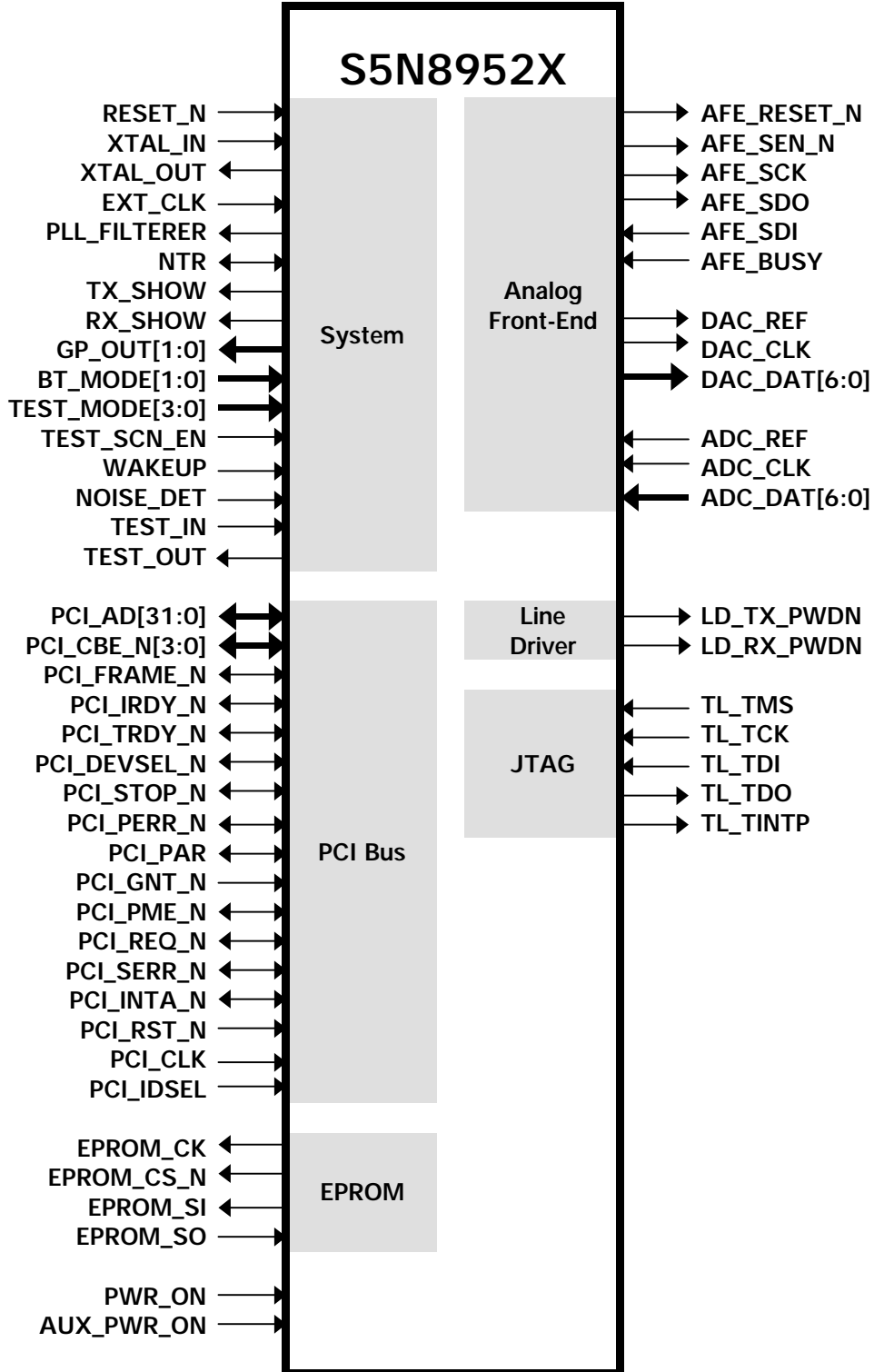
3. Logical Symbol Diagram

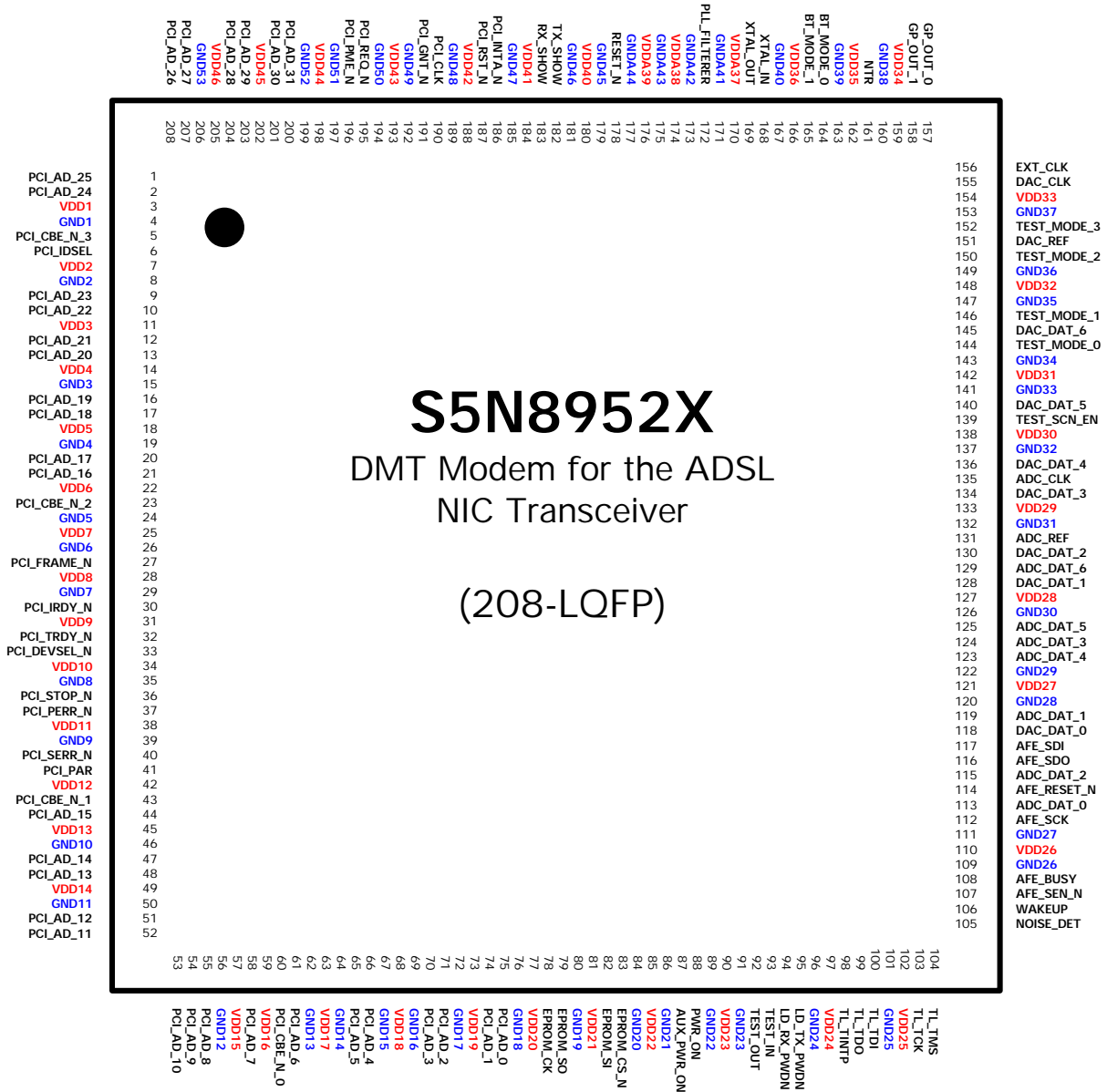Figure 2: Logical Symbol Diagram of the S5N8952X

4. Pin Configuration

Figure 3: Pin Configuration of the S5N8952X

5. Pin Description

Table 1: Pin Description of the S5N8952X

Pin No	Pin Name	I/O Type	Description
			System
178	**RESET_N**	I	System master reset (Active low)
168	**XTAL_IN**	I	System master clock (17.664MHz xtal oscillator for ATU-C, and VCXO for ATU-R)
169	**XTAL_OUT**	O	
156	**EXT_CLK**	I	External clock for test (Float in normal mode)
172	**PLL_FILTERER**	O	PLL pump out (A 320 pF capacitor between the pin and ground)
161	**NTR**	B	ATM network timing reference (8KHz, Float if not needed)
182	**TX_SHOW**	O	Tx show time indicator (Active high. Connect to LED)
183	**RX_SHOW**	O	Rx show time indicator (Active high. Connect to LED)
158	**GP_OUT_1**	O	General purpose outputs (Float if not needed)
157	**GP_OUT_0**		
165	**BT_MODE_1**	I	Boot Mode Selection [0] Reset, [1] Boot from Host [2] Boot from JTAG, [3] Self-Booting
164	**BT_MODE_0**		
152	**TEST_MODE_3**	I	Chip test mode [0] Normal mode, [1-15] Test mode
150	**TEST_MODE_2**		
146	**TEST_MODE_1**		
144	**TEST_MODE_0**		
139	**TEST_SCN_EN**	I	Test scan enable (Set to '0' in normal mode)
106	**WAKEUP**	I	Wake up (Active High)
105	**NOISE_DET**	I	Noise Detect (Active high)
93	**TEST_IN**	I	Test input (Float in normal mode)
92	**TEST_OUT**	O	Test output (Float in normal mode)
			PCI Bus
200	**PCI_AD_31**	B	PCI address data [31:0]
201	**PCI_AD_30**		
203	**PCI_AD_29**		
204	**PCI_AD_28**		
207	**PCI_AD_27**		
208	**PCI_AD_26**		
1	**PCI_AD_25**		
2	**PCI_AD_24**		
9	**PCI_AD_23**		
10	**PCI_AD_22**		
12	**PCI_AD_21**		
13	**PCI_AD_20**		
16	**PCI_AD_19**		
17	**PCI_AD_18**		
20	**PCI_AD_17**		

21	**PCI_AD_16**		
44	**PCI_AD_15**		
47	**PCI_AD_14**		
48	**PCI_AD_13**		
51	**PCI_AD_12**		
52	**PCI_AD_11**		
53	**PCI_AD_10**		
54	**PCI_AD_9**		
55	**PCI_AD_8**		
58	**PCI_AD_7**		
61	**PCI_AD_6**		
65	**PCI_AD_5**		
66	**PCI_AD_4**		
70	**PCI_AD_3**		
71	**PCI_AD_2**		
74	**PCI_AD_1**		
75	**PCI_AD_0**		
5	**PCI_CBE_N_3**	B	PCI command byte enable
23	**PCI_CBE_N_2**		
43	**PCI_CBE_N_1**		
60	**PCI_CBE_N_0**		
27	**PCI_FRAME_N**	B	PCI frame
30	**PCI_IRDY_N**	B	PCI initiator ready
32	**PCI_TRDY_N**	B	PCI target ready
33	**PCI_DEVSEL_N**	B	PCI device select
36	**PCI_STOP_N**	B	PCI stop
37	**PCI_PERR_N**	B	PCI parity error
41	**PCI_PAR**	B	PCI parity bit
191	**PCI_GNT_N**	I	PCI grant
40	**PCI_SERR_N**	OZ	PCI system error
186	**PCI_INTA_N**	OZ	PCI interrupt A
196	**PCI_PME_N**	OZ	PCI power management event
195	**PCI_REQ_N**	OZ	PCI request
187	**PCI_RST_N**	I	PCI reset
190	**PCI_CLK**	I	PCI clock
6	**PCI_IDSEL**	I	PCI initialization device select
78	**EPROM_CK**	O	EPROM clock
83	**EPROM_CS_N**	O	EPROM chip select (Active low)
82	**EPROM_SI**	O	EPROM serial data in
79	**EPROM_SO**	I	EPROM serial data out
88	**PWR_ON**	I	Main power detected (Active high)
87	**AUX_PWR_ON**	I	Aux power detected (Active high)
	Analog Front-End		
114	**AFE_RESET_N**	O	AFE reset (Active low)
107	**AFE_SEN_N**	O	AFE serial interface enable (Active low)
112	**AFE_SCK**	O	AFE serial interface clock
116	**AFE_SDO**	O	AFE serial interface data out
117	**AFE_SDI**	I	AFE serial interface data in
108	**AFE_BUSY**	I	AFE serial interface busy (Active high. Float if not

			needed)
151	**DAC_REF**	O	DAC data reference
155	**DAC_CLK**	O	DAC sample clock
145	**DAC_DAT_6**		
140	**DAC_DAT_5**		
136	**DAC_DAT_4**		
134	**DAC_DAT_3**	O	DAC data
130	**DAC_DAT_2**		
128	**DAC_DAT_1**		
118	**DAC_DAT_0**		
131	**ADC_REF**	I	ADC data reference
135	**ADC_CLK**	I	ADC sample clock
129	**ADC_DAT_6**		
125	**ADC_DAT_5**		
123	**ADC_DAT_4**		
124	**ADC_DAT_3**	I	ADC data
115	**ADC_DAT_2**		
119	**ADC_DAT_1**		
113	**ADC_DAT_0**		
	Line Driver		
95	**LD_TX_PWDN**	O	Tx line driver power down (Active high)
94	**LD_RX_PWDN**	O	Rx line driver power down (Active high)
	JTAG		
104	**TL_TMS**	I	JTAG test mode selection
103	**TL_TCK**	I	JTAG test clock
100	**TL_TDI**	I	JTAG test data in
99	**TL_TDO**	O	JTAG test data out
98	**TL_TINTP**	O	TJAM interrupt to host
	Power/Ground		
11	**VDD3**		
22	**VDD6**		
31	**VDD9**		
42	**VDD12**		
59	**VDD16**		
77	**VDD20**		
85	**VDD22**		
97	**VDD24**	P1	1.8V supply voltage
110	**VDD26**		
127	**VDD28**		
138	**VDD30**		
148	**VDD32**		
159	**VDD34**		
162	**VDD35**		
180	**VDD40**		
202	**VDD45**		
3	**VDD1**	P1	3.3V supply voltage
14	**VDD4**		
18	**VDD5**		
25	**VDD7**		
34	**VDD10**		

38	**VDD11**		
49	**VDD14**		
57	**VDD15**		
63	**VDD17**		
73	**VDD19**		
81	**VDD21**		
90	**VDD23**		
102	**VDD25**		
121	**VDD27**		
133	**VDD29**		
142	**VDD31**		
154	**VDD33**		
166	**VDD36**		
184	**VDD41**		
188	**VDD42**		
198	**VDD44**		
205	**VDD46**		
7	**VDD2**		
28	**VDD8**		
45	**VDD13**	P1	3.3V or 5V supply voltage for PCI
68	**VDD18**		
193	**VDD43**		
4	**GND1**	P0	Ground
8	**GND2**		
15	**GND3**		
19	**GND4**		
24	**GND5**		
26	**GND6**		
29	**GND7**		
35	**GND8**		
39	**GND9**		
46	**GND10**		
50	**GND11**		
56	**GND12**		
62	**GND13**		
64	**GND14**		
67	**GND15**		
69	**GND16**		
72	**GND17**		
76	**GND18**		
80	**GND19**		
84	**GND20**		
86	**GND21**		
89	**GND22**		
91	**GND23**		
96	**GND24**		
101	**GND25**		
109	**GND26**		
111	**GND27**		

120	GND28		
122	GND29		
126	GND30		
132	GND31		
137	GND32		
141	GND33		
143	GND34		
147	GND35		
149	GND36		
153	GND37		
160	GND38		
163	GND39		
167	GND40		
179	GND45		
181	GND46		
185	GND47		
189	GND48		
192	GND49		
194	GND50		
197	GND51		
199	GND52		
206	GND53		
170	VDDA37		
174	VDDA38	P1	1.8V analog supply voltage
176	VDDA39		
171	GNDA41		
173	GNDA42	P0	Analog ground
175	GNDA43		
177	GNDA44		

[NOTE]

I = Input
O = Output
OZ = Tri-state Output
B = Bi-direction
P1 = Power
P0 = Ground

6. Functional Description

DMT inherently transmits an optimized time-variable spectrum. This spectrum is adjusted according to the desired data rate and the transmission characteristics (transfer function and noise spectrum) on each and every subchannel. For this, CO and CPE transmit 256 4kHz-wide tone downstream and upstream respectively to each other during initialization. They measure the quality of each of these received tones and then decide whether a tone has sufficient quality to be used for further transmission and, if so, how much data this tone should carry relative to the other tones that are used. They inform the bit loading informations to each other.

In FDM-based DMT (Discrete MultiTone) modulation, the frequency band, 0 to 1.104MHz, is divided into 256 equi-spaced subchannels with 4.3125KHz tone spacing. The frequency band, 26KHz (#6) to 134KHz (#31) is used for the upstream, and 142KHz (#33) to 1.1MHz (#255) for the downstream.

The S5N8952 provides PCI bus interface for NIC application and 14-bit AD/DA interface. SAR (Segmentation and Reassembly) and TC (Transmission Convergence) are implemented for ATM cell handling and especially on-chip hardware SAR provides more processing power by reducing the PCI bus traffic than the software SAR. Reed-Solomon forward error correction with/without interleaver and Trellis coded modulation increase channel noise immunity. Time/frequency-domain equalizers, echo canceler, and digital filters, of which coefficients are adaptively updated according to the channel conditions, enhance the performance of data recovery.
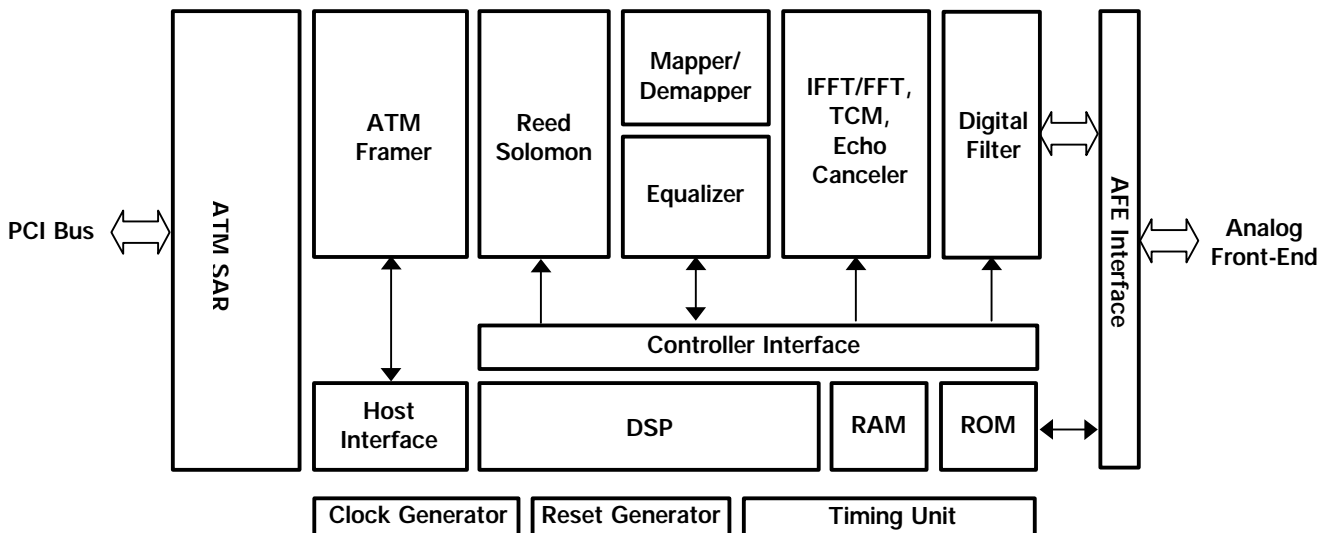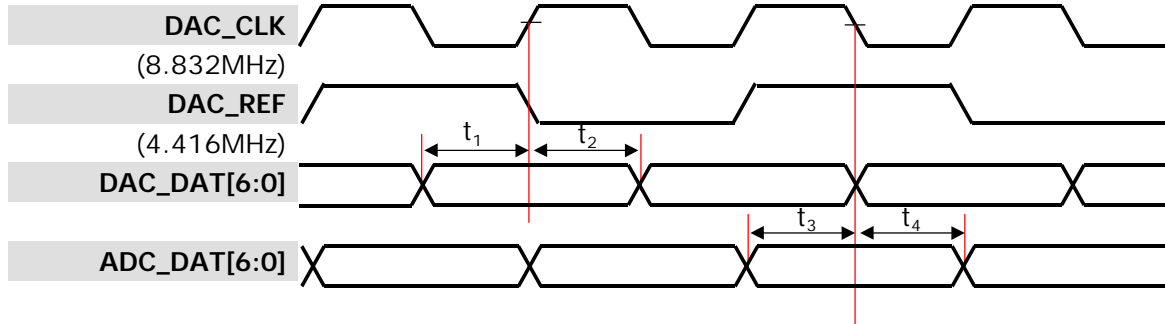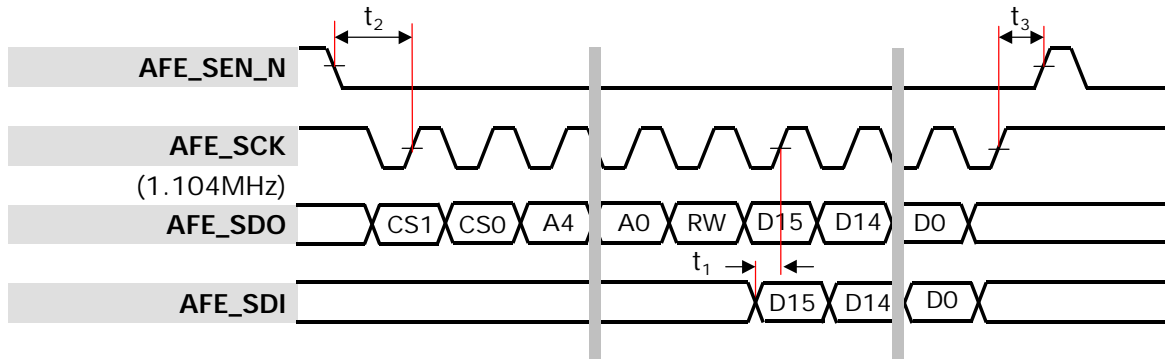

Figure 4: Functional Block Diagram of the S5N8952X

7. I/O Timing Description

Parameter	Description	Min	Max	Unit
t_1	DAC_DAT setup to DAC_CLK ↑	15		ns
t_2	DAC_DAT hold after DAC_CLK ↑	15		ns
t_3	ADC_DAT setup to DAC_CLK ↓	30		ns
t_4	ADC_DAT hold after DAC_CLK ↓	1		ns

Figure 5: AFE Data I/F Timing Diagram

Parameter	Description	Min	Max	Unit
t_1	AFE_SDI setup to AFE_SCK↑	30		ns
t_2	AFE_SEN_N ↓ before AFE_SCK ↑	30		ns
t_3	AFE_SEN_N ↑ from AFE_SCK ↑	15		ns

Figure 6: AFE Control I/F Timing Diagram
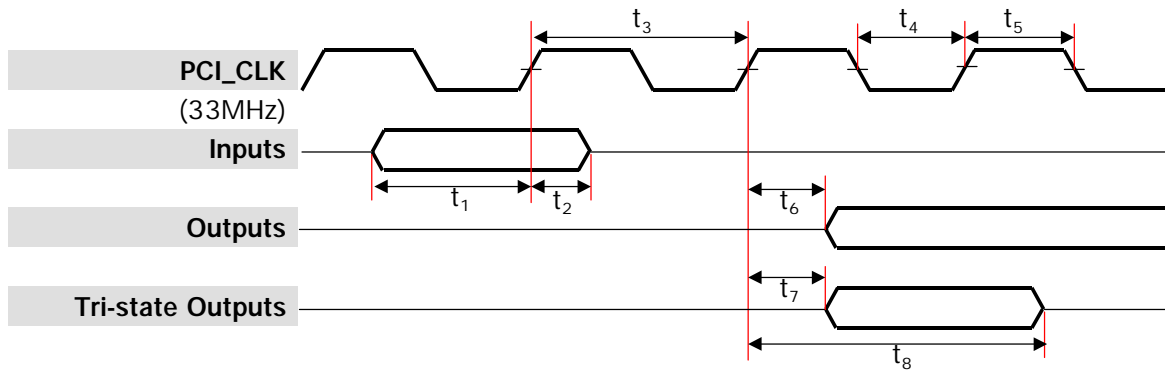
Parameter	Description	Min	Max	Unit
t_1	Input setup to PCI_CLK ↑	3		ns
t_2	Input hold after PCI_CLK ↑	0		ns
t_3	PCI_CLK period	30		ns
t_4	PCI_CLK low time	6		ns
t_5	PCI_CLK high time	6		ns
t_6	PCI_CLK ↑ to signal valid delay	1	6	ns
t_7	Float to active delay	1		ns
t_8	Active to float delay		14	ns

Figure 7: PCI I/F Timing Diagram

8. Electrical Characteristics

Table 2: Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
I_{LATCH}	Latch-up Current	±200	mA
T_{STG}	Storage Temperature	-65 to 150	°C

Table 3: Recommended Operating Conditions

Symbol	Parameter	Rating		Unit
V_{DD}	DC Supply Voltage	1.8V I/O	1.65 to 1.95	V
		3.3V I/O	3.0 to 3.6	
		5V-tolerant I/O (3.3V Interface)	3.0 to 3.6	
	Analog Core DC Supply Voltage	1.8V Core	1.8±5%	
T_A	Operating Temperature (Ambient)	Commercial	0 to 70	°C

Table 4: Power Dissipation

Symbol	Parameter	Min	Typ	Max	Unit
P_D	Power Dissipation	-	0.3	-	W

Table 5: DC Characteristics

Symbol	Parameters	Min	Typ	Max	Unit
V_{IH}	Input High Voltage	2.0	-	-	V
V_{IL}	Input Low Voltage	-	-	0.8	
V_{OH}	Output High Voltage	2.4	-	-	
V_{OL}	Output Low Voltage	-	-	0.4	
VT	Switching Threshold	-	1.4	-	
VT+	Schmitt Trigger, Positive-going Threshold	-	-	2.0	
VT-	Schmitt Trigger, Negative-going Threshold	0.8	-	-	
I_{IH}	Input High Current ($V_{IN} = V_{DD}$)	-10	-	10	µA
		10*	33*	60*	
I_{IL}	Input Low Current ($V_{IN} = V_{SS}$)	-10	-	10	
		-60*	-33*	-10*	
I_{OZ}	Tri-state Output Leakage Current	-10	-	10	
I_{DD}	Quiescent Supply Current	-	-	100	
C_{IN}	Input Capacitance	-	-	4	pF
C_{OUT}	Output Capacitance	-	-	4	

9. Package Description

A: 30.00±0.30
B: 28.00±0.20
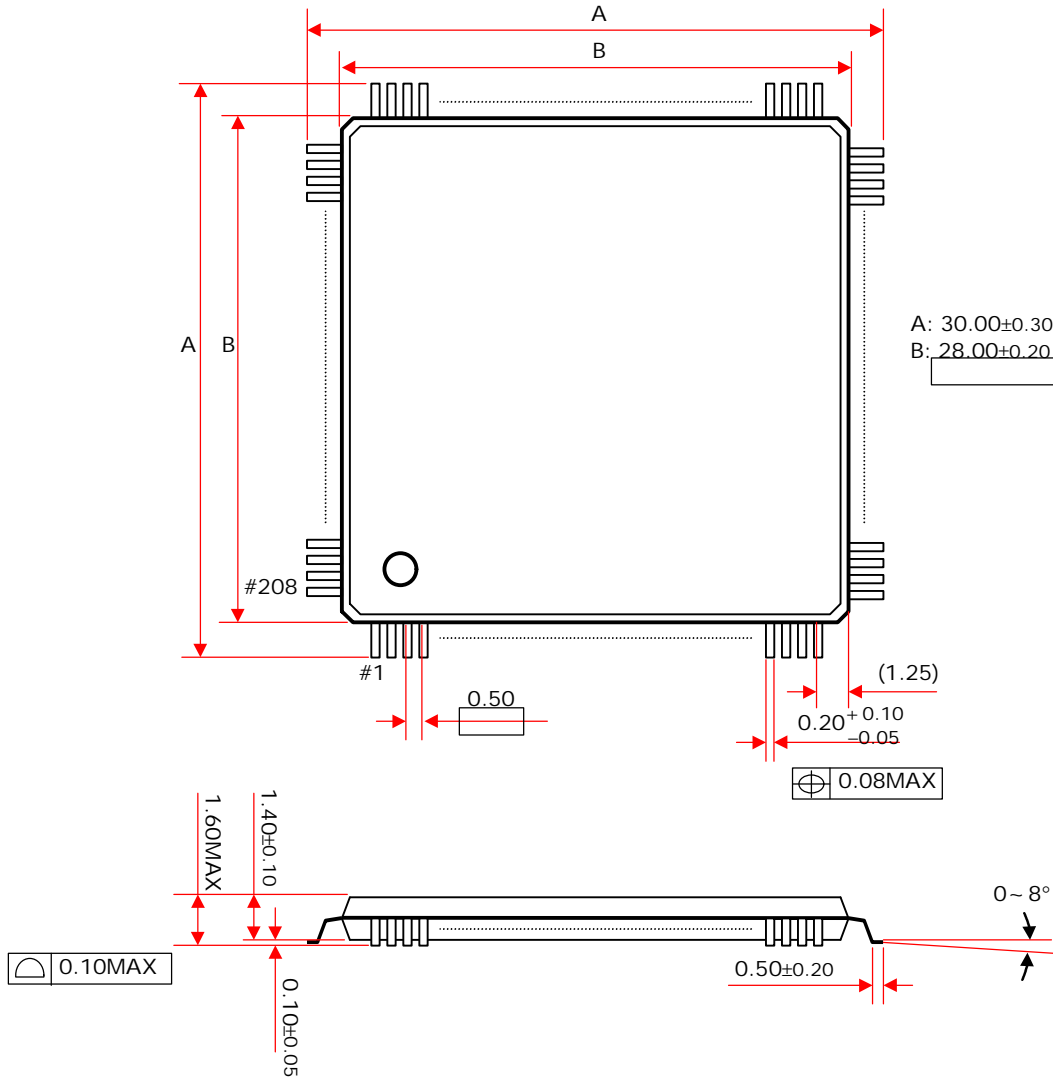
Figure 8: 208-LQFP Package Diagram

Revision History

Revision No.	Date	Description
1.0	2000-09-15	First released
1.1	2000-09-20	**Pin configuration** changed
2.2	2001-01-05	**Functional Description** updated

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