Data Sheet

NT68520X,E

XGA,SXGA Flat Panel Monitor Controller

Ver.1.0

REVISION HISTORY

NT68520 Specification Revision History		
Version	**Content**	**Date**
1.0	Final sheet first version	Apr 2003

FEATURES

VGA Front End

- Built-in triple high-speed ADC, PLL, and pre-amplifier for analog RGB input
- Support both non-interlaced and interlaced RGB graphic input signals
- Internal generated programmable clamping pulse
- Gain control for input signal ranging from 0.5V~1.0V
- Support 32 steps of phase adjust
- ADC sampling rate up to 110 MHz for X type and135 MHz for E type
- VGA input resolution up to XGA 1024x768@75 for X type and SXGA 1280x1024@75Hz for E type

YUV Front End

- Support ITU-R BT.656 8-bit Input
- Built-in YUV to RGB color space converter

Video Processor

- Flexible de-interlacing unit for VGA and digital YUV video input data
- Independent Horizontal and Vertical zoom in/out algorithm
- Enhanced interpolation algorithm for optimal image quality
- RGB offset control for brightness adjust
- RGB gain control for contrast adjust
- 8-bit programmable gamma table for panel compensation
- Dithering function supports 24-bit quality for 18-bit panel
- Auto-calibration function for quick video centering, clock adjust, and phase adjust

Sync Processor

- Signal type accepts separate, composite and TTL-Level Sync-On-Green (SOG)
- Polarity detection for HSYNCI and VSYNCI
- Fast mode change detection function

Internal OSD Support

- 128 ROM fonts at the size of 12x18
- 64 programmable RAM fonts
- Internal SRAM allows up to 320 characters, with programmable OSD frame size
- Programmable shadow or border control for each character
- Programmable blinking effect for each character

- Support simultaneous display of up to 4 OSD windows
- Programmable shadow display for each window
- Each OSD row can be independently zoomed up to 4 times for horizontal and vertical axes
- Support transparent, translucent, and opaque effects
- 16 colors for foreground display and background display selected from internal color palette

Display Interface

- Display resolution up to 1024x768@75Hz for X type and 1280x768@75Hz for E type
- Support single pixel mode (18-bit) and dual pixel mode (24-bit)

MCU Interface

- Support serial 2-wire IIC bus

Power

- 3.3V power supply
- Less than 2.5 W

GENERAL DESCRIPTION

The NT68520 is a high-quality image and highly integrated LCD controller, which combines triple video pre-amplifier, triple ADC, de-interlacing, YUV to RGB color space converter, scaling engine, gamma, OSD, and digital gain/offset, and supports analog RGB input, digital RGB input, and video CCIR656 8-bit input.

The video amplifier supports a full scale range of 0.5 ~ 1Vp-p with 0.8 ~ 2X gain and also provides a DC offset adjustment.

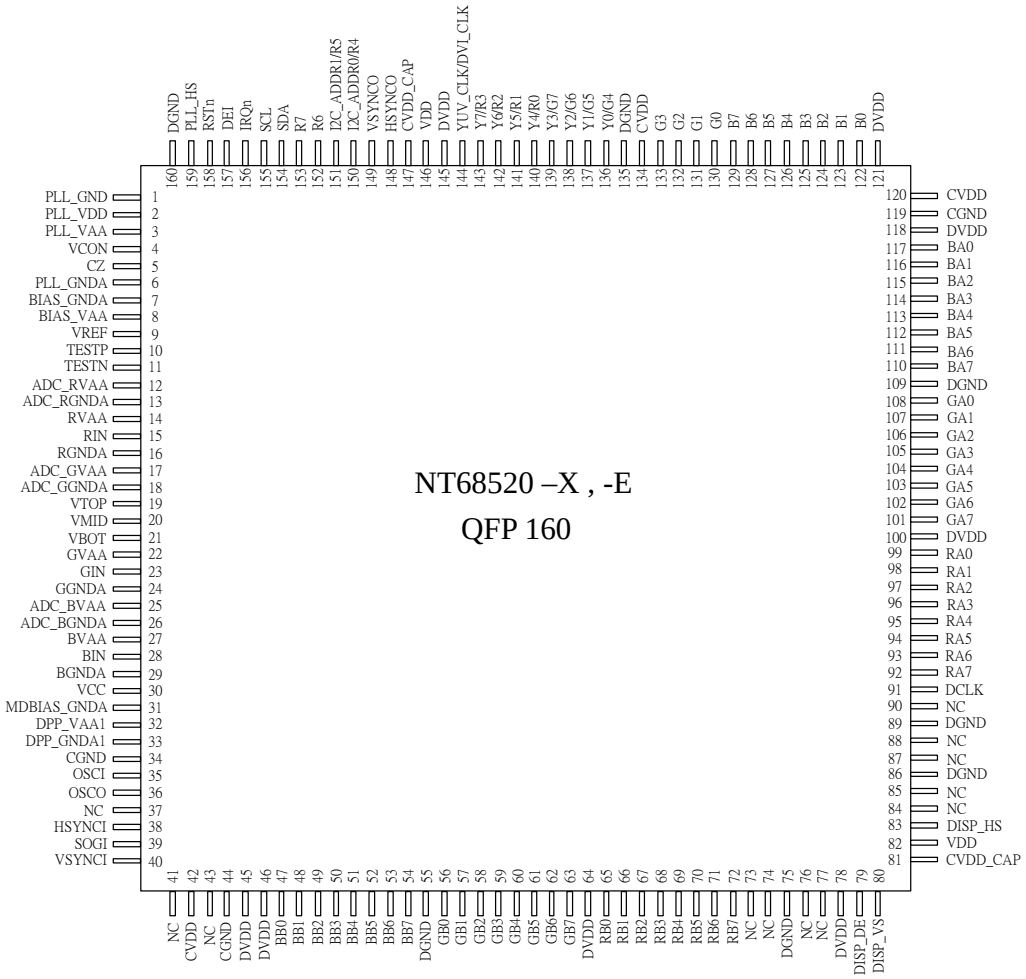
The ADC supports up to 135MHz pixel rate and build in a low jitter PLL to sampling input video that provides a low-noise and more stabile image quality.

The NT68520 also builds in a DSP engine to execute linear zoom-in, zoom-out function of image to fit different panel resolutions.

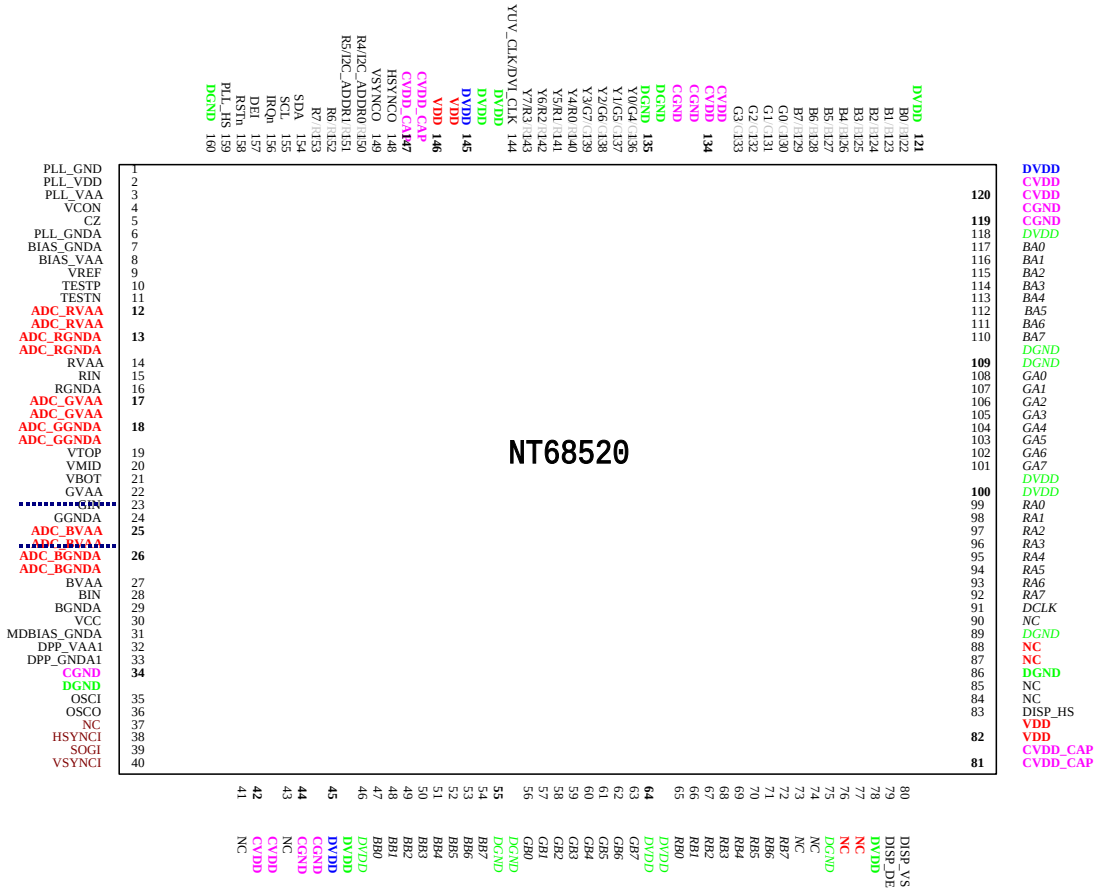
The OSD provides 64 RAM font and 128 ROM font that is very simply to create customer OSD.

The display interface supports single (24-bit) or dual (48-bit) pixel out format, and supports the 6-bit/color or 8-bit/color LCD panel. The built-in internal PLL locking to the reference clock generates all of the display timing to various LCD panels.

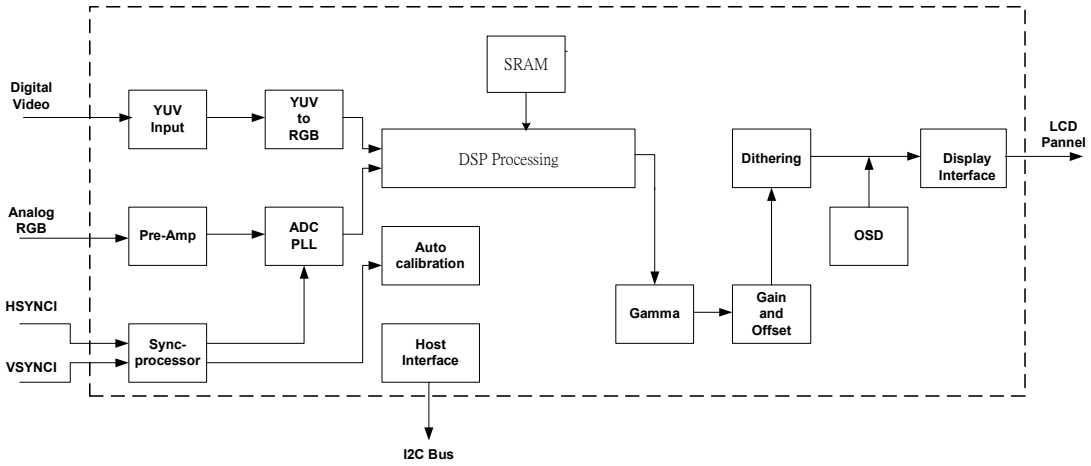
PIN CONFIGURATION



PAD CONFIGURATION



BLOCK DIAGRAM



PIN AND PAD DESCRIPTIONS

Pin No.	Pad No.	Name	Type	Description
1	1	PLL_GND	P	ADC PLL digital ground
2	2	PLL_VDD	P	ADC PLL digital power
3	3	PLL_VAA	P	ADC PLL analog power
4	4	VCON	I	PLL loop filter input
5	5	CZ	I	PLL loop filter internal resister input
6	6	PLL_GNDA	P	ADC PLL analog ground
7	7	BIAS_GNDA	P	Analog ground for ADC PLL internal bias circuit
8	8	BIAS_VAA	P	Analog power for ADC PLL internal bias circuit
9	9	VREF	P	External reference voltage of 2.5V
10	10	TESTP	O	VGA output test pin
11	11	TESTN	O	VGA output test pin
12	12,13	ADC_RVAA	P	ADC analog power for R channel
13	14,15	ADC_RGNDA	P	ADC analog ground for R channel
14	16	RVAA	P	Front-end analog power for R channel
15	17	RIN	I	R channel analog video input
16	18	RGNDA	P	Front-end analog ground for R channel
17	19,20	ADC_GVAA	P	ADC analog power for G channel
18	21,22	ADC_GGNDA	P	ADC analog ground for G channel
19	23	VTOP	P	ADC resister ladder top de-couple input
20	24	VMID	P	ADC resister ladder middle de-couple input
21	25	VBOT	P	ADC resister ladder bottom de-couple input
22	26	GVAA	P	Front-end analog power for G channel
23	27	GIN	I	G channel analog video input
24	28	GGNDA	P	Front-end analog ground for G channel
25	29,30	ADC_BVAA	P	ADC analog power for B channel
26	31,32	ADC_BGNDA	P	ADC analog ground for B channel
27	33	BVAA	P	Front-end analog power for B channel
28	34	BIN	I	B channel analog video input

29	35	BGNDA	P	Front-end analog ground for B channel
30	36	VCC	P	Display PLL analog power supply
31	37	MDBIAS_GNDA	P	Analog power for display PLL internal bias circuit
32	38	DPP_VAA1	P	Display PLL analog power
33	39	DPP_GNDA1	P	Display PLL analog ground
34	40	CGND	P	Core logic ground
	41	DGND		
35	42	OSCI	I	Crystal OSC input
36	43	OSCO	O	Crystal OSC output
37	44	NC		NC pin
38	45	HSYNCI	I	VGA port horizontal sync input with smith trigger
39	46	SOGI	I	VGA port Sync On Green input with smith trigger
40	47	VSYNCI	I	VGA port vertical sync input with smith trigger
41	48	NC	I	Connect to digital ground
42	49,50	CVDD	P	Core logic power de-couple pin. External capacitor (0.1uF) Connection is recommended.
43	51	NC		NC pin
44	52,53	CGND	P	Core logic ground
45	54,55	DVDD	P	Display digital power supply
46	56	DVDD	P	Display digital power supply
47-54	57-64	BB0 ~ BB7	O	Port B, B channel output
55	65,66	DGND	P	Display digital ground
56-63	67-74	GB0 ~ GB7	O	Port B, G channel output
64	75,76	DVDD	P	Display digital power supply
65-72	77-84	RB0- RB7	O	Port B, R channel output
73	85	NC		NC pin
74	86	NC		NC pin
75	87	DGND	P	Display digital ground
76	88	NC	P	Connect to digital ground
77	89	NC	P	Connect to digital ground
78	90	DVDD	P	Display digital power supply
79	91	DISP_DE	O	Panel display data enable signal
80	92	DISP_VS	O	Panel display vertical sync
81	93,94	CVDD_CAP	P	Internal regulator output pin. External regulating capacitor (10uF~100uF) connected is needed.
82	95,96	VDD	P	Main power supply for internal regulator (3.3V)
83	97	DISP_HS	O	Panel display horizontal sync
84	98	NC		NC pin

85	99	NC		NC pin
86	100	DGND	P	Display digital ground
87	101	NC		Connect to digital ground
88	102	NC		Connect to digital ground
89	103	DGND	P	Display digital ground
90	104	NC		NC pin
91	105	DCLK	O	Display clock
92-99	106-113	RA0 ~ RA7	O	Port A, R channel output
100	114,115	DVDD	P	Display digital power supply
101-108	116-123	GA0 ~ GA7	O	Port A, G channel output
109	124,125	DGND	P	Display digital ground
110-117	126-133	BA0 ~ BA7	O	Port A, B channel output
118	124	DVDD	P	Display digital power supply
119	125,126	CGND	P	Core logic ground
120	127	CVDD	P	Core logic power de-couple pin. External capacitor (0.1uF) Connection is recommended.
121	128	DVDD	P	Display digital power supply
122-133	129-140	B0~B7, G0~G3	I	Digital input B0~B7, G0~G7
134	141,142	CVDD	P	Core logic power de-couple pin. External capacitor (0.1uF) Connection is recommended.
	143,144	CGND	P	Core logic ground
135	145,146	DGND	P	Display digital ground
136-143	147-154	Y0-Y7 G4~G7, R0~R3	I	Video data input of bit 0~7 Digital input G4~G7, R0~R3
144	155	YUV_CLK/DVI_CLK	I	1.Video port clock input 2.Digital RGB clock input
145	156-158	DVDD	P	Display digital power supply
146	159-160	VDD	P	Main power supply for internal regulator (3.3V)
147	161,162	CVDD_CAP	P	Internal regulator output pin. External regulating capacitor (10uF~100uF) connection is needed.
148	163	HSYNCO	O	Sync-process horizontal sync output
149	164	VSYNCO	O	Sync-process vertical sync output
150	165	I2C_ADDR0/R4	I	1.I2C slave address, Refer to Page 27 I2C slave address setting 2.Digital input R4
151	166	I2C_ADDR1/R5	I	1.I2C slave address. Refer to Page 27 for I2C slave address setting 2.Digital input R5
152	167	R6		Digital input R6
153	168	R7		Digital input R7

154	169	SDA	I/O	Host interface serial data in/out incorporate smith trigger
155	170	SCL	I	Host interface serial clock incorporate smith trigger buffer & spike filter.
156	171	IRQn	I/O	Interrupt request output
157	172	DEI	I	Digital input data enable signal
158	173	RSTn	I	System reset
159	174	PLL_HS	I	H sync input for PLL
160	175	DGND	P	Display digital ground

FUNCTION DESCRIPTION

VGA Front End

The NT68520 provides a built-in video pre-amplifier, a clock-recovery circuit and an analog-to-digital converter to effectively save the cost of the required external expensive Pre-amp and ADCPLL.

The pre-amplifier circuit is used to adjust the gain (Contrast) of input video amplitude and shift the DC offset voltage (Brightness).

The clock-recovery circuit consisting of a high-speed phase lock loop (PLL) is used to generate the clock to sample analog RGB data. This circuit is locked to the HSYNC of the incoming video signal.

The analog-to-digital converter (ADC) transfers the input analog RGB video to digital output data with each color 8-bit resolution.

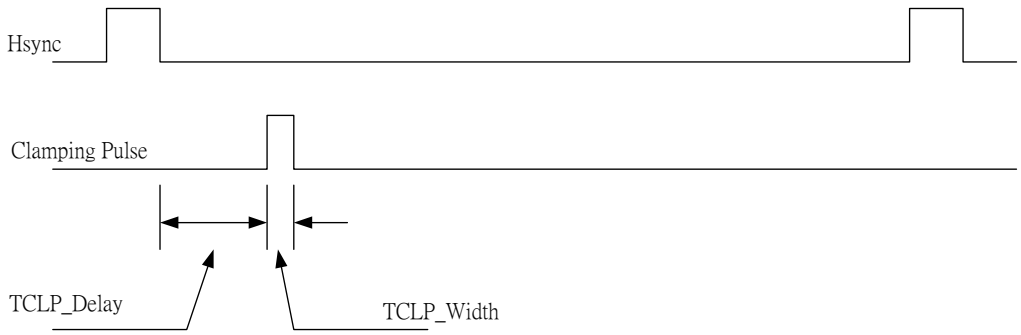
Pre-amplifier Unit

RIN/GIN/BIN are high-impedance input pins that accept the RED, GREEN, and BLUE channel graphics signals. They accommodate input signals ranging from 0.5V to 1.0V full scale. Signals should be AC-couple to these pins.

Due to AC coupling, clamping pulse is needed to define the time during which the input signal is clamped to ground, establishing a black reference. Typically, the clamping pulse is defined during the back porch period of the graphics signal. The NT68520 generates the clamping pulse internally and the position and duration are programmable. Clamping pulse-starting position is defined in register 0B[3:0], and pulse width is defined in 0B[7:4].

T_{CLP_Delay} = Reg0B[3:0] * CKOUT

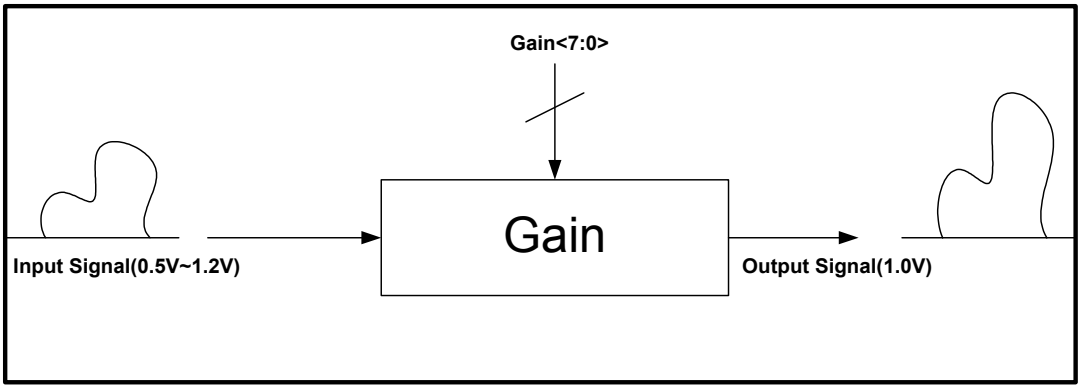
T_{CLP_Width} = Reg0B[7:4] * CKOUT



The NT68520 has three independent variable gain amplifiers for each channel with input

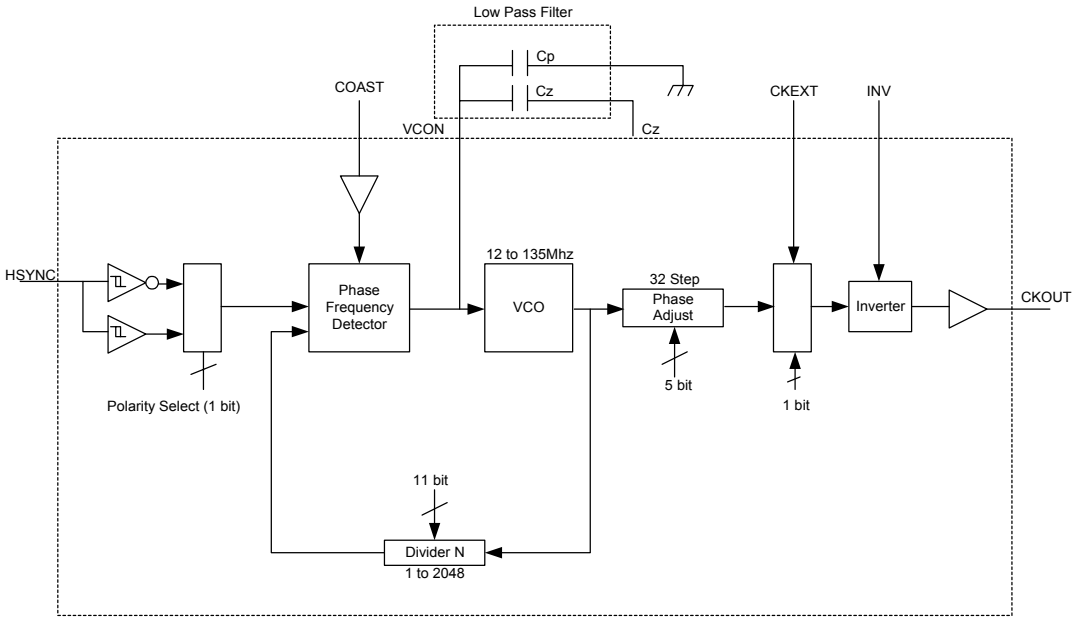
signal ranging from 0.5V to 1.0V（p-p）, the ADC's full-scale input level is 1V（p-p）. Three independent registers are used to adjust the signal level (gain), the relation between the gain and register value is as follows:

Gain = 0.8 + 1.2/ 255 * Gain <7:0>



Phase-locked loop

The internal PLL locks to the HSYNC input (frequency range 15~100 KHz) and derives a sampling clock (CKOUT) to internal ADC. The bandwidth of PLL is from 16 MHz to 135 MHz.



PLL diagram

Divider

The 11-bit value of Divider supports division ratios from 1 to 2048. The higher the value loaded in this register, the higher is the resulting clock frequency with respect to a fixed Hsync frequency. Users should program the corrective Divider value with respect to the incoming video frequency. An incorrectly set Divider value will usually produce one or more vertical noise bars on the display. The greater the error, the greater the number of bars produced.

CKEXT

This pin may be used to provide an external clock to the internal ADC in place of the clock internally generated from Hsync. When an external clock is used, all other internal functions are operated normally. When unused, this pin should be tied through a 10K resistor to ground.

COAST

This input is used to stop the pixel clock generator synchronizing with Hsync and continue producing a clock at its current frequency and phase. This is useful when processing composite sync that fails to produce horizontal sync pulses in the vertical interval.

Analog-to-Digital Converter

The ADC is 8-bit resolution for each R/G/B channel and maximum clock frequency is 135 MHz. The ADC's input range is 1V(p-p) full-scale.

There is one over-range bit for each channel (ROR、GOR and BOR). It will be set to '1' when the signal is over the ADC's full-scale range.

There is one under-range bit for each channel (RUR、GUR and BUR). It will be set to '1' when the signal is under the ADC's black level.

The phase adjustment for R/G/B as the same time to ensure signal is correctly sampled by sampling clock.

CAPTURE INTERFACE

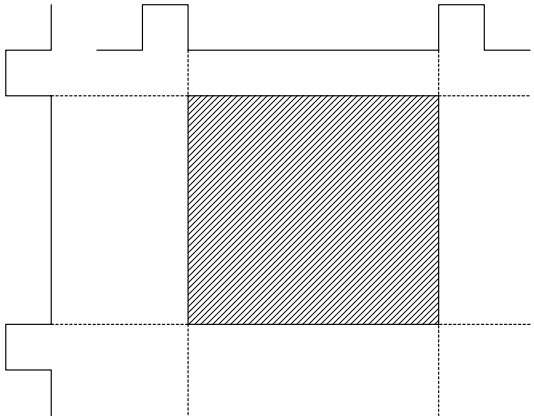
The function of Capture Interface is to provide the interface between NT68520 and external input devices. It can process non-interlaced and interlaced RGB graphic input and digital YUV video input. It also contains the built-in YUV to RGB color space converter.

Users should select the video input source (YUV or VGA) and the polarity of external control signal, then program the H/V to capture size registers to indicate the display area.

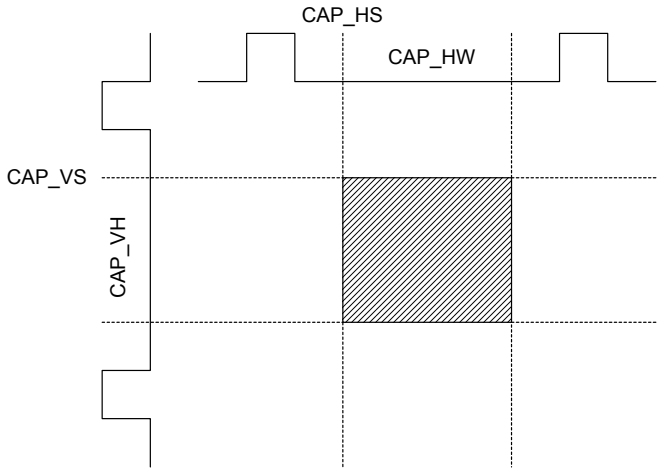
Auto Tune

Auto Tune function includes Auto Gain, Auto Position, and Auto Phase. With such auto

adjustment support, it is possible to measure the correct phase, frequency, gain, and offset of ADC. The horizontal and vertical back porches of input image and the horizontal and vertical active regions can also be measured.

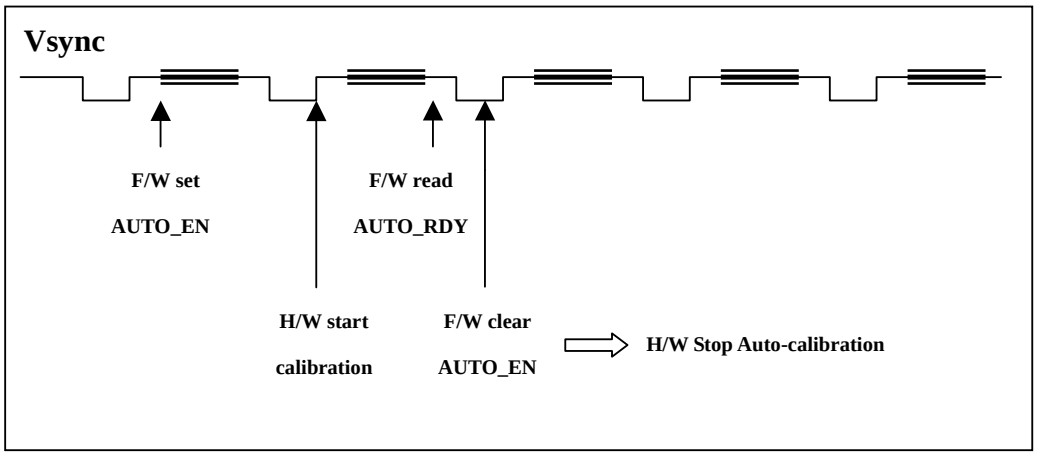


AUTO_DAE=0

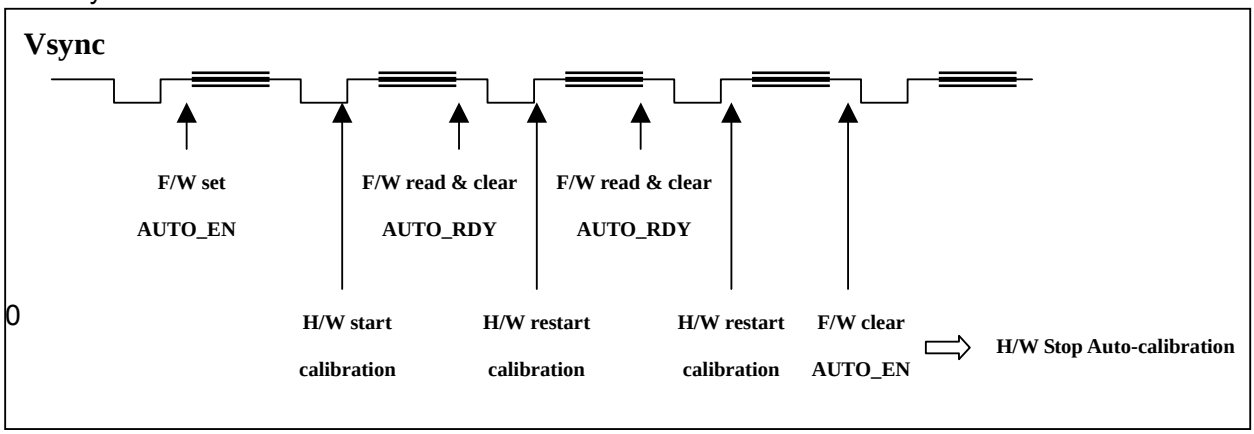


AUTO_DAE=1

One-cycle calibration



Multi-cycle Calibration



Auto Gain

Gain value is the Minimum or Maximum pixel value within a specified input image region for each RGB channel. This function is useful for measuring the noise margin of input video or for auto-contrast calibrating by adjusting ADC' s offset and gain.

Programming Steps:

1. Assign the capture area
2. Enable the Auto Gain function
3. Waiting for AUTO_RDY bit
4. Read the Max/Min result

Auto Position

The NT68520 provides the Horizontal/Vertical back porch and active region information. Users can use these values to set input capture registers to aid centering the screen automatically, and adjust the ADCPLL's divider value to figure out the correct input pixel frequency.

If the YUV input is enabled, the Auto Position will detect the video back-porch and active region values according to the YUV_HREF input signal instead of the RGB input data.

Programming Steps:

1. Specify an area covering the back porch of input video.
2. Enable the Auto Gain function.
3. Get the max R/G/B value.
4. Set the R/G/B Noise Margin value.
5. Enable the Auto Position function in Single mode.
6. Wait for Ready bit.
7. Read the detected value.

Auto Clock

By setting the H Active Reference Count value and getting the Auto Position result, it is easy to get the frequency of input pixel clock.

Programming Steps:

1 ~ 4. It is the same as above.

5. Set the H Active Reference Count value.

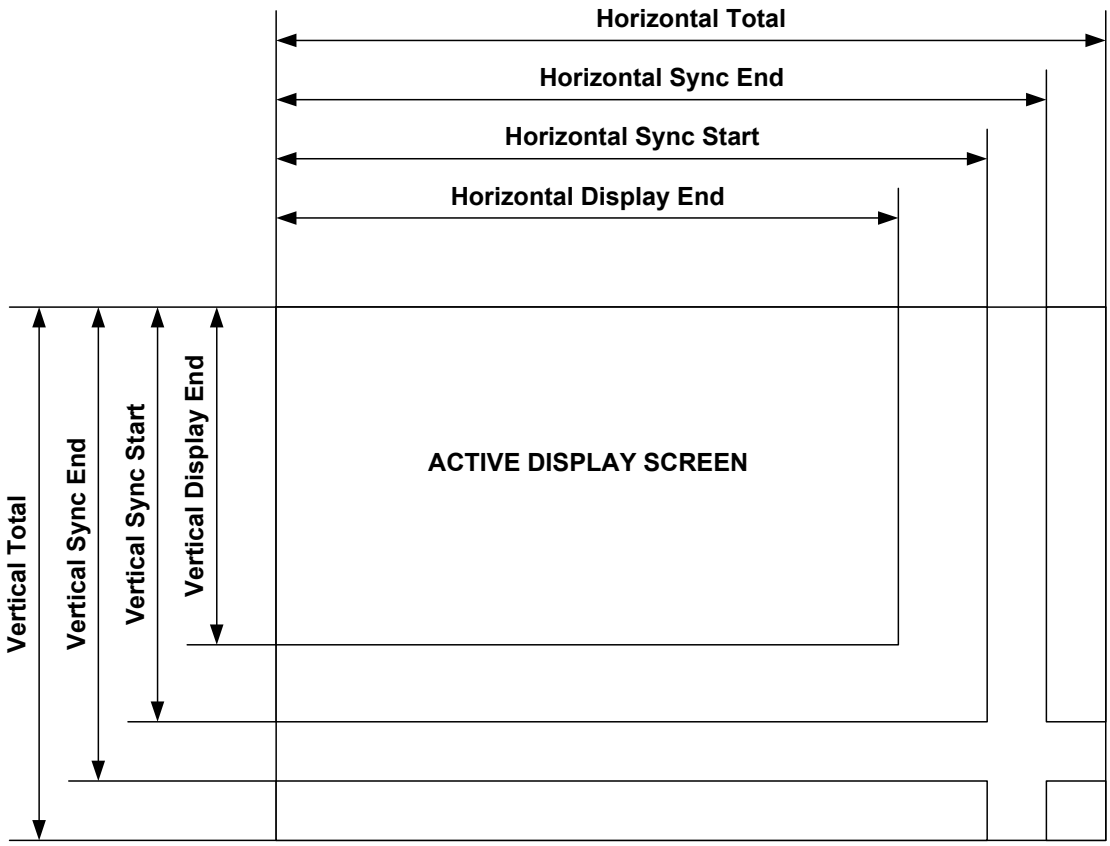
Ex: If the input video resolution is 800x600, then program the H Active Reference Count register with 800 values.

6. Enable the Auto Position function in Burst mode.
7. Wait for Ready bit.
8. Read the Status Register [3:2] to decide whether to increase or decrease the ADCPLL's divider value.
9. If Status Register [3:2] = 01 (Detected H width = H Reference Count), it means the correct input pixel clock is obtained.

DISPLAY INTERFACE

The NT68520 display interface supports a single (24-bit) or a dual (48-bit) pixel out format and a 6-bit/color or 8-bit/color LCD panel. The built-in internal PLL locking to the reference clock generates all of the display timing to various LCD panels.

The NT68520 also provides the programmable display driving capacity to reduce EMI influence as well as programmable clock delay to compensate clock skew.



VIDEO PROCESSOR

A video processor includes Interpolation Control, RGB Gain Control, RGB Offset Control, Dithering Control, and Gamma Correction Control.

The NT68520's enhanced interpolation method makes the zoomed display image look smoother and more comfortable.

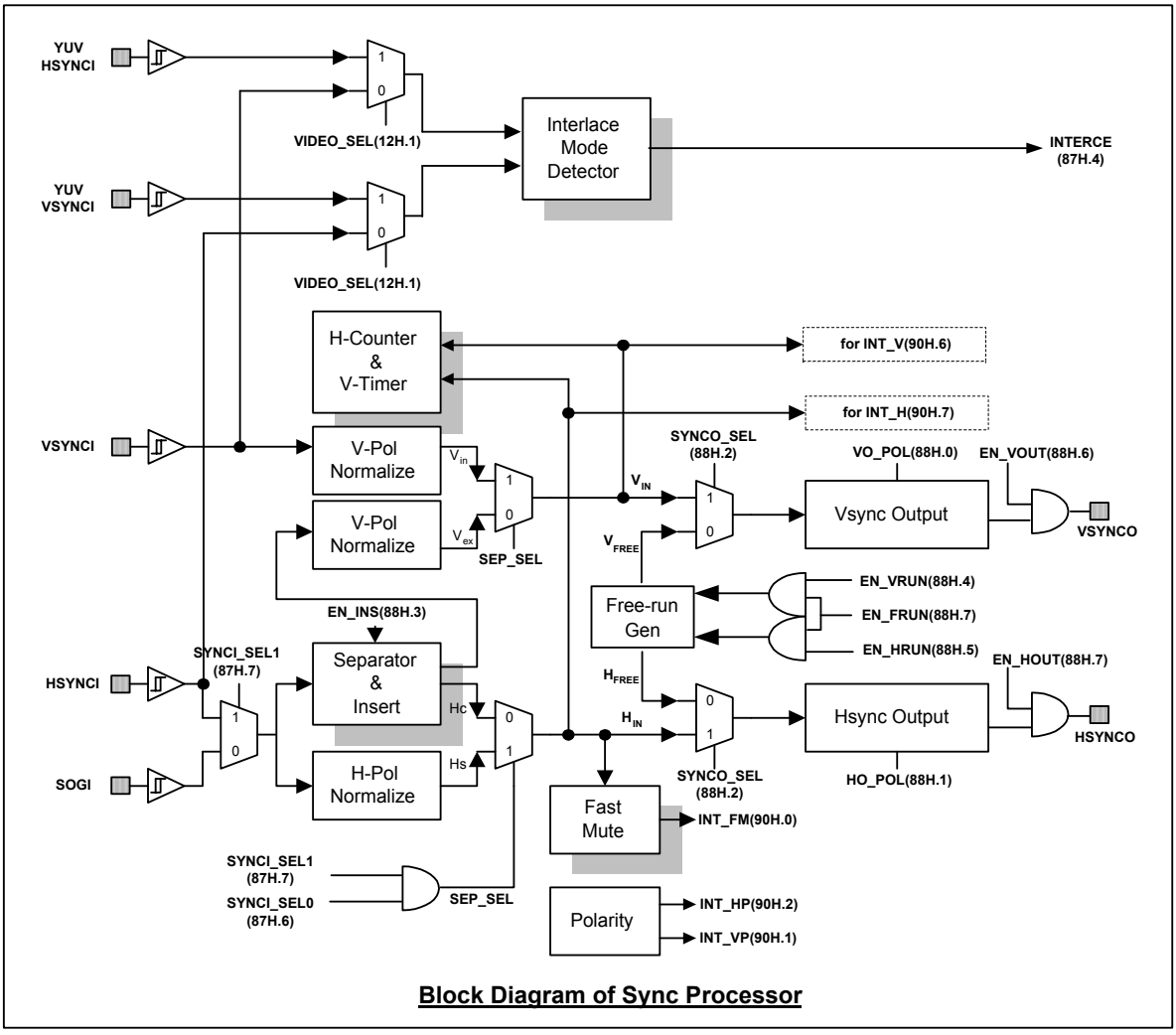
Users can adjust the RGB Gain (Contrast) and RGB Offset (Brightness) by the registers in the ADCPLL block, or registers in the Video processor block. But for YUV video input, it is suitable to adjust Contrast and Brightness here.

Dithering function can provide 16.7 million color spaces for the 6-bit/color panel. It is recommended to open the dithering function when a 6-bit panel is used.

Sync Processor

The architecture of the sync processor is shown in the **Sync Processor Block Diagram.** The functions of the modules include polarity detection, horizontal frequency counter, vertical frequency counter, and polarity controllable **HSYNCO** and **VSYNCO** outputs. It can accept various input sources, such as separate sync, composite sync, and

Sync-On-Green. The **SYNCI_SEL1/0** bit in **Sync Input Control** register will determine the type of the input sync sources. All HSYNCI, VSYNCI, and SOGI inputs have internal Schmitt trigger to improve noise immunity.



Block Diagram of Sync Processor

Sync Inputs

The video sync signals input from the pins HSYNCI, VSYNCI, and SOGI. All VSYNCI, HSYNCI and SOGI pins have Schmitt Trigger and digital filter to improve noise immunity. Any pulse shorter than 125ns is regarded as a glitch and ignored.

SYNCI_SEL 1	SYNCI_SEL 0	Sync Source
0	-	Composite Sync from SOGI
1	0	Composite Sync from HSYNCI

1	1	Separate Sync from HSYNCI/VSYNCI

Frequency detection

Vsync counter: VCNT [13:0], the 14-bit READ ONLY register, contains information of the Vsync frequency. An internal counter counts the numbers of 8us pulse between two VSYNC pulses. When a next VSYNC signal is recognized, the counter is stopped and the VCNT register latches the counter value and then the counter counts from zero again for evaluating the next VSYNC time interval. The counted data can be converted to the time duration between two successive Vsync pulses by timing 8 us. If no VSYNC comes in, the counter will overflow and set the VCNTOV bit (in VCNT_HB register) to HIGH. Once the VCNTOV is set to HIGH, it will remain unchanged until the next counter cycle is completed for its update. That means the VCNTOV bit will be updated every Vsync Counter cycle. It is necessary for various applications to provide various overflow time intervals. They are selectable as shown in the following table.

VOV_SEL1	VOV_SEL0	Time Interval
0	0	32.768ms
0	1	65.536ms
1	0	98.304ms
1	1	131.072ms

Hsync counter: If the **HGATE_SRC** bit is set to Low, the internal counter counts the Hsync pulses between two Vsync pulses. The HCNT [11:0] control registers contain the numbers of Hsync pulse between two Vsync pulses. These data can determine if the Hsync frequency is valid or not to determine the accurate video mode. The system supports two other options of intervals for users to count the frequency of Hsync pulses. If users set the HGAT_SRC and the HGATE_TME bits properly, the internal counter counts the Hsync pulses during this system defined time interval. The time interval is defined below:

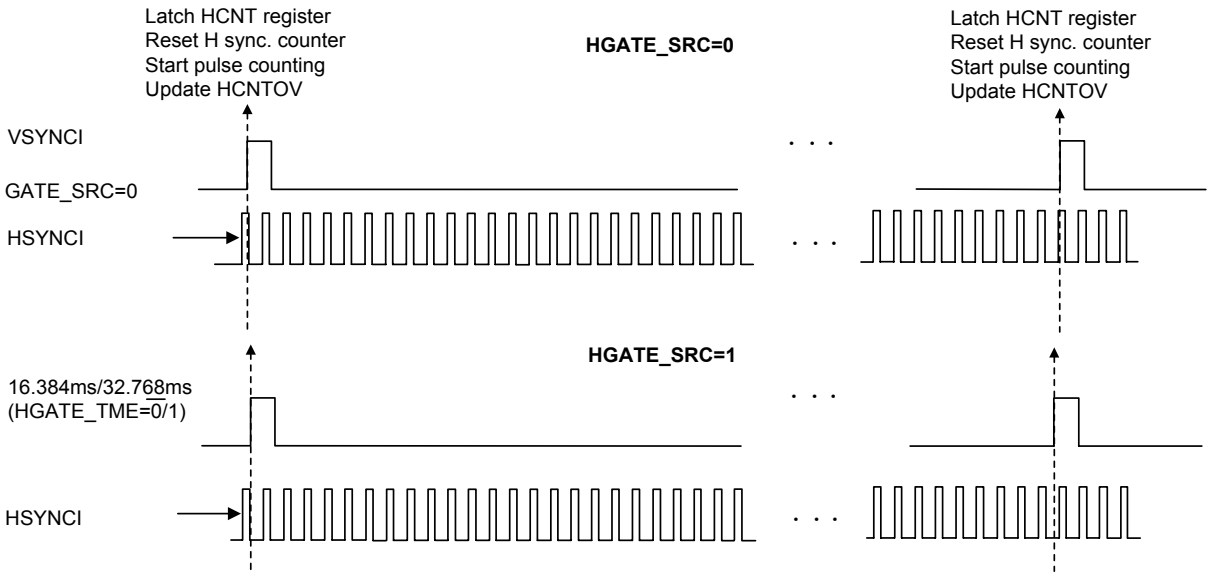
HGATE_SRC	HGATE_TME	Gate Time
0	-	Vsync Period
1	0	16.384 ms

1	1	32.768 ms

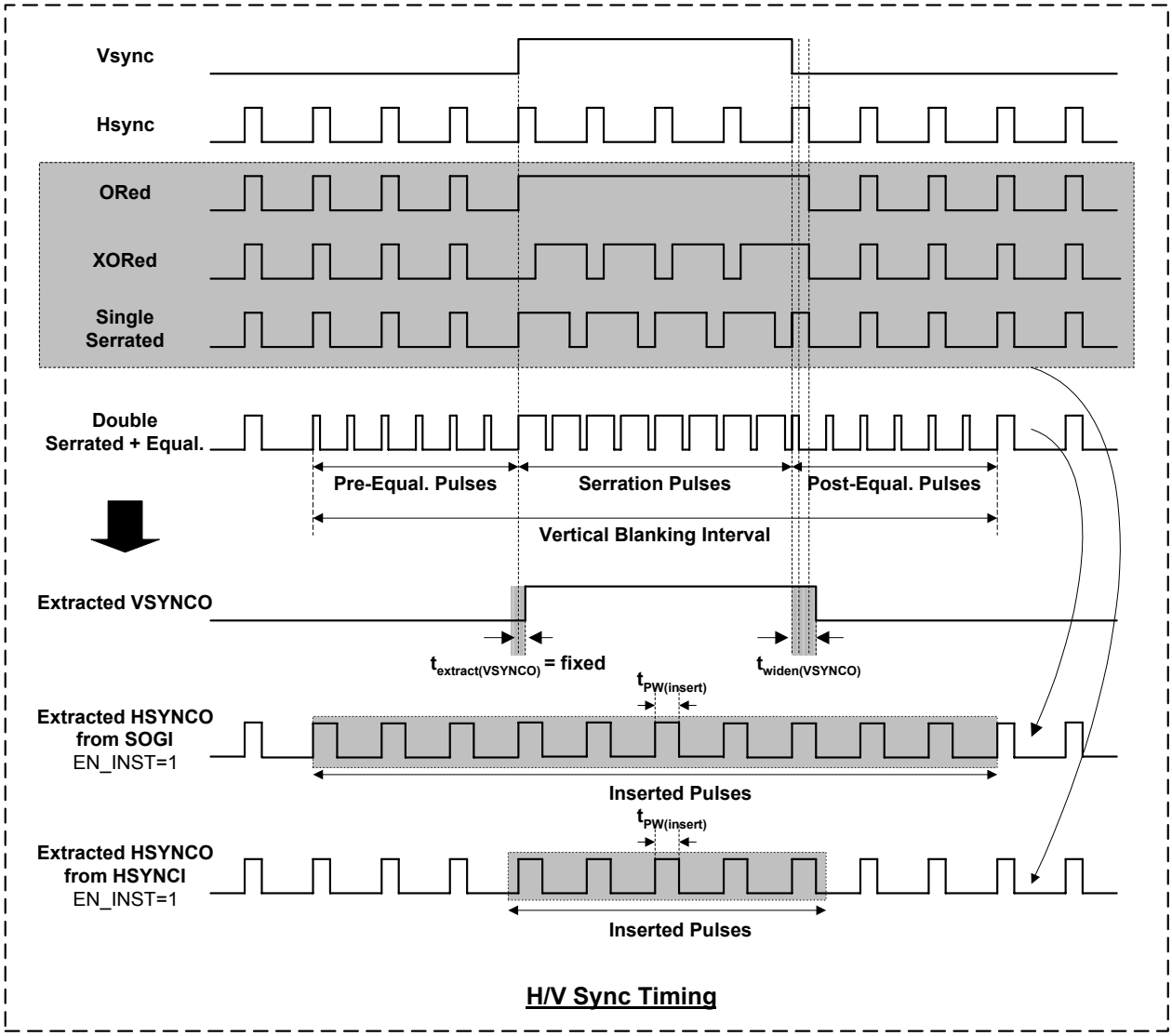
After system reset, this gate interval source will be disabled and the contents of the **HGATE_SRC** bits are '0'. When this function is disabled, the HCNT_LB/HB counter is working on the VSYNC pulse.

Latching the Hsync counter: The counted value will be latched by the HCNT_HB/LB registers which are updated by Vsync pulse or user's selected time interval. If the counter overflows, the HCNTOV bit (in HCNT_HB register) will be set to HIGH. It will not change until the next counter cycle is completed to update it. That means the HCNTOV bit will be updated every Gate cycle of Hsync counter.

All counters are with 2-lay content latches for counting sync period/frequency, so users will get stable counter results even at the latch transient.



Extract Vsync from Composite/SOG Signal



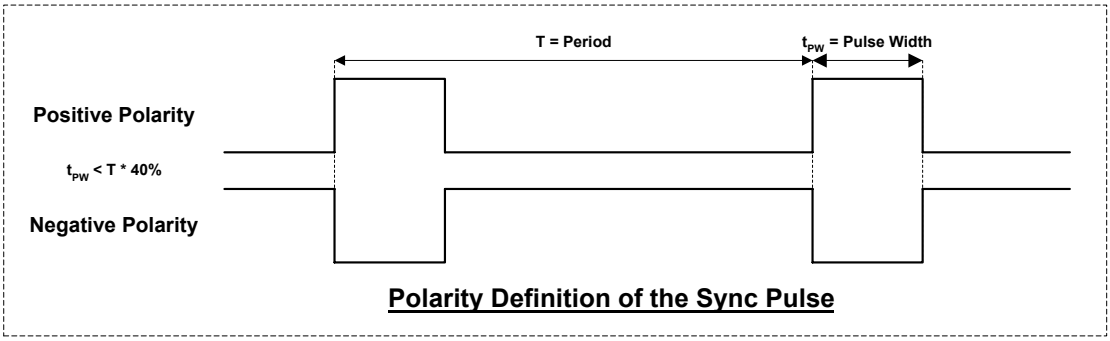
H/V Sync Timing

Polarity Detection

The sync polarity detection circuit will measure the length of high period of sync and the length of the low period of sync. If the length of the low period is longer than **60%** of the input sync period, the input polarity bit (**HI_POL** or **VI_POL**) will be one, indicating a positive polarity. If the length of the low period is shorter than **40%** of the input sync period, the input polarity will be zero, indicating a negative polarity. The specifications of the polarity detection circuit are listed below.

Spec. Table of H/V Polarity Detect Unit

$f_{VSYNC (SEP)}$	Vsync Frequency from Separate VSYNCI input for Sync Processor	15	-	250	Hz	Vsync Duty Cycle = 40%
$t_{VPW(SEP)}$	VSYNC input Pulse Width of Separate SYNC	0.150	-	32000	us	Vsync Duty Cycle < 40%
$t_{VPW(COMP)}$	VSYNC input pulse width of Composite/SOG SYNC	0.150	-	2000	us	Vsync Duty Cycle < 40%
f_{HSYNC}	Hsync Input Frequency	15	-	250	KHz	Hsync Duty Cycle = 40%
$t_{HPW(SEP)}$	HSYNC input Pulse Width of Separate-Type SYNC	0.150	-	85	us	Hsync Duty Cycle < 40%
$t_{HPW(COMP)}$	HSYNC input Pulse Width of Composite/SOG SYNC	0.150	-	20.8	us	Hsync Duty Cycle < 40%

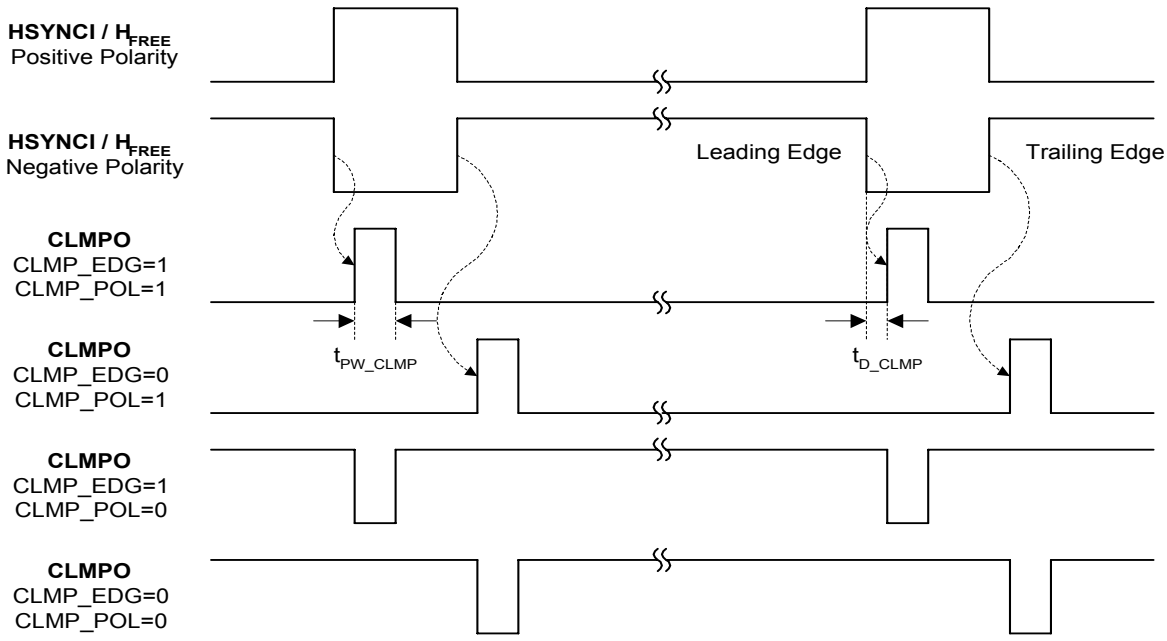


Polarity Definition of the Sync Pulse

Clamp Pulse Output

A block circuit called **clamp pulse generator** generates clamp pulse on the **CLMPO**, and outputs it to the video Pre-Amplifier for DC restoration. There are two input trigger sources of the clamp generator, one is the signal **HSYNCI** from separator and another is **H_{FREE}** from the internal free-run block. If the bit **SYNCO_SEL** is 1 then the Hin input source will be selected, otherwise the H_{FREE} will be selected. The polarity and the trigger edge of the CLMPO can be selected by using bit CLMP_POL and bit CLMP_EDG respectively. The trigger delay of the CLMPO (td_clmp) is less than **50ns**. It is a fixed delay and independent from the input video timing. The output transient of the CLMPO will not cause any crosstalk and phase jitter. The pulse width of the CLMPO output may be selected by bit **CLMP_PW0** and bit **CLMP_PW1**. Refer to the description of the CLMP_REG for details.

Clamp Pulse Timing



Clamp Pulse Timing

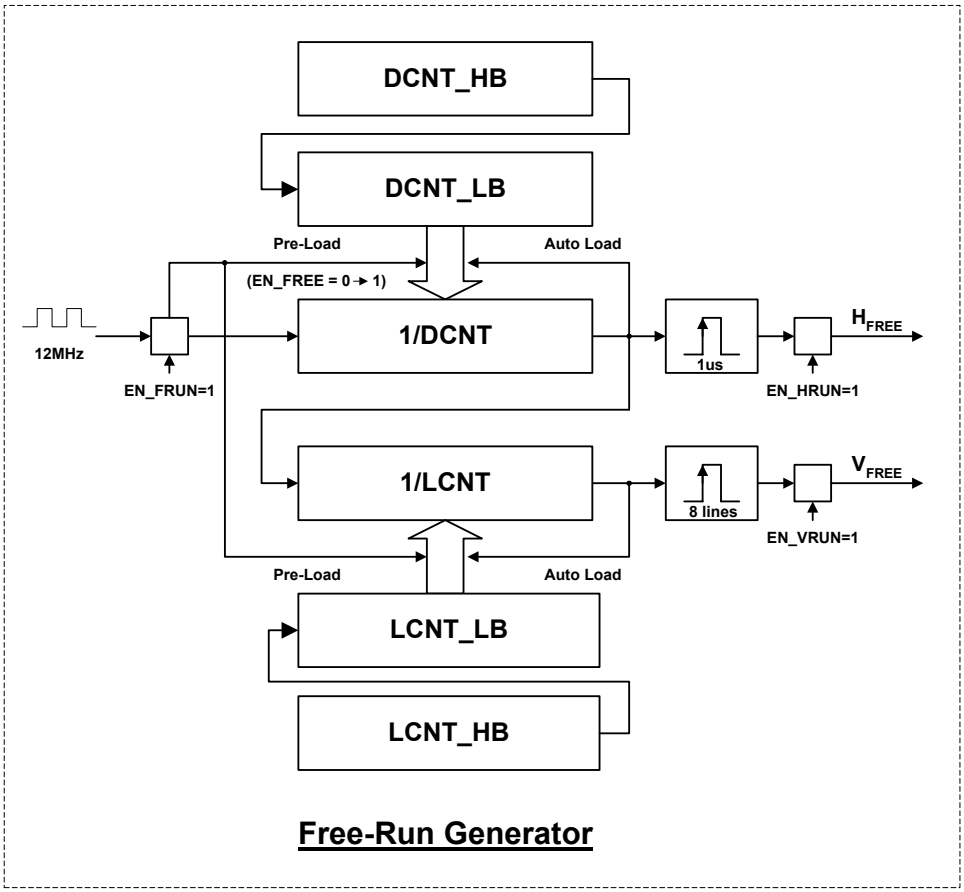
Free Running

This Block can generate various free-running outputs to satisfy various application requirements. The pulse width of the H_{FREE} output is fixed to **1us** and the V_{FREE} is **8 lines**. Users can properly set the contents of the dot counters, DCNT_HB and DCNT_LB, to get the required frequency of the H_{REEE}, and set the contents of the line counters, LCNT_HB and LCNT_LB, to get the frequency of the V_{FREE}. Refer to the descriptions of the free-run registers DCNT_HB, DCNT_LB, LCNT_HB, and LCNT_LB for details. Refer to the descriptions of the DCNT register and the LCNT register for obtaining user's required frequencies in details.

The **EN_FRUN** bit can gate the 12MHz clock source to disable this block function and to save power consumption. The previous values will be preloaded into the DCNT/LCNT counters from the DCNT_HB, LB / LCNT_HB, LB at the transient of EN_FRUN from 0 to 1. Users also can disable the H/V free run output by clearing the EN_HRUN / EN_VRUN.

When you want to set the H/V free-running frequency, remember to set the high byte

content registers (DCNT_HB, LCNT_HB) first, the H/V frequency will change after you set the low byte contents registers (DCNT_LB, LCNT_LB).



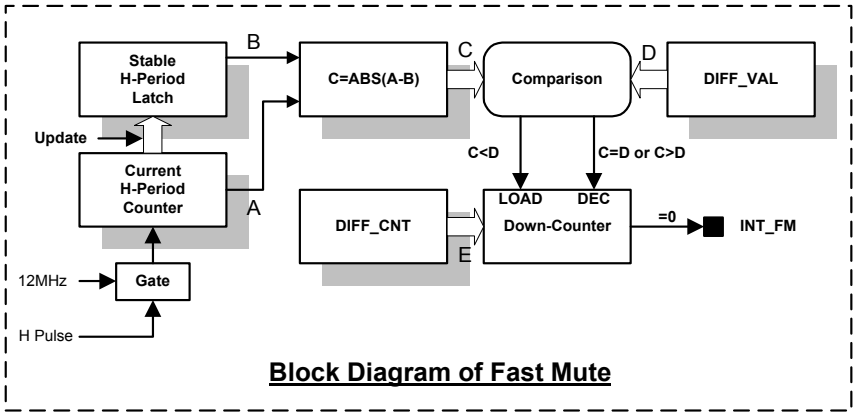
Free-Run Generator

Note：The Pulse width of the H_{FREE} is 1us, and that means it is equal to 12 dots under 12MHz OSC.

Fast Mute

1. The block generates a fast mute interrupt, **INT_FM**, to indicate an actable state of horizontal frequency. The operations of this block are A H-Period Counter counts the 12MHz pulse number within a period of the horizontal sync, and gets the current value **A**
2. The previous stable H-Period Latch held the previous counter value **B.**
3. Subtract or obtains a difference **C** from **A** and **B**, then B will be replaced with A for updating the next previous value.
4. **C** is compared with the difference boundary value **DIFF_VAL** written by user.

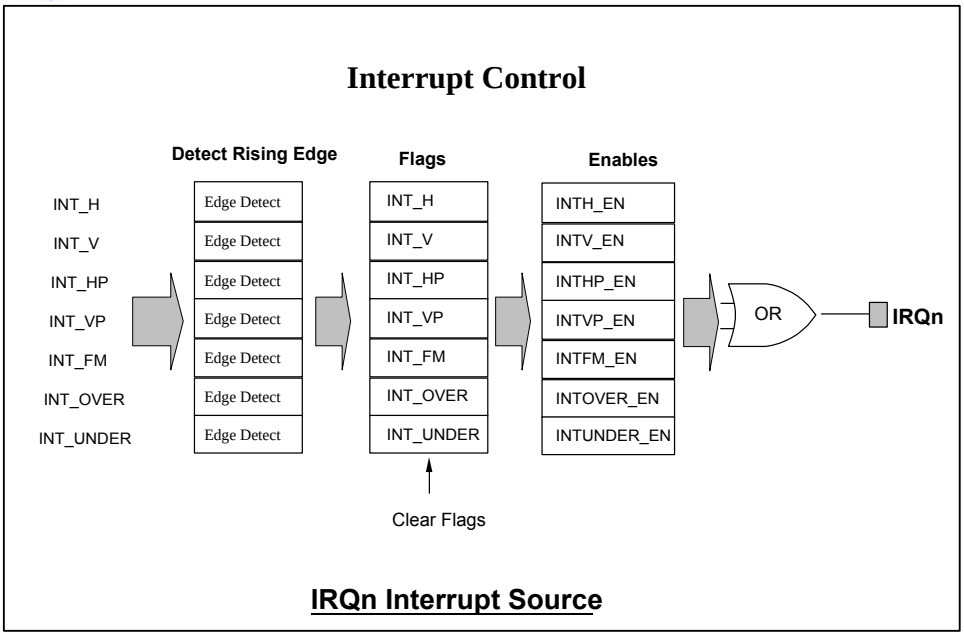
5. The result C<D loads the contents of the **DIFF_CNT**, value **E**, to the Down-Counter to indicate the Hsync input is under a stable condition. It does not affect the flag **INT_FM**.
6. The Down-Counter will decrease its content if the comparison result is C>D or C=D.
7. The flag INT_FM in the Interrupt Flag register will be set to 1 if the content of the Down-Counter is decreased to zero, then an **INT_FM** interrupt will occur when the enable bit **INT_FM** in the Interrupt Enable register is enabled.



Block Diagram of Fast Mute

IRQn Interrupt Sources

The NT68520 provides an interrupt request output pin IRQn. The following figure shows the detailed structure of the IRQn sources.



INTHV_IRQ	Meaning	Action
INT_HP	H-Polarity Change INT	It will be activated when the Input Polarity of Hsync changes.
INT_VP	V-Polarity Change INT	It will be activated when the Input Polarity of Vsync changes.
INT_FM	Fast-Mute INT	It will be activated when the Fast-Mute block detects an actable Hsync period.
INT_H	Hsync Edge INT	It will be activated when the Hsync edge is matched with the selected trigger edge.
INT_V	Vsync Edge INT	It will be activated when the Vsync edge is matched with the selected trigger edge.

OSD Function

The NT68520 supports internal OSD with the following features:

1. Max frame size 320 font (640-byte SRAM)
2. 128 ROM Font, 64 RAM Font (12-dot x 18-dot for each font)
3. Four windows Control
4. Horizontal/Vertical zoom control
5. 16 palettes with 5-bit resolution for each R/G/B color
6. Shadow/Border/Blinking effect

7. Translucent effect

OSD Palette Format

15	14:10	9:5	4:0
Reserved	R	G	B

OSD Code Format

7:0
Font Index

OSD Attribute Format

7:5	4:2	1	0
FG[2:0]	BG[2:0]	Mix	Blink

FG[2:0]: Foreground color palette index LSB 3 bits (MSB in RegABH[0])

BG[2:0]: Background color palette index LSB 3 bits (MSB in RegABH[1])

Mix: 0- Normal

1- Translucent ((Display+OSD_BG)/2)

BG : 0- Font will be background transparent

Blink: 0- No blinking

1- Blinking

DPLL Clock Control

The NT68520 contains one PLL (Bandwidth 160MHz), each for SDRAM timing generator and Display timing generator. Users should carefully program the right divider value for normal operations.

***Formula*:**

F*out* = ((N+2) x F*ref)* / (M+2)

F*ref* = 12 MHz

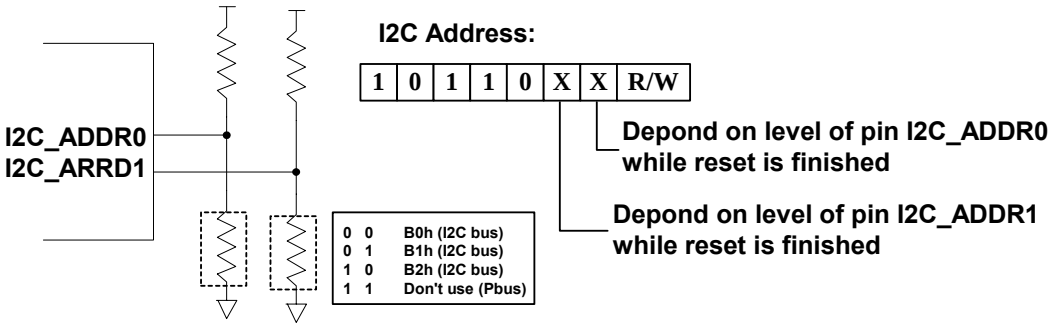
MCU Interface

The NT68520 supports two wires of I2C bus and one IRQ output to communicate with MCU. The I2C data rate is up to 400K bits/s. The NT68520's I2C address can be selected in the range of B0~B5, the value of the address bit 1/2 depends on the level of pin I2C_ADDR0/I2C_ADDR1 while the NT68520 is on the reset state.

*** If both I2C_ADDR0 and I2C_ADDR1 are pulled high, the NT68520 will go into the test mode after the reset**.

e.g. :

IF the NT68520's I2C_ADDR1,I2C_ADDR2 pins are pulled up by resisters, when the reset signal is going from low to high, the value of the two pins ('1') will be latched, and then the I2C address is determined as BXh.



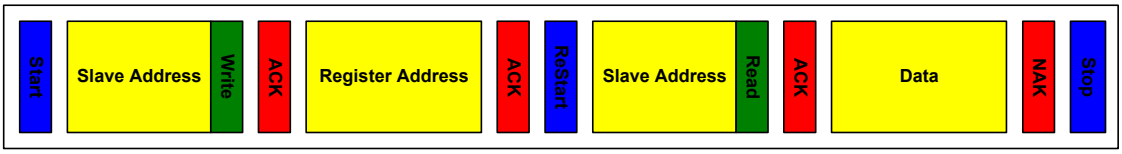
I2C Protocol

General Register R/W

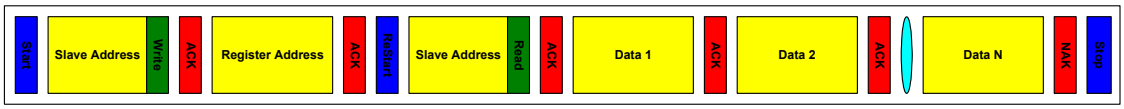
Byte Write

Sequential Write

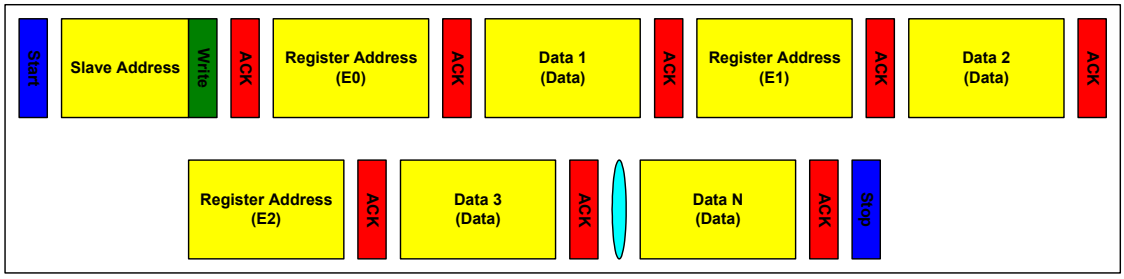
Byte Read



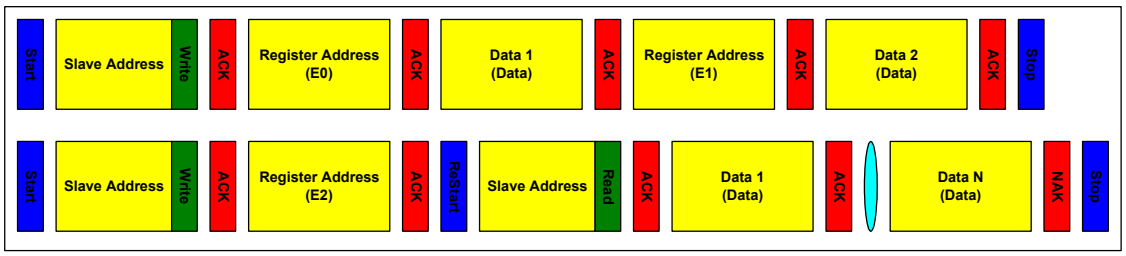
Sequential Read



Internal SRAM Write



Internal SRAM Read



Register Summary

SCALER

POWER CONTROL

00H: Power Down Control (R/W)

Bits	Name	Description
D7-1		Reserved
D0	SYS_PD	System Power Down Enable 0: Disable 1: Enable

Default：XXXX XXX0B

ADC INTERFACE

01H: ADCPLL Control (R/W)

Bits	Name	Description
D7	EN_intclp	Clamp pulse source selection 0 : External clamp pulse. 1 : Internal clamp pulse.
D6	CoastINV	ADC coast inverter 0 : Non-inverter. 1 : Inverter.
D5-4		Reserve
D3	COAST_EN	COAST function enable 0: Disable 1: Enable
D2	HI_POL_SEL	ADC Hsync input polarity select 0 : Non-invert polarity 1 : Invert polarity
D1	REGvref	ADCPLL reference voltage(2.5V) source select 0 : External (from VREF pin) 1 : Internal (from internal regulator)
D0	CAP_CLK_EN	Capture clock enable 0: Disable PLL output 1: Enable PLL output

Default：00XX 0101B

02H: Red Channel Gain Control (R/W)

Bits	Name	Description
D7-0	RGAIN[7:0]	The gain range from 0.8 to 2.0 for R-channel, the register is defined by 8-bits to produce 1V(p-p) output signal for ADC input. R_{Gain} = 0.8 + 1.2/255 * D[7:0]

Default：0000 0000B

03H: ADC Phase Control (R/W)

Bits	Name	Description
D7	PU_Amck1	1= Power-up ADC clock generator.
D6	PU_Rvga1	1= Power-up R channel VGA circuit.
D5	PU_Radc1	1= Power-up R channel A2D converter.
D4-0		Reserve

Default：1110 0000B

04H: Green Channel Gain Control (R/W)

Bits	Name	Description
D7-0	GGAIN[7:0]	The gain ranges from 0.8 to 2.0 for the G-channel, the register is defined by 8-bits to produce the 1V(p-p) output signal for ADC input. G_{Gain} = 0.8 + 1.2/255 * D[7:0]

Default：0000 0000B

05H: CKBO Channel Phase Control (R/W)

Bits	Name	Description
D7	PU_Omck1	1= Power-up CKBO clock generator.
D6	PU_Gvga1	1= Power-up G channel VGA circuit.
D5	PU_Gadc1	1= Power-up G channel A2D converter.
D4-0	Oph[4:0]	The Phase Adjust Control is defined by 5-bits, and the total step is 32 for phase shift （360°/ 32Step = 11.25°/Step）

Default：1110 0000B

06H: Blue Channel Gain Control (R/W)

Bits	Name	Description
D7-0	BGAIN[7:0]	The gain ranges from 0.8 to 2.0 for B-channel, the register is defined by 8-bits to produce 1V(p-p) output signal for ADC input. B_{Gain} = 0.8 + 1.2/255 * D[7:0]

Default：0000 0000B

07H: VGA Control (R/W)

Bits	Name	Description
D7		Reserve
D6	PU_Bvga1	1= Power-up B channel VGA circuit.
D5	PU_Badc1	1= Power-up B channel A2D converter.
D4-2		Reserve
D1	CALDIS	VGA DC offset adjust 0 : Auto adjust. 1 : User adjust.
D0	DRVCTL	VGA output driver 0 : Normal drive. 1 : Strong drive.

Default：X11X XX00B

08H: Reserve (R/W)

Bits	Name	Description
D7-0		Reserved

Default：XXXX XXXXB

09H: ADC PLL Divider Value - High Byte (R/W)

Bits	Name	Description
D7-3		Reserved
D2-0	DIV[10:8]	The high byte[2:0] of PLL divider value. Write this register will transfer the data of double-buffered register 0AH to the actual position. N divider = Divider<10:0> + 1

Default：XXXX X101B

0AH: ADC PLL Divider Value - Low Byte (R/W)

Bits	Name	Description
D7-0	DIV [7:0]	The low byte[7:0] of PLL divider value. The register is double-buffered. N divider = Divider<10:0> + 1

Default：0100 0000B

0BH: Clamp Pulse Control (R/W)

Bits	Name	Description
D7-4	Width[3:0]	Clamp pulse width control, 0~15 pixel clocks width.
D3-0	Dly [3:0]	Clamp pulse starting position control, 0~15 pixel clocks away from trailing edge of Hsync pulse, 0 maps to the first pixel.

Default：0101 0101B

0CH: VCO Gain Control (R/W)

Bits	Name	Description
D7-6	Hfrange[1:0]	Frequency range 00 : 10~40 Mhz; Kvco~15MHz/V 01 : 37~64 Mhz; Kvco~30Mhz/V 10 : 59~106 Mhz; Kvco~60Mhz/V 11 : 97~167 Mhz; Kvco~100Mhz/V
D5-4	HICP[1:0]	Charge pump current 00 : 100uA 01 : 200uA 10 : 400uA 11 : 700uA
D3-2	RCZ[1:0]	PLL Low filter internal resister 00 : 8K 01 : 4K 10 : 2K 11 : 1K

D1-0		Reserved

Default：0100 00XXB

0DH: Reserve(R/W)

Bits	Name	Description
D7		Reserved

Default：XXXX XXXXB

0EH: ADC Status (R)

Bits	Name	Description
D7-6		Reserved
D5	BUF	ADC B-channel under range flag. 0: No under range 1: Under range
D4	GUF	ADC G-channel under range flag. 0: No under range 1: Under range
D3	RUF	ADC R-channel under range flag. 0: No under range 1: Under range
D2	BOR	ADC B-channel over range flag. 0: No over range 1: Over range
D1	GOR	ADC G-channel over range flag. 0: No over range 1: Over range
D0	ROR	ADC R-channel over range flag. 0: No over range 1: Over range

Default：XXXX XXXXB

0FH: Red Channel DC Shift Control (R/W)

Bits	Name	Description
D7-5		Reserved
D4-0	Rsf [4:0]	Control the R channel DC shift value to compensate the color excursion. MSB is sign bit. 00000 ~ 01111 -> 0 ~ 15 11111 ~ 10000 -> 0 ~ -15 (1's complement)

Default：XXX0 0000B

10H: Green Channel DC Shift Control (R/W)

Bits	Name	Description
D7-5		Reserved
D4-0	Gsf [4:0]	Control the G channel DC shift value to compensate the color excursion. MSB is sign bit. 00000 ~ 01111 -> 0 ~ 15

		11111 ~ 10000 -> 0 ~ -15 (1's complement)

Default：XXX0 0000B

11H: Blue Channel DC Shift Control (R/W)

Bits	Name	Description
D7-5		Reserved
D4-0	Bsf[4:0]	Control the B channel DC shift value to compensate the color excursion. MSB is sign bit. 00000 ~ 01111 -> 0 ~ 15 11111 ~ 10000 -> 0 ~ -15 (1's complement)

Default：XXX0 0000

CAPTURE INTERFACE

12H: Capture Interface Control (R/W)

Bits	Name	Description
D7	FLASH_NOISE	Flash noise detection data port, this is a double buffer and write action by writing any data to CR1F 1:Enable flash noise detection
D6	INTE_DET_EDGE	Interlace detecting edge to work with CR94H to detect the ODD/EVEN filed 0 : Falling edge. 1 : Rising Edge. use the normalized Vsync rising edge.
D5-4		Reserve
D3	CAPCLK_POL	Invert the polarity of Pixel Clock from external YUV decoder or internal ADCPLL 1: Invert 0: Normal
D2	YUV_SWAP	Swap the Y & UV byte from external YUV decoder 1: Swap 0: Normal
D1	VIDEO_SEL	Select video input source 1: From digital YUV input port, VGA circuit entering power- down 0: From analog VGA input port, YUV circuit entering power- down
D0	CAPCLK_SEL	Capture clock source select 0: Internal clock, from PLL 1: External clock, from YUV_CLK pin

Default：X0XX 0000B

13H: Capture VGA and YUV Control (R/W)

Bits	Name	Description
D7-6		Reserved
D5-4	DEINTE_SEL [1:0]	Select the de-interlace method to display for interlace input 11: Spatial interpolation. 10: Display only even field. 01: Display only odd field. 00: Display both odd and even field.

D3	CAP_HS_SOU	Decide the Hsync pulse source referenced by capture circuit 0: From external HSYNCI pin 1: From internal re-synchronized Hs(re-sync by CAPTURE CLOCK falling edge)
D2	FIELD_POL	Invert the polarity of input Field signal. Field signal '1' is considered as ODD field 1: Invert 0: Normal
D1	FIELD_SEL	Field Indicator Source Select 1: From YUV656 decoded FIELD signal. 0: From Internal Synchronization Processor detected FIELD signal
D0	INTE_SEL	Interlace or non-interlace input select 1: Interlace 0: Non-interlace

Default：XX00 0000B

14H: Capture Vertical Start - Low Byte (R/W)

Bits	Name	Description
D7-0	CAP_VS [7:0]	Define the low byte[7:0] of the start position of the input vertical active window. This register is double-buffered by REG 15H.

Default：0000 0000B

15H: Capture Vertical Start - High Byte (R/W) and Capture Vertical Start Shift in odd/even field (works in interlace mode, CR13, D0 =1)(R/W)

Bits	Name	Description
D7	FIELD_CAP_SH_EN	Enable either ODD or EVEN field Vertical Capture Start shift 1 line 0: Enable 1: Disable
D6	FIELD_CAP_SH_SEL	Select the Field to shift vertical capture start 1: ODD field 0: EVEN field
D5	CAP_VS_SH_EN	Enable either ODD or EVEN field Capture Vertical Sync. pulse shift 1 line 0: Enable 1: Disable
D4	CAP_VS_SH_SEL	Select the Field to shift Capture Vertical Synchronization pulse 1: ODD field 0: EVEN field
D3		Reserved
D2-0	CAP_VS [10:8]	Define the high byte[10:8] of the start position of the input vertical active window. Write this register will transfer the data of double-buffered register 14H to the actual position.

Default：0000 X000B

16H: Capture Vertical Height - Low Byte (R/W)

Bits	Name	Description

D7-0	CAP_VH [7:0]	Define the low byte[7:0] of the height of the input vertical active window.

Default：0000 0000B

17H: Capture Vertical Height - High Byte (R/W)

Bits	Name	Description
D7-3		Reserved
D2-0	CAP_VH [10:8]	Define the high byte[10:8] of the height of the input vertical active window.

Default：0000 0000B

18H: Capture Horizontal Start - Low Byte (R/W)

Bits	Name	Description
D7-0	CAP_HS [7:0]	Define the low byte[7:0] of the start position of the input horizontal active window. This register is double-buffered by REG 19H.

Default：0000 0000B

19H: Capture Horizontal Start - High Byte (R/W)

Bits	Name	Description
D7-3		Reserved
D2-0	CAP_HS [10:8]	Define the high byte[10:8] of the start position of the input horizontal active window.

Default：0000 0000B

1AH: Capture Horizontal Width - Low Byte (R/W)

Bits	Name	Description
D7-0	CAP_HW [7:0]	Define the low byte[7:0] of the width of the input horizontal active window.

Default：0000 0000B

1BH: Capture Horizontal Width - High Byte (R/W)

Bits	Name	Description
D7-3		Reserved
D2-0	CAP_HW [10:8]	Define the high byte[10:8] of the width of the input horizontal active window.

Default：0000 0000B

1C: Capture Synchronous Lock Position in lines (W)

Bits	Name	Description
D7-6		Reserved
D5-4	LAST_H_CH	Change the position of the last abnormal Hsync 00 : In VFP 01 : Delay 1 line. 10 : Delay 2 line.

		11 : Delay 3 line.
D3-0	VLOCK [3:0]	Define the Lock Position in lines that display timing will be re-synchronized to capture timing in Manual Display mode

Default：0000 0001B

1C: Capture Synchronous Lock Position in lines Read Back(R)

Bits	Name	Description
D7-6		Reserved
D5-4	LAST_H_CH	Change the position of the last abnormal Hsync 00 : In VFP 01 : Delay 1 line. 10 : Delay 2 line. 11 : Delay 3 line.
D3-0	VLOCK [3:0]	Read Back Lock Position in lines in Auto Display mode

Default：XXXX XXXXB

1D: Capture Synchronous Lock Position in Pixels (W)

Bits	Name	Description
D7-0	HLOCK	Define the Lock Position in pixels of CR1D defined line that display timing will be re-synchronized to capture timing in Manual Display mode

Default：1000 0000B

1D: Capture Synchronous Lock Position in Pixels Read Back(R)

Bits	Name	Description
D7-0	HLOCK	Read back the hardware auto Lock Position in pixels of CR1D defined line in Auto Display Mode

Default：XXXX XXXXB

AUTO TUNE

1EH: Auto Calibration Control (W)

Bits	Name	Description
D7-5		Reserved
D3	AUTO_MS	Auto Gain/Position Mode Select 0: Auto Gain Mode 1: Auto Position Mode
D2	AUTO_GAIN_DA_SEL	Auto Gain Detecting Area Selection 0: Between two V-sync trailing edges. 1: Specified by Reg14H ~ Reg1BH
D1		Reserved
D0	AUTO_EN	Auto Gain/Position Start Enable 0: Disable

		1: Enable

Default：XXX0 0000B

1FH: Auto Calibration Status (R)

Bits	Name	Description
D7-4	AUTO_DIFF [3:0]	Difference between Detected H width and H Reference Count 0000(0) ~ 1111(15) = | Detected H width - H Reference Count |, Value 1111 means the difference ≥ 15
D3-2	AUTO_P_COMP [1:0]	Auto Position comparing result for comparing the H Reference Count with the detected H Active Count. It is useful for input pixel clock detection. 00: Detected H width < H Reference Count (F/W should Increase the PLL divider value) 01: Detected H width = H Reference Count 10: Detected H width > H Reference Count (F/W should decrease the PLL divider value) 11: Reserved
D1		Reserved
D0	AUTO_RDY	Auto Gain/Position ready flag. User should clear this bit after reading the status register to restart the next auto-calibration cycle. 0: Not ready 1: Ready

Default：XXXX XXXXB

1FH: Auto Calibration Status (W)

Bits	Name	Description
D7-1		Reserved
D0	CLR_RDY	Writing this register will clear AUTO_RDY bit.

Default: XXXX XXXXB

AUTO PHASE

20H: Auto Phase/Histogram Calibration Control (R/W)

Bits	Name	Description
D7-6		Reserved
D5-4	SEL_CAL_CH	Select Auto Phase or Auto Histogram calibration channels 00: R&G&B channel (Auto phase) 01: R channel (Auto Phase / Histogram) 10: G channel (Auto Phase / Histogram) 11: B channel (Auto Phase / Histogram)
D3-2	SEL_CAL_METHOD	Select Auto Phase or Auto Histogram calibration method 00: Auto Phase 01: Reserve 10: Auto Histogram method 0 (Low Bound(more than threshold value amount of pixel)), the threshold defined in CR27 11: Auto Histogram method 1 (High Bound(less than threshold value amount of pixel))

D1	BURST_MODE	Auto Phase/Histogram calibration is working in burst or single mode 0: single 1: burst
D0	AUTO_PH_EN (W)	Auto Phase/Histogram Start Enable 0: Disable 1: Enable
D0	AUTO_PH_READY(R)	Auto Phase/Histogram calibration Ready 0: Ready 1: Not Ready

Default：XX00 0000B

21H: Auto Phase/Histogram Calibration result BYTE 3 (Low Byte) (R)

Bits	Name	Description
D7-0	AUTO_PH_B3	Auto Phase/Histogram calibration result BYTE 3

Default：XXXX XXXXB

22H: Auto Phase/Histogram Calibration result BYTE 2 (R)

Bits	Name	Description
D7-0	AUTO_PH_B2	Auto Phase/Histogram calibration result BYTE 2

Default：XXXX XXXXB

23H: Auto Phase/Histogram Calibration result BYTE 1 (R)

Bits	Name	Description
D7-0	AUTO_PH_B1	Auto Phase/Histogram calibration result BYTE 1

Default：XXXX XXXXB

24H: Auto Phase/Histogram Calibration result BYTE 0 (High Byte) (R)

Bits	Name	Description
D7-0	AUTO_PH_B0	Auto Phase/Histogram calibration result BYTE 0

Default：XXXX XXXXB

25H: Auto Phase Red/Green Difference Mask (R/W)

Bits	Name	Description
D7		Reserved
D6-4	PH_G_MASK	Auto Phase Green difference mask, the difference will be masked before summation.
D3		Reserved

D2-0	PH_R_MASK	Auto Phase Red difference mask, the difference will be masked before summation

Default：0000 0000B

26H: Auto Phase Blue Difference Mask (R/W)

Bits	Name	Description
D7-3		Reserved
D2-0	PH_B_MASK	Auto Phase Blue difference mask, the difference will be masked before summation.

Default：0000 0000B

27H: Auto Histogram Threshold (R/W)

Bits	Name	Description
D7-0	AUTO_HIS_TH	Auto Histogram threshold for R/G/B in high bound or low bound modes.

Default：0000 0000B

AUTO GAIN

28H: Auto Gain Red Max Value (R)

Bits	Name	Description
D7-0	AUTO_G_RMAX [7:0]	The max red value of Auto-Gain in the specified scan area

Default：XXXX XXXXB

29H: Auto Gain Green Max Value (R)

Bits	Name	Description
D7-0	AUTO_G_GMAX [7:0]	The max green value of Auto-Gain in the specified scan area

Default：XXXX XXXXB

2AH: Auto Gain Blue Max Value (R)

Bits	Name	Description
D7-0	AUTO_G_BMAX [7:0]	The max blue value of Auto-Gain in the specified scan area

Default：XXXX XXXXB

2BH: Auto Gain Red Min Value (R)

Bits	Name	Description
D7-0	AUTO_G_RMIN [7:0]	The min red value of Auto-Gain in the specified scan area

Default：XXXX XXXXB

2CH: Auto Gain Green Min Value (R)

Bits		Description
D7-0	AUTO_G_GMIN [7:0]	The min green value of Auto-Gain in the specified scan area

Default：XXXX XXXXB

2DH: Auto Gain Blue Min Value (R)

Bits	Name	Description
D7-0	AUTO_G_BMIN [7:0]	The min blue value of Auto-Gain in the specified scan area

Default：XXXX XXXXB

AUTO POSITION

2EH: Auto Position Pixel Mask (R/W)

Bits	Name	Description
D7-0	Pixel_Mask[7:0]	Auto position pixel mask area for H-back porch.(3C H-front porch)

Default：0000 0000B

2FH: Auto Position Red Noise Margin (R/W)

Bits	Name	Description
D7-0	AUTO_P_RNM [7:0]	Define the red noise margin value for selecting between black and non-black pixels.

Default：0000 0000B

30H: Auto Position Green Noise Margin (R/W)

Bits	Name	Description
D7-0	AUTO_P_GNM [7:0]	Define the green noise margin value for selecting between black and non-black pixels.

Default：0000 0000B

31H: Auto Position Blue Noise Margin (R/W)

Bits	Name	Description
D7-0	AUTO_P_BNM [7:0]	Define the blue noise margin value for selecting between black and non-black pixels.

Default：0000 0000B

32H: Auto Position V Back-porch Count - Low Byte (R)

Bits	Name	Description
D7-0	AUTO_P_VBPC [7:0]	Auto position detected vertical start position low byte [7:0]

Default：XXXX XXXXB

33H: Auto Position V Back-porch Count - High Byte (R)

Bits	Name	Description
D7-3		Reserved
D2-0	AUTO_P_VBPC [10:8]	Auto position detected vertical start position high byte [10:8]

Default：XXXX XXXXB

34H: Auto Position V Active Count - Low Byte (R)

Bits	Name	Description
D7-0	AUTO_P_VAC [7:0]	Auto position detected vertical active height low byte [7:0]

Default：XXXX XXXXB

35H: Auto Position V Active Count - High Byte (R)

Bits	Name	Description
D7-3		Reserved
D2-0	AUTO_P_VAC[10:8]	Auto position detecting vertical active height high byte [10:8]

Default：XXXX XXXXB

36H: Auto Position H Back-porch Count - Low Byte (R)

Bits	Name	Description
D7-0	AUTO_P_HBPC[7:0]	Auto position detected horizontal start position low byte [7:0]

Default：XXXX XXXXB

37H: Auto Position H Back-porch Count - High Byte (R)

Bits	Name	Description
D7-3		Reserved
D2-0	AUTO_P_HBPC[10:8]	Auto position detected horizontal start position high byte [10:8]

Default：XXXX XXXXB

38H: Auto Position H Active Count - Low Byte (R)

Bits	Name	Description
D7-0	AUTO_P_HAC [7:0]	Auto position detected horizontal active width low byte [7:0]

Default：XXXX XXXXB

39H: Auto Position H Active Count - High Byte (R)

Bits	Name	Description
D7-3		Reserved
D2-0	AUTO_P_HAC [10:8]	Auto position detected horizontal active width high byte [10:8]

Default：XXXX XXXXB

3AH: Auto Position H Active Reference Count - Low Byte (R/W)

Bits	Name	Description
D7-0	AUTO_P_HARC [7:0]	H active reference count low byte [7:0], Comparing this counter value with the AUTO_P_HAC[10:0], it is easy to adjust the ADCPLL's divider value to get the right clock frequency.

Default：0000 0000B

3BH: Auto Position H Active Reference Count - High Byte (R/W)

Bits	Name	Description
D7-3		Reserved
D2-0	AUTO_P_HARC[10:8]	H active reference count high byte [10:8]

Default：XXXX X000B

3CH: Auto Position Pixel Mask (R/W)

Bits	Name	Description
D7-0	Pixel_Mask[7:0]	Auto position pixel mask area for H-front porch.(2Eh H-back porch)

Default：0000 0000B

3DH ~4BH: Reserved (R/W)

DISPLAY INTERFACE

4CH: Display Control (R/W)

Bits	Name	Description
D7	AUTO_SYNC_LOCK_EN	Auto Capture Synchronous Lock position stop 0: Disable 1: Enable
D6	DISP_AUTO	Decide the working mode of Display Horizontal Timing generation. 0: Manual mode. H/W automatically adjusts the VT and VFP timings, others fully depend on Reg4EH ~ Reg5DH. Capture Synchronous Lock Position = Reg1CH ~ Reg1DH 1: Auto mode. H/W automatically adjusts the HT(only once), HFP, VT, VFP. H/W automatically adjusts Capture Synchronous Lock position, but can be Disabled by 4CH(D7)
D5	DISP_AUTO_STEP_HT_EVEN_ONLY	Decide the H-total adjust value even step 0 : Disable 1 : Enable
D4	SKEW	Skew output control for double pixel display.
D3	DISP_EN	Display Enable 0: Disable. Tri-state control lines and data lines. 1: Enable
D2	DISP_CD	Display Color Depth 0: 8-bit/color 1: 6-bit/color
D1	DISP_BW	Display Bus Width 0: Double pixel 48-bit 1: Single pixel 24-bit(A group)
D0	DISP_DE	Panel DE Mode Support 0: Panel supports Sync mode, display Hs/Vs signal is at normal state 1: Panel supports DE mode, display Hs/Vs signals will be pulled LOW or HIGH, it depends on REG 61H(D1-0), if DISP_HS_POL = 0 and DISP_VS_POL = 1, then Hs is pulled to LOW, and Vs is pulled to HIGH

Default：0000 0000B

4DH: Display Mute Control (R/W)

Bits	Name	Description
D7	BYPASS	Enable the captured data by-passing the scaler 0: Normal 1: Bypass
D6	MUTE_AUTO	Mute with OSD when VGA input sync fail 0: Disable 1: Enable
D5		Reserved

D4-2	MUTE_CLR [2:0]	Select background color while Mute Data With OSD On function is selected. D4 = 1 : Output red background color D3 = 1 : Output green background color D2 = 1 : Output blue background color
D1-0	DISP_MUTE [1:0]	Display Mute Mode Select 11: Mute All (control lines and data lines set to 0) 10: Mute Data with OSD on (free running mode) 01: Mute Data (data lines set to 0) 00: Normal display

Default：0XX0 0000B

4EH: Display Vertical Total Height - Low Byte (R/W)

Bits	Name	Description
D7-0	DISP_VT [7:0]	Define the low byte[7:0] of total number in scan lines per frame

Default：0000 0000B

4FH: Display Vertical Total Height - High Byte (R/W)

Bits	Name	Description
D7-3		Reserved
D2-0	DISP_VT [10:8]	Define the high byte [10:8] of total number in scan lines per frame

Default：XXXX X000B

50H: Display Vertical Active Height - Low Byte (R/W)

Bits	Name	Description
D7-0	DISP_VAE [7:0]	Define the low byte [7:0] of vertical active end position in scan lines

Default：0000 0000B

51H: Display Vertical Active Height - High Byte (R/W)

Bits	Name	Description
D7-3		Reserved
D2-0	DISP_VAE [10:8]	Define the high byte [10:8] of vertical active end position in scan lines

Default：XXXX X000B

52H: Display Vertical Sync Start Height - Low Byte (R/W)

Bits	Name	Description
D7-0	DISP_VSS [7:0]	Define the low byte [7:0] of Vsync start position in scan lines

Default：0000 0000B

53H: Display Vertical Sync Start Height - High Byte (R/W)

Bits	Name	Description
D7-3		Reserved
D2-0	DISP_VSS [10:8]	Define the high byte [10:8] of Vsync start position in scan lines

Default：XXXX X000B

54H: Display Vertical Sync End Height - Low Byte (R/W)

Bits	Name	Description
D7-0	DISP_VSE [7:0]	Define the low byte [7:0] of Vsync end position in scan lines

Default：0000 0000B

55H: Display Vertical Sync End Height - High Byte (R/W)

Bits	Name	Description
D7-3		Reserved
D2-0	DISP_VSE [10:8]	Define the high byte [10:8] of Vsync end position in scan lines

Default：XXXX X000B

56H: Display Horizontal Total Width - Low Byte (R/W)

Bits	Name	Description
D7-0	DISP_HT [7:0]	Define the low byte [7:0] of total number in pixels per line

Default：0000 0000B

57H: Display Horizontal Total Width - High Byte (R/W)

Bits	Name	Description
D7-3		Reserved
D2-0	DISP_HT [10:8]	Define the high byte [10:8] of total number in pixels per line

Default：XXXX X000B

58H: Display Horizontal Active End Width - Low Byte (R/W)

Bits	Name	Description
D7-0	DISP_HAE [7:0]	Define the low byte [7:0] of horizontal active end position in pixels

Default：0000 0000B

59H: Display Horizontal Active End Width - High Byte (R/W)

Bits	Name	Description
D7-3		Reserved
D2-0	DISP_HAE [10:8]	Define the high byte [10:8] of horizontal active end position in pixels

Default：XXXX X000B

5AH: Display Horizontal Sync Start Width - Low Byte (R/W)

Bits	Name	Description
D7-0	DISP_HSS [7:0]	Define the low byte [7:0] of Hsync start position in pixels

Default：0000 0000B

5BH: Display Horizontal Sync Start Width - High Byte (R/W)

Bits	Name	Description
D7-3		Reserved
D2-0	DISP_HSS [10:8]	Define the high byte [10:8] of Hsync start position in pixels

Default：XXXX X000B

5CH: Display Horizontal Sync End Width - Low Byte (R/W)

Bits	Name	Description
D7-0	DISP_HSE [7:0]	Define the low byte [7:0] of Hsync end position in pixels

Default：0000 0000B

5DH: Display Horizontal Sync End Width - High Byte (R/W)

Bits	Name	Description
D7-3		Reserved
D2-0	DISP_HSE [10:8]	Define the high byte [10:8] of Hsync end position in pixels

Default：XXXX X000B

5EH: Display Drive Select 1 (R/W)

Bits	Name	Description
D7	DISP_CLK_SR	Select panel interface CLOCK slew rate 0: Fast 1: Slow
D6-4	DISP_CLK_DRV [2:0]	Select panel interface CLOCK drive strength 000: 2mA 100: 10mA 001: 4mA 101: 12mA 010: 6mA 110: 14mA 011: 8mA 111: 16mA
D3	DISP_DATA_SR	Select panel interface DATA slew rate 0: Fast 1: Slow
D2-0	DISP_DATA_DRV [2:0]	Select panel interface DATA drive strength 000: 2mA 100: 10mA 001: 4mA 101: 12mA 010: 6mA 110: 14mA 011: 8mA 111: 16mA

Default：1001 1001B

5FH: Display Drive Select 2 (R/W)

Bits	Name	Description
D7-4		Reserved
D3	DISP_HVD_SR	Select panel interface HS/VS/DE slew rate

		0: Fast 1: Slow
D2-0	DISP_HVD_DRV [2:0]	Select panel interface HS/VS/DE drive strength 000: 2mA 100: 10mA 001: 4mA 101: 12mA 010: 6mA 110: 14mA 011: 8mA 111: 16mA

Default：XXXX 1001B

60H: Display Delay Select (R/W)

Bits	Name	Description
D7-4		Reserved
D3-0	DISP_CLK_DLY [3:0]	Select panel interface CLOCK delay time, 1 ~ 16 nS (1nS/Step)

Default：XXXX 0000B

61H: Display Polarity Control (R/W)

Bits	Name	Description
D7-4		Reserved
D3	DISP_DE_POL	Display DE 0: Active High 1: Active Low
D2	DISP_CLK_POL	Display Clock 0: Normal 1: Inverted
D1	DISP_HS_POL	Display Hsync 0: Active High 1: Active Low
D0	DISP_VS_POL	Display Vsync 0: Active High 1: Active Low

Default：XXXX 0000B

62H: Display Auto Control Ready (R)

Bits	Name	Description
D7-0		Reserved

Default：XXXX XXXXB

63H ~ 66H: Reserved (R/W)

Bits		Description
D7-0	Reserved	Reserved

Default：0000 0000B

67H: Display Horizontal Total Read Back– Low Byte (R)

Bits	Name	Description
D7-0	DISP_HTRB [7:0]	Read back the low byte value of display horizontal total.

Default：XXXX XXXXB

68H: Display Horizontal Total Read Back – High Byte (R)

Bits	Name	Description
D7-3		Reserved
D2-0	DISP_HTRB[10:8]	Read back the high byte value of display horizontal total.

Default：XXXX XXXXB

VIDEO PROCESSOR

69H: Gain Control - Red (R/W)

Bits	Name	Description
D7-0	GAIN_R [7:0]	Adjust the gain of red component, step size = 2/255, 00h (0) -> 80h (1) -> FFh (2).

Default：1000 0000B

6AH: Gain Control – Green (R/W)

Bits	Name	Description
D7-0	GAIN_G [7:0]	Adjust the gain of green component, step size = 2/255, 00h (0) -> 80h (1) ->FFh (2).

Default：1000 0000B

6BH: Gain Control - Blue (R/W)

Bits	Name	Description
D7-0	GAIN_B [7:0]	Adjust the gain of blue component, step size = 2/255, 00h (0) -> 80h (1) -> FFh (2).

Default：1000 0000B

6CH: Offset Control - Red (R/W)

Bits	Name	Description
D7-0	OFFSET_R [7:0]	Adjust the offset of red component by 2's complement value, 80h (-128) -> 00h (0) -> 7Fh (127).

Default：0000 0000B

6DH: Offset Control - Green (R/W)

Bits	Name	Description
D7-0	OFFSET_G	Adjust the offset of green component by 2's complement value.

	[7:0]	80h (-128) -> 00h (0) -> 7Fh (127)

Default：0000 0000B

6EH: Offset Control - Blue (R/W)

Bits	Name	Description
D7-0	OFFSET_B [7:0]	Adjust the offset of blue component by 2's complement value 80h (-128) -> 00h (0) -> 7Fh (127).

Default：0000 0000B

6FH: Scaling and Dithering Control (R/W)

Bits	Name	Description
D7	GAMMA_EN	Enable Display Gamma Table 0 : Disable 1 : Enable
D6	GEN_GAMMA_PATTERN	Generator Gamma Adjust Pattern 0 : Disable. 1 : Enable.
D5-3		Reserved
D2	INPUT_TIME	0 : Recalibrate input timing ready (R). 1 : Recalibrate input timing enable (W).
D1	SCAL_EN	If the frequency of input video sampling clock or display clock is changed, it is needed to clear this bit to '0' then set to '1' to activate the scaling unit to accommodate the data racing.
D0	DITHER_EN	Dithering enable 0: Disable 1: Enable

Default：00XX X001B

70H: Horizontal Interpolation Filter Type (R/W)

Bits	Name	Description
D7-6		Reserved
D5	AF1	Advance Filter1
D4	AF2	Advance Filter1
D3		Reserved
D2-0	HIFM [2:0]	Horizontal Interpolation Filter Mode 000: Bi-linear 001: Little sharp 010: Middle sharp 011: High sharp 100: Ultra sharp 101: Duplicated, all the interpolated pixels are duplicated and not partial duplicated. 110: Programmable filter 111: Balance

Default：XXXX X000B

71H: Vertical Interpolation Filter Type (R/W)

Bits	Name	Description
D7-3		Reserved
D2-0	VIFM [2:0]	Vertical Interpolation Filter Mode 000: Bi-linear 001: Little sharp 010: Middle sharp 011: High sharp 100: Ultra sharp 101: Duplicated, all the interpolated pixels are duplicated and not partial duplicated. 110: Programmable filter 111: Balance

Default：XXXX X000B

72H: Programmable Interpolation Filter Access index (W)

Bits	Name	Description
D7	FILTER_PORT_W_EN	1: Enable Interpolation port write
D6	H_V_FILTER_SEL	0: V interpolation table 1: H interpolation table
D5~0		Reserved

Default：XXXX XXXXB

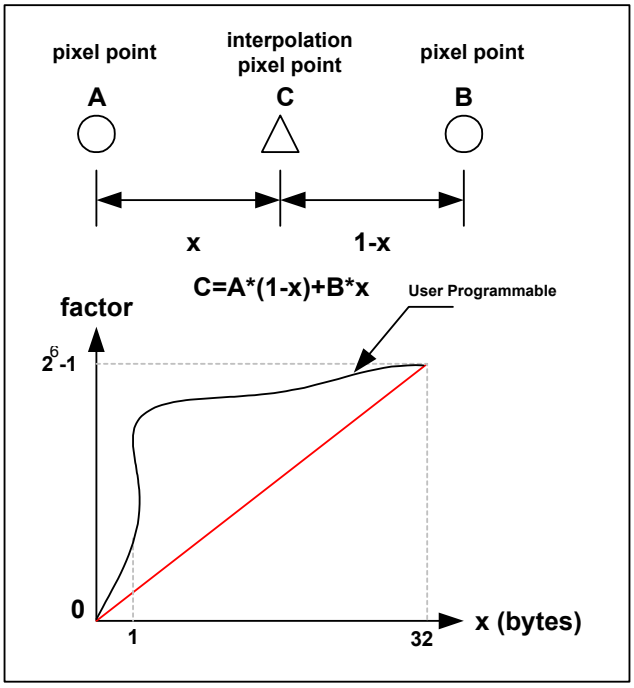
73H: Interpolation Filter Table Data Port(W)

Bits	Name	Description
D7-0	IN_F_TB	Write 32 x 6bit Programmable Interpolation filter table data in this port.

Default：XXXX XXXXB

74H ~ 76H: Reserved(W)

Interpolation filter table


pixel point
interpolation pixel point
pixel point
A
C
B
x
1-x
C=A*(1-x)+B*x
User Programmable
factor
2^6-1
0
1
32
x (bytes)

FIFO Build-In Self Test (BIST)

77H: FIFO BIST Control (R/W)

Bits	Name	Description
D7	FIFO_BIST_EN(W)	1: Enable FIFO Build-In Self Test.
D7	FIFO_BIST_EN(R)	0: FIFO Build-In Self Test Ready 1: FIFO Build-In Self Test not Ready
D6	FIFO_BIST_STATE	0 : Success 1 : Fail
D5-4	FIFO_SEL	FIFO Select
D3	FIFO_FAULT_GEN	Select FIFO test fault generation enable.
D2-0		Reserved

Default：00XX XXXXB

78H: FIFO0 BIST Fail Start (R)

Bits	Name	Description
D7-0	FIFO0_BIST_F_ST[7:0]	FIFO 0 BIST Fail Start Position[7:0]

Default：XXXX XXX0B

79H: FIFO0 BIST Fail End (R)

Bits	Name	Description
D7-0	FIFO0_BIST_F_END[7:0]	FIFO 0 BIST Fail End Position[7:0]

Default：XXXX XXX0B

7AH ~ 84H : Reserved

Sync Processor

85H: Clamp Pulse Control (R/W)

Bits	Name	Description
D7-4		Reserved
D3	CLMP_EDG	Trigger Edge of the Clamp Pulse 0 : Clamp pulse is at the trailing edge of Hsync 1 : Clamp pulse is at the leading edge of Hsync
D2	CLMP_POL	Clamp Pulse Polarity Selection 0 : Negative polarity 1 : Positive polarity
D1-0	CLMP_PW[1:0]	Clamp Pulse Width Selection 00 : 0.25us 01 : 0.5us 10 : 1us 11 : 2us

Default: XXXX 0100B

86H: Sync Processor Control (R/W)

Bits	Name	Description
D7	EN_FRUN	0: Disable free-run function to save power consumption. 1: Enable free-run function.
D6	AUTO_FLT	0: Disable Auto Filter function 1: Enable Auto Filter function of H/V extract circuit.
D5	EN_SOG	SOG function control bit 0: Disable SOGI pin 1: Enable SOGI pin, HSYNCI input will be discarded
D4		Reserved
D3	EN_POL_HID	Hsync polarity user programming 0 : Disable 1 : Enable
D2	HI_POL_SEL	Hsync input polarity select 0 : Active low 1 : Active high
D1	EN_POL_VID	Vsync polarity user programming 0 : Disable 1 : Enable
D0	VI_POL_SEL	Vsync input polarity select 0 : Active low 1 : Active high

Default: 000X 0000B

87H: H/V Sync Input Control (W)

Bits		Description
D7-6	SYNCI_SEL [1:0]	Type Selection of Sync Input 0X: Composite Sync from SOGI pin 10: Composite Sync from HSYNCI or YUV_HS pin 11: Separate Sync from HSYNCI/VSYNCI or YUV_HS/YUV_VS

D5	INS_HPW	Pulse Width Selection of inserted Hsync pulse 0: Pulse Width = value HPW[7:0] 1: Pulse Width =1uS
D4-0		Reserved

Default: 110X XXXXB

87H: H/V Sync Input Control (R)

Bits		Description
D7-5		Reserved
D4	INTERLACE	Interlace auto-detecting indicator flag. 0: Not interlace input sync 1: Interlace input sync
D3	HS_LVL	The input digital level of HSYNCI pin at the sampling moment.(for debug) 0: Low Level 1: High Level
D2	VS_LVL	The input digital level of VSYNCI pin at the sampling moment.(for debug) 0: Low Level 1: High Level
D1	HI_POL	H-Polarity Flag Detected by Input Polarity Detection Circuit. 0: Negative polarity. The high period is longer than 60% of input sync period 1: Positive polarity. The low period is longer than 60% of input sync period
D0	VI_POL	V-Polarity Flag Detected by Input Polarity Detection Circuit. 0: Negative polarity. The high period is longer than 60% of input sync period 1: Positive polarity. The low period is longer than 60% of input sync period

Default：XXXX XXXXB

88H: H/V Sync Output Control (R/W)

Bits		Description
D7	EN_HOUT	HSYNCO output enable 0: Disable 1: Enable
D6	EN_VOUT	VSYNCO output enable 0: Disable 1: Enable
D5	EN_HRUN	Free-run horizontal output control 0: Disable 1: Enable
D4	EN_VRUN	Free-run vertical output control 0: Disable 1: Enable
D3	EN_INS	Insert Hsync pulse control 0: Disable 1: Enable
D2	SYNCO_SEL	Source selection control of sync-out (HSYNCO and VSYNCO) 0: Sync output from the external sync input pin 1: Sync output from the internal free-run generator.
D1	HO_POL	Hsync output polarity control

		0: Negative polarity 1: Positive polarity
D0	VO_POL	Vsync output polarity control 0: Negative polarity 1: Positive polarity

Default: 0000 0000B

89H: Hsync Pulse Width (R)

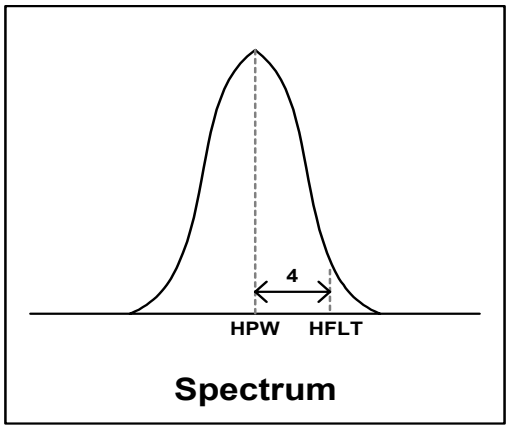
Bits	Name	Description
D7-0	HPW [7:0]	Sync processor will detect the pulse width of the external HSYNCI/SOG Input. Unit : 83.3ns/count

Default：XXXX XXXXB

8AH: Hsync Filter Reference (R/W)

Bits	Name	Description
D7-0	HFLT [7:0]	Time width of Pulse Filter for Composite/SOG sync extraction. H sync pulse with pulse width less than the reference value will be filtered out.(HPW+4) Unit : 83.3ns/count

Default: 1111 1111B



8BH: H/V Sync Counter Interval (R/W)

Bits	Name	Description
D7-4		Reserved
D3-2	VOV_SEL [1:0]	Overflow time interval control bits of Vsync Counter 00: 32.768ms 01: 65.536ms 10: 98.304ms 11: 131.072ms
D1	HGATE_SRC	Gate Source control bit for Hsync Counter 0: from Vsync Period 1: from Internal Time Gate; see HGATE_TME bit in this byte

D0	HGATE_TME	Gate Time control bit for Hsync Counter 0: 16.384ms 1: 32.768ms

Default: XXXX 0000B

8CH: Hsync Counter Value – Low Byte (R)

Bits	Name	Description
D7-0	HCNT [7:0]	Low byte value of the Hsync counter

Default: XXXX XXXXB

8DH: Hsync Counter Value – High Byte (R)

Bits	Name	Description
D7	HCNTOV	Overflow Flag of Hsync Counter 1: Overflow 0: Normal
D6-4		Reserved
D3-0	HCNT [11:8]	High byte value of the Hsync counter

Default: XXXX XXXXB

8EH: Vsync Counter Value – Low Byte (R)

Bits	Name	Description
D7-0	VCNT [7:0]	Low byte value of the Vsync counter

Default: XXXX XXXXB

8FH: Vsync Counter Value – High Byte (R)

Bits	Name	Description
D7	VCNTOV	Overflow Flag of Vsync Counter 1: Overflow 0: Normal
D6		Reserved
D5-0	VCNT [13:8]	High byte value of the Vsync counter

Default: XXXX XXXXB

90H: H/V Interrupt flag (R)

Bits	Name	Description
D7	INT_H	1: Hsync leading edge interrupt from separate or composite signal 0: No interrupt
D6	INT_V	1: Vsync leading edge interrupt from separate or composite signal 0: No interrupt

D5		Reserved
D4	INT_OVER	Line buffer overflow interrupt flag 0: No Overflow 1: Overflow
D3	INT_UNDER	Line buffer underflow interrupt flag 0: No Underflow 1: Underflow
D2	INT_HP	Input Hsync polarity change INT 1: Change 0: No change
D1	INT_VP	Input Vsync polarity change INT 1: Change 0: No change
D0	INT_FM	Fast mute INT 1: Fast mute occur 0: Not occur

Default: XXXX XXXXB

Reset scaler by CR6F bit1 will clear all CR90's flags.

91H: H/V Interrupt Clear (W)

Bits	Name	Description
D7	CLR_H	1:Clear INT_H bit 0: No effect
D6	CLR_V	1:Clear INT_V bit 0: No effect
D5		Reserved
D4	CLR_OVER	1:Clear INT_OVER bit 0: No effect
D3	CLR_UNDER	1:Clear INT_UNDER bit 0: No effect
D2	CLR_HP	1:Clear INT_HP bit 0: No effect
D1	CLR_VP	1:Clear INT_VP bit 0: No effect
D0	CLR_FM	1:Clear INT_FM bit 0: No effect

Default: 00X0 0000B

92H: H/V Interrupt Enable (R/W)

Bits	Name	Description
D7	INTH_EN	1: Enable INT_H interrupt 0: Disable
D6	INTV_EN	1: Enable INT_V interrupt 0: Disable
D5		Reserved
D4	INTOVER_EN	1: Enable INT_OVER interrupt 0: Disable

D3	INTUNDER_EN	1: Enable INT_UNDER interrupt 0: Disable
D2	INTHP_EN	1: Enable INT_HP interrupt 0: Disable
D1	INTVP_EN	1: Enable INT_VP interrupt 0: Disable
D0	INTFM_EN	1: Enable INT_FM interrupt 0: Disable

Default: 00X0 0000B

93H: Fast Mute Control (W)

Bits	Name	Description
D7	UPD_HT	This bit is controlled by S/W if AUTO_UPD=0. 0: Hold B 1: Update B from A per Hsync; see Fast Mute block diagram
D6	AUTO_UPD	0: Manually control the UPD_HT bit 1: H/W automatically sets UPD_HT to update B from A when the fast mute occurs, then it clears UPD_HT after the input Hsync has been stable for at least 3mS.
D5	VINT_POL	Invert the internal V-sync polarity. (for debug) 0: Normal 1: Invert
D4	HINT_POL	Invert the internal H-sync polarity. (for debug) 0: Normal 1: Invert
D3-2	DIFF_CNT [1:0]	The FAST MUTE will occur if the number of times out of DIFF_VAL are larger than the DIFF_CNT setting. 00: 4 times 01: 8 times 10: 16 times 11: 32 times
D1-0	DIFF_VAL [1:0]	Difference Boundary of the H-Period Counter 00: 4 counts 01: 8 counts 10: 16 counts 11: Reserved

Default: 11XX 0101B

93H: Fast Mute Control (R)

Bits	Name	Description
D7-6		Reserved
D5	HS_ACT	0: No Hsync in 3mS interval. (for debug) 1: Hsync is active.
D4	VS_ACT	0: No Vsync in 132mS interval. (for debug) 1: Vsync is active.
D3-0		Reserved

94H: Interlaced Field Decision Window (R/W)

Bits	Name	Description
D7-4	WIN_END	The 4-bit defines the Window End position.
D3-0	WIN_STR	Divide the H-sync period into 16 parts; the 4-bit defines the Window Start position. IF the input V-sync leading edge locates inside the window, it represents the occurrence of the ODD field.

OSD Function

95H: OSD and Window Enable Control (R/W)

Bits	Name	Description
D7-5		Reserved
D4	WIN4_EN	Enable Window 4 0: Disable 1: Enable
D3	WIN3_EN	Enable Window 3 0: Disable 1: Enable
D2	WIN2_EN	Enable Window 2 0: Disable 1: Enable
D1	WIN1_EN	Enable Window 1 0: Disable 1: Enable
D0	OSD_EN	Enable OSD 0: Disable 1: Enable

Default: XXX0 0000B

96H: OSD Frame Horizontal Start - Low byte (R/W)

Bits	Name	Description
D7-0	OSD_HS [7:0]	OSD frame horizontal start low byte [7:0]. Specifies the horizontal starting position of the OSD in pixel units. This register is double-buffered.

Default: 0000 0000B

97H: OSD Frame Horizontal Start - High Byte (R/W)

Bits	Name	Description
D7-3		Reserved
D2-0	OSD_HS [10:8]	OSD frame horizontal start high byte [10:8]. Specifies the horizontal starting position of the OSD in pixel units. This register is double-buffered.

Default: XXXX X000B

98H: OSD Frame Horizontal Width (R/W)

Bits	Name	Description
D7-5		Reserved
D4-0	OSD_HW [4:0]	Specifies the width of the OSD in font units. Writing this register will transfer the double-buffered registers 96h – 97h to the actual OSD frame control registers. Range: 0~20

Default: XXX0 0000B

99H: OSD Frame Vertical Start Low byte (R/W)

Bits	Name	Description
D7-0	OSD_VS [7:0]	OSD frame vertical start low byte [7:0]. Specifies the vertical starting position of the OSD in line units. This register is double-buffered.

Default: 0000 0000B

9AH: OSD Frame Vertical Start High byte (R/W)

Bits	Name	Description
D7-3		Reserved
D2-0	OSD_VS [10:8]	OSD frame vertical start high byte [10:8]. Specifies the vertical starting position of the OSD in line units. This register is double-buffered.

Default: XXXX X000B

9BH: OSD Frame Vertical Height (R/W)

Bits	Name	Description
D7-5		Reserved
D4-0	OSD_VH [4:0]	Specifies the height of the OSD in font units. Writing to this register will transfer the double-buffered registers 99h – 9Ah to the actual OSD frame control registers Range: 0~16

Default: XXX0 0000B

9CH: OSD SRAM Address Offset (R/W)

Bits	Name	Description
D7-5		Reserved
D4-0	OSD_SRAM_OFF [4:0]	OSD SRAM address offset. Number of fonts between OSD rows. Range: 0~31

Default: XXX0 0000B

9DH: Reserved (R/W)

Bits	Name	Description
D7-0		Reserved

Default: XXXX XXXXB

OSD Zoom Control

9EH: OSD Zoom Control (R/W)

Bits	Name	Description
D7-4		Reserved
D3	VROW_ZMEN	Vertical Row Zoom Enable; Vertical zoom for all characters in one row defined in RegA6H/RegA7H. 0: Disable 1: Enable.
D2	HROW_ZMEN	Horizontal Row Zoom Enable; Horizontal zoom for all characters in one

		row defined in regA4H/RegA5H. 0: Disable 1: Enable.
D1	VGLOB_ZMEN	Vertical Global Zoom Enable; Vertical zoom for all characters in OSD frame. 0: Disable 1: Enable.
D0	HGLOB_ZMEN	Horizontal Global Zoom Enable; Horizontal zoom for all characters in OSD frame. 0: Disable 1: Enable.

Default: XXXX 0000B

9FH: OSD Font Horizontal Zoom Pattern - Low Byte (R/W)

Bits	Name	Description
D7-0	HZM_PATN [7:0]	Least significant 8 bits(7:0) of the horizontal zoom pattern. This is a user definable zoom pattern. Pixels with '1' pattern are duplicated according to the zoom range.

Default: 0000 0000B

A0H: OSD Font Horizontal/Vertical Zoom Pattern - High Byte (R/W)

Bits	Name	Description
D7-6		Reserved
D5-4	VZM_PATN [17:16]	Most significant 2 bits(17:16) of the vertical zoom pattern. This is a user definable zoom pattern. Pixels with '1' pattern are duplicated according to the zoom range.
D3-0	HZM_PATN [11:8]	Most significant 4 bits(11:8) of the horizontal zoom pattern. This is a user definable zoom pattern. Pixels with '1' pattern are duplicated according to the zoom range.

Default: XX00 0000B

A1H: OSD Font Vertical Zoom Pattern - Low Byte (R/W)

Bits	Name	Description
D7-0	VZM_PATN [7:0]	Least significant 8 bits(7:0) of the vertical zoom pattern. This is a user definable zoom pattern. Pixels with '1' pattern are duplicated according to the zoom range.

Default: 0000 0000B

A2H: OSD Font Vertical Zoom Pattern - Mid Byte (R/W)

Bits	Name	Description
D7-0	VZM_PATN [15:8]	Bits (15:8) of the vertical zoom pattern. This is a user definable zoom pattern. Pixels with '1' pattern are duplicated according to the zoom range.

Default: 0000 0000B

A3H: OSD Font Global Zoom Range (R/W)

Bits	Name	Description
D7-4		Reserved
D3-2	VGLOB_ZMRNG [1:0]	Vertical Global Zoom Range 00: No Zoom 01: Vertical Zoom Pattern (RegA0H-RegA2H) '1' bits are duplicated once, '0' bits are not duplicated (Zooms from 1x to 2x). 10: Vertical Zoom Pattern '1' bits are duplicated twice, '0' bits are duplicated once (Zooms from 2x to 3x). 11: Vertical Zoom Pattern '1' bits are duplicated three times, '0' bits are duplicated twice (Zooms from 3x to 4x).
D1-0	HGLOB_ZMRNG [1:0]	Horizontal Global Zoom Range 00: No Zoom 01: Horizontal Zoom Pattern (Reg9FH-RegA0H) '1' bits are duplicated once, '0' bits are not duplicated (Zooms from 1x to 2x). 10: Horizontal Zoom Pattern '1' bits are duplicated twice, '0' bits are duplicated once (Zooms from 2x to 3x). 11: Horizontal Zoom Pattern '1' bits are duplicated three times, '0' bits are duplicated twice (Zooms from 3x to 4x).

Default: XXXX 0000B

A4H: Horizontal Row Zoom Control Row 7 - 0 (R/W)

Bits	Name	Description
D7-0	HROW_ZMPN [7:0]	Horizontal Row Zoom Pattern 7-0 Zooms each row horizontally defined as zoom range according to each bit. Each bit controls a row correspondingly. Reg9E[2] must be set to '1'.

Default: 0000 0000B

A5H: Horizontal Row Zoom Control Row 15 - 8 (R/W)

Bits	Name	Description
D7-0	HROW_ZMPN [15:8]	Horizontal Row Zoom Pattern 15-8, Zooms each row horizontally defined as zoom range according to each bit. Each bit controls a row correspondingly. Reg9E[2] must be set to '1'.

Default: 0000 0000B

A6H: Vertical Row Zoom Control Row 7 - 0 (R/W)

Bits	Name	Description
D7-0	VROW_ZMPN [7:0]	Vertical Row Zoom Pattern 7-0, Zooms each row vertically defined as zoom range according to each bit. Each bit controls a row correspondingly. Reg9E[3] must be set to '1'.

Default: 0000 0000B

A7H: Vertical Row Zoom Control Row 15 - 8 (R/W)

Bits	Name	Description
D7-0	VROW_ZMPN	Vertical Row Zoom Pattern 15-8, Zooms each row vertically defined as

	[15:8]	zoom range according to each bit. Each bit controls a row correspondingly. Reg9E[3] must be set to '1'.

Default: 0000 0000B

A8H: OSD Font Row Zoom Range (R/W)

Bits	Name	Description
D7-4		Reserved
D3-2	VROW_ZMRNG[1:0]	Vertical Row Zoom Range; The rows assigned by Vertical Row Zoom Control registers will be zoomed up. 00: Vertical Zoom 1x for all fonts in the row 01: Vertical Zoom 2x for all fonts in the row 10: Vertical Zoom 3x for all fonts in the row 11: Vertical Zoom 4x for all fonts in the row
D1-0	HROW_ZMRNG[1:0]	Horizontal Row Zoom Range; The rows assigned by Horizontal Row Zoom Control registers will be zoomed up. 00: Horizontal Zoom 1x for all fonts in the row 01: Horizontal Zoom 2x for all fonts in the row 10: Horizontal Zoom 3x for all fonts in the row 11: Horizontal Zoom 4x for all fonts in the row

Default: XXXX 0000B

A9H: Reserved (R/W)

Bits	Name	Description
D7-0		Reserved

Default: XXXX XXXXB

OSD Attribute Control

AAH: OSD Attribute (R/W)

Bits	Name	Description
D7-0	OSD_ATTR [7:0]	This value is appended with the character font code when updating the OSD SRAM code from host and "attribute from Reg AAh" is selected in register E0[5:4].

Default: 0000 0000B

ABH: OSD Blink Control (R/W)

Bits	Name	Description
D7		Reserved
D6	OSD_BLINK	Blink 1=OSD frame blink enable, and the attribute bit 0 is ignored. 0=Blink control from font attribute bit 0.
D5	BS_BLINK	Mask Border/Shadow at Blink 1=Character border/shadow will not blink with the foreground of the character. 0= Character border/shadow will blink with the foreground of the character.

D4-2	BLINK_RATE [2:0]	Blink Rate 000: Character foreground is turned on/off every 16 frames. 001: Character foreground is turned on/off every 8 frames. 010: Character foreground is turned on/off every 4 frames. 011: Character foreground is turned on/off every 2 frames. 100: Character foreground is turned on/off every other frames.
D1	OSD_BG [3]	OSD Background bit BG[3], The most significant bit of the OSD background color attribute. This bit is appended with the attribute bits [4:2] to make up the 4-bit background color.
D0	OSD_FG [3]	OSD Foreground bit FG[3], The most significant bit of the OSD foreground color attribute. This bit is appended with the attribute bits [7:5] to make up the 4-bit background color.

Default: X000 0000B

OSD Window Control

ACH: OSD Window 1 Horizontal Start (R/W)

Bits	Name	Description
D7-5		Reserved
D4-0	WIN1_HS [4:0]	Horizontal starting position relative to the OSD. The unit is in font. Range: 0~19

Default: XXX0 0000B

ADH: OSD Window 1 Horizontal End (R/W)

Bits	Name	Description
D7-5		Reserved
D4-0	WIN1_HE [4:0]	Horizontal ending position relative to the OSD. Range: 0~19 fonts

Default: XXX0 0000B

AEH: OSD Window 1 vertical Start/End (R/W)

Bits	Name	Description
D7-4	WIN1_VE [3:0]	Vertical ending position relative to the OSD. The unit is in font. Range: 0~15
D3-0	WIN1_VS [3:0]	Vertical starting position relative to the OSD. The unit is in font. Range: 0~15

Default: 0000 0000B

AFH: OSD Window 1 Attribute (R/W)

Bits	Name	Description
D7-4	WIN1_ATTR [3:0]	Attribute Color for the OSD Window 1. This color will cover the character background color when Window 1 is enabled.
D3-2	WIN1_SDSZ [1:0]	Shadow Size 00: 2 pixels in width and 2 lines in height. 01: 4 pixels in width and 4 lines in height. 10: 6 pixels in width and 6 lines in height.

		11: 8 pixels in width and 8 lines in height.
D1	WIN1_SDEN	Window Shadow Enable Shadow size is specified in bits 3:2. 1= Shows a shadow for Window 1. 0= No shadow
D0		Reserved

Default: 0000 000XB

B0H: OSD Window 2 Horizontal Start (R/W)

Bits	Name	Description
D7-5		Reserved
D4-0	WIN2_HS [4:0]	Horizontal starting position relative to the OSD. The unit is in font. Range: 0~19

Default: XXX0 0000B

B1H: OSD Window 2 Horizontal End (R/W)

Bits	Name	Description
D7-5		Reserved
D4-0	WIN2_HE [4:0]	Horizontal ending position relative to the OSD. The unit is in font. Range: 0~19

Default: XXX0 0000B

B2H: OSD Window 2 vertical Start/End (R/W)

Bits	Name	Description
D7-4	WIN2_VE	Vertical ending position relative to the OSD. The unit is in font. Range: 0~15
D3-0	WIN2_VS	Vertical starting position relative to the OSD. The unit is in font. Range: 0~15

Default: 0000 0000B

B3H: OSD Window 2 Attribute (R/W)

Bits	Name	Description
D7-4	WIN2_ATTR [3:0]	Attribute Color for the OSD Window 2. This color will cover the character background color when Window 2 is enabled.
D3-2	WIN2_SDSZ [1:0]	Shadow Size 00: 2 pixels in width and 2 lines in height. 01: 4 pixels in width and 4 lines in height. 10: 6 pixels in width and 6 lines in height. 11: 8 pixels in width and 8 lines in height.
D1	WIN2_SDEN	Window Shadow Enable, Shadow size is specified in bits 3:2. 0: Window2 no shadow 1: Shows a shadow for Window 2.
D0		Reserved

Default: 0000 000XB

B4H: OSD Window 3 Horizontal Start (R/W)

Bits	Name	Description
D7-5		Reserved
D4-0	WIN3_HS [4:0]	Horizontal starting position relative to the OSD. The unit is in font. Range: 0~19

Default: XXX0 0000B

B5H: OSD Window 3 Horizontal End (R/W)

Bits	Name	Description
D7-5		Reserved
D4-0	WIN3_HE [4:0]	Horizontal ending position relative to the OSD. The unit is in font. Range: 0~19

Default: XXX0 0000B

B6H: OSD Window 3 vertical Start/End (R/W)

Bits	Name	Description
D7-4	WIN3_VE	Vertical ending position relative to the OSD. The unit is in font. Range: 0~15
D3-0	WIN3_VS	Vertical starting position relative to the OSD. The unit is in font. Range: 0~15

Default: 0000 0000B

B7H: OSD Window 3 Attribute (R/W)

Bits	Name	Description
D7-4	WIN3_ATTR [3:0]	Attribute Color for the OSD Window 3. This color will cover the character background color when Window 3 is enabled.
D3-2	WIN3_SDSZ [1:0]	Shadow Size 00: 2 pixels in width and 2 lines in height. 01: 4 pixels in width and 4 lines in height. 10: 6 pixels in width and 6 lines in height. 11: 8 pixels in width and 8 lines in height.
D1	WIN3_SDEN	Window Shadow Enable, Shadow size is specified in bits 3:2. 0: Window3 no shadow 1: Shows a shadow for Window 3.
D0		Reserved

Default: 0000 000XB

B8H: OSD Window 4 Horizontal Start (R/W)

Bits	Name	Description
D7-5		Reserved
D4-0	WIN4_HS [4:0]	Horizontal starting position relative to the OSD. The unit is in font. Range: 0~19

Default: XXX0 0000B

B9H: OSD Window 4 Horizontal End (R/W)

Bits	Name	Description
D7-5		Reserved
D4-0	WIN4_HE [4:0]	Horizontal ending position relative to the OSD. The unit is in font. Range: 0~19

Default: XXX0 0000B

BAH: OSD Window 4 vertical Start/End (R/W)

Bits	Name	Description
D7-4	WIN4_VE	Vertical ending position relative to the OSD. The unit is in font. Range: 0~15
D3-0	WIN4_VS	Vertical starting position relative to the OSD. The unit is in font. Range: 0~15

Default: 0000 0000B

BBH: OSD Window 4 Attribute (R/W)

Bits	Name	Description
D7-4	WIN4_ATTR [3:0]	Attribute Color for the OSD Window 4. This color will cover the character background color when Window 4 is enabled.
D3-2	WIN4_SDSZ [1:0]	Shadow Size 00: 2 pixels in width and 2 lines in height. 01: 4 pixels in width and 4 lines in height. 10: 6 pixels in width and 6 lines in height. 11: 8 pixels in width and 8 lines in height.
D1	WIN4_SDEN	Window Shadow Enable, Shadow size is specified in bits 3:2. 0: Window 4 no shadow 1: Shows a shadow for Window 4.
D0		Reserved

Default: 0000 000XB

BCH: OSD Window Shadow Color (R/W)

Bits	Name	Description
D7-4		Reserved
D3-0	WIN_SDCL [3:0]	Color index for all four window's shadow

Default: XXXX 0000B

BDH: Reserved (R/W)

Bits	Name	Description
D7-0		Reserved

Default: XXXX XXXXB

OSD Border And Shadow Control

BEH: OSD Shadow Control Row 7 - 0 (R/W)

Bits	Name	Description
D7-0	OSD_SCR [7:0]	Character Row Shadow Enable for 7-0. Each bit controls each row correspondingly. 1= Enable shadow for a row.

Default: 0000 0000B

BFH: OSD Shadow Control Row 15 - 8 (R/W)

Bits	Name	Description
D7-0	OSD_SCR [15:8]	Character Row Shadow Enable for 15-8. Each bit controls each row correspondingly. 1= Enable shadow for a row.

Default: 0000 0000B

C0H: OSD Border Control Row 7 - 0 (R/W)

Bits	Name	Description
D7-0	OSD_BCR [7:0]	Character Row Border Enable for 7-0. Each bit controls each row correspondingly. 1= Enable border for a row.

Default: 0000 0000B

C1H: OSD Border Control Row 15-8 (R/W)

Bits	Name	Description
D7-0	OSD_BCR [15:8]	Character Row Border Enable for 15-8. Each bit controls each row correspondingly 1= Enable border for a row.

Default: 0000 0000B

C2H: OSD Border & Shadow Color Row 1 - 0 (R/W)

Bits		Description
D7-4	OSD_BSCR1 [3:0]	Character Border/Shadow Color Index For Row 1
D3-0	OSD_BSCR0 [3:0]	Character Border/Shadow Color Index For Row 0

Default: 0000 0000B

C3H: OSD Border & Shadow Color Row 3 - 2 (R/W)

Bits	Name	Description
D7-4	OSD_BSCR3 [3:0]	Character Border/Shadow Color Index For Row 3
D3-0	OSD_BSCR2 [3:0]	Character Border/Shadow Color Index For Row 2

Default: 0000 0000B

C4H: OSD Border & Shadow Color Row 5 - 4 (R/W)

Bits	Name	Description
D7-4	OSD_BSCR5 [3:0]	Character Border/Shadow Color Index For Row 5
D3-0	OSD_BSCR4 [3:0]	Character Border/Shadow Color Index For Row 4

Default: 0000 0000B

C5H: OSD Border & Shadow Color Row 7- 6 (R/W)

Bits	Name	Description
D7-4	OSD_BSCR7 [3:0]	Character Border/Shadow Color Index For Row 7
D3-0	OSD_BSCR6 [3:0]	Character Border/Shadow Color Index For Row 6

Default: 0000 0000B

C6H: OSD Border & Shadow Color Row 9 - 8 (R/W)

Bits	Name	Description
D7-4	OSD_BSCR9 [3:0]	Character Border/Shadow Color Index For Row 9
D3-0	OSD_BSCR8 [3:0]	Character Border/Shadow Color Index For Row 8

Default: 0000 0000B

C7H: OSD Border & Shadow Color Row 11 - 10 (R/W)

Bits	Name	Description
D7-4	OSD_BSCR11 [3:0]	Character Border/Shadow Color Index For Row 11
D3-0	OSD_BSCR10 [3:0]	Character Border/Shadow Color Index For Row 10

Default: 0000 0000B

C8H: OSD Border & Shadow Color Row 13 - 12 (R/W)

Bits	Name	Description
D7-4	OSD_BSCR13 [3:0]	Character Border/Shadow Color Index For Row 13
D3-0	OSD_BSCR12 [3:0]	Character Border/Shadow Color Index For Row 12

Default: 0000 0000B

C9H: OSD Border & Shadow Color Row 15 - 14 (R/W)

Bits	Name	Description

D7-4	OSD_BSCR15 [3:0]	Character Border/Shadow Color Index For Row 15
D3-0	OSD_BSCR14 [3:0]	Character Border/Shadow Color Index For Row 14

Default: 0000 0000B

CAH: Reserved (R/W)

Bits	Name	Description
D7-0		Reserved

Default: XXXX XXXXB

OSD Fast Clear Control

CBH: OSD SRAM Attribute Value For Fast Clear (R/W)

Bits	Name	Description
D7-0	ATTR_FC [7:0]	SRAM attribute for fast clear.

Default: 0000 0000B

CCH: OSD SRAM Code Value For Fast Clear (R/W)

Bits	Name	Description
D7-0	CODE_FC [7:0]	SRAM code for fast clear. Writing in this register will fill the entire SRAM with the values in RegCBh ~ RegCCh (Attribute Code:).

Default: 0000 0000B

CDH: Fast Clear Status (R)

Bits	Name	Description
D7-1		Reserved
D0	FC_RDY	Fast Clear Ready. H/W will clear all bits after reading this register. 1: Ready 0: Not Ready

Default: XXXX XXX0B

CEH: Reserved (R/W)

Bits	Name	Description
D7-0		Reserved

Default: XXXX XXXXB

DPLL Clock Control

Formula :

F*out* = ((N+2) x F*ref)* / (M+2)

F*ref* = 12 MHz

CFH: DPLL Control(R/W)

Bits	Name	Description
D7-2		Reserved
D1	DPLL_EN	Enable DPLL 0: Disable 1: Enable
D0		Reserved

Default: XXXX XX10B

D0H: Reserved

D1H: Reserved

D2H: DPLL VCO Divider –N (R/W)

Bits	Name	Description
D7-6	RCZ1 [1:0]	
D5-0	DPLL_N [5:0]	DPLL VCO Divider Value (N). This register is double-buffered.

Default: 0000 0000B

D3H: DPLL VCO Divider –M (R/W)

Bits	Name	Description
D7-6	FOA [1:0]	
D5-4	VCA [1:0]	
D3-0	DPLL_M [3:0]	DPLL VCO Divider Value (M), Writing in this register will load the double-buffered register D2h to take affect

Default: 0000 0000B

D4H: DPLL Select and Power Up Control (R/W)

Bits	Name	Description
D7	PU_APLL	Power up PLL internal circuit 0: Power down 1: Power up
D6	PU_V	Power up PLL internal circuit 0: Power down 1: Power up
D5	EN_FOA	

D4	EN_FOB	
D3		Reserved
D2-1	VREG [1:0]	For PLL internal regulator adjust
D0	SEL_DPLL	Select PLL 0: Reserve 1: DPLL

Default: 1100 X001B

D5H: Reserved

D6H: DPLL VCO Adjust (R/W)

Bits	Name	Description
D7-6	DFRANGE [1:0]	DPLL frequency range 00: 22~40 MHz KVCO= 17MHz/V 01: 37~64 MHz KVCO= 26MHz/V 10: 59~106 MHz KVCO= 48MHz/V 11: 97~167 MHz KVCO= 60MHz/V
D5-4	DCPI [1:0]	DPLL charge pump current 00: 100 uA 01: 200 uA 10: 400 uA 11: 800 uA
D3	DLOWICP	Lower the charge pump current by factor. 0: 1 1: 1.5
D2-0	DKVCO [2:0]	KVCO adjust for process variation 100: Normal below 100: Lower KVCO above 100: Higher KVCO

Default: 1000 0100B

D7H: DPLL PFD Test (R/W)

Bits	Name	Description
D7	EN_MONT	
D6-5	MONT[1:0]	
D4	TPFD2	
D3-2	PFDMONT [1:0]	
D1	TPFD	
D0	TCNT	

Default: 0000 0000B

D8H~D9H: Reserved for testing(R/W)

Bits	Name	Description
D7-0		For scaler test

Default: XXXX XXXXB

Miscellaneous

DA: Syncprocessor Free Run Horizontal Divider - Low Byte (R/W)

Bits	Name	Description
D7-0	DCNT [7:0]	Written Content of Dot Divider for Horizontal free running: ①Bit Number = 9 Bits ②Dot Clock = 12MHz ③Valid Range = 48 ~ 511 If out of this valid range, the reset default values will be loaded into DCNT & LCNT to protect the following circuit. ④Horizontal Frequency of the free running is Hfreq(free) = 12MHz / DCNT (ex) If 100KHz free-run horizontal frequency is required , then the following divider content will be set. DCNT = 12MHz / 100KHz =120(dec) = 78(hex)

Default: 0111 1100B

DB: Syncprocessor Free Run Horizontal Divider - High Byte (R/W)

Bits	Name	Description
D7-1		Reserved
D0	DCNT[8]	MSB of Free Run Horizontal Divider (double buffer)

Default: XXXX XXX1B

DC: Syncprocessor Free Run Vertical Divider - Low Byte (R/W)

Bits	Name	Description
D7-0	LCNT [7:0]	Written Content of Line Divider for Vertical free running: ①Bit Number = 11 Bits ②Line Clock = Hfreq(free) ③Valid Range = 100 ~ 2047 If out of this valid range, the reset default values will be loaded into DCNT & LCNT to protect the following circuit. ④Vertical Frequency of the free running is Vfreq(free) = Hfreq(free)/LCNT = (12MHz / DCNT) / LCNT (ex) if 100Hz free-run vertical frequency is required wanted at Hfreq(free)=100KHz condition, then the following Line divider content will be set LCNT = 100KHz / 100Hz =1000(dec) = 3E8(hex)

Default: 0000 1101B

DD: Syncprocessor Free Run Vertical Divider - High Byte (R/W)

Bits	Name	Description
D7-3		Reserved
D2-0	LCNT[10:8]	MSB of Free Run Vertical Divider (double buffer)

Default: XXXX X010B

DE: Capture Horizontal Total Read Back - Low Byte (R)

Bits	Name	Description
D7-0	CAP_HTRB [7:0]	Read back the low byte value of input Hsync Total (Unit: DCLK) (for debug)

Default: XXXX XXXXB

DF: Capture Horizontal Total Read Back - High Byte (R)

Bits	Name	Description
D7-6		Reserved
D5-0	LCNT[13:8]	Read back the high byte value of input Hsync Total (Unit: DCLK) (for debug)

Default: XXXX XXXXB

Index Port Access Control

E0H: Index Access Port (R/W)

Bits	Name	Description
D7-6	GAMA_SEL	Gamma SRAM Select 00: Red Gamma Table 01: Green Gamma Table 10: Blue Gamma Table 11: R/G/B Gamma Tables modified simultaneously
D5-4	SRAM_AC	SRAM Access Control Controls different ways of updating the OSD SRAM. 00: Update SRAM code and attribute. 01: Update SRAM attribute only. 10: Update SRAM code only. 11: Update SRAM code from host and attribute from REG AAh.
D3-2	PORT_AC	Port Access Control Specifies which set of memory to access. 00: Read/Write OSD SRAM. 01: Read/Write OSD Palette. 10: Read/Write OSD Programmable Font. 11: Read/Write Gamma SRAM.
D1	PORT_RW	Port Read/Write 0: Write 1: Read
D0	INDEX [8]	Bit 8 of SRAM address for OSD. Bit 7-0 is in E1h

Default: 0000 0000B

E1H: Index Address Port (R/W)

Bits	Name	Description
D7-0	INDEX [7:0]	♦ OSD SRAM: Indexed by font SRAM: Least significant 7 bits of the SRAM index.

		SRAM size is 320 fonts. Index range 0 – 0x13F (319). Bit 8 in E0h[0] ♦ Palette: Indexed by word Index range 0 – 0x0F. ♦ Gamma: Indexed by byte 256 bytes for each R/G/B component Index range 0 - 0xFF. ♦ Programmable Font: Indexed by font 64 characters available for programming. Index range 0 - 0x3F.

Default: 0000 0000B

E2H: Index Data Port (R/W)

Bits	Name	Description
D7-0	PORT_DATA [7:0]	Data port for the SRAM, Palette, Programmable Font and ROM.

Default: 0000 0000B

E3H: Device ID (R)

Bits	Name	Description
D7-0	ID	01H

Default: XXXX XX01B

E4H~E6HReserve

E7H: Test Mode Control (R/W)

Bits	Name	Description
D7	Dclk_ext	Feed DCLK signal from external pin 1: Enable 0: Disable
D6		Reserve
D5	Refclk_out	REFCLK output enable 1: Enable 0: Disable
D4	Rgb_ext	Feed RGB signal from external pins 1: Enable 0: Disable
D3	Pll_out	PLL output enable 1: Enable 0: Disable
D2	Adc_out	ADC output Enable 1: Enable 0: Disable
D1	Pbus	I2C parallel bus enable

		1: Enable 0: Disable
D0	Tm_en	Test Mode Enable Control 1: Enable 0: Disable

Default：0X00 0000B

E8H: Power Control (R/W)

Bits	Name	Description
D7	MPU1	Master power control 1: Power up except PLL circuit 0: Power down except PLL circuit
D6	PU_pll1	Power up frequency PLL 1: Power up 0: Power down
D5		Reserved
D4	PU_tsen1	Power up on chip temperature sensor 1: Power up 0: Power down
D3		Reserved
D2	AC_couple	DC/AC Coupling Select 1: AC Couple 0: DC Couple
D1-0		Reserved

Default：11X1 01XXB

E9H: Temperature control (R)

Bits	Name	Description
D7-5	Temp[2:0]	Temperature readout
D4-0		Reserved

Default：XXXX XXXXB

EAH: VGA differential output control (R/W)

Bits	Name	Description
D7		Reserved
D6-4	Test_Ctrl[2:0]	Test control 000 : none 001 : R channel VGA output,TestP=VGAoutP,TestN=VGAoutM 010 : G channel VGA output,TestP=VGAoutP,TestN=VGAoutM 011 : B channel VGA output,TestP=VGAoutP,TestN=VGAoutM 100 : TestP=Tpout1 101 : TestP=Tpout2 110 : TestP=Tpout3

D3		Reserved
D2	EN_acmux4	
D1	EN_acmux1	
D0	EN_acmux_vga	

Default：X000 X000B

EBH: DAC Clock Comparator Control (R/W)

Bits	Name	Description
D7		Reserved
D6		Reserved
D5		Reserved
D4		Reserved
D3	EN_intclp	=1, Enable internal AC_couple clock for VGA and auto-zero clock ADC.
D2	Rgc_sw	Comparator gain control for R channel
D1-0	Rrf_mg[1:0]	Reference voltage controller R channel resistor ladder 00 : 0.75v~1.25v 01 : 0.70v~1.30v 10 : 0.65v~1.35v 11 : 0.60v~1.40v

Default：000X 0000B

ECH: ADC R channel gain control (R/W)

Bits	Name	Description
D7-4	Rbgc2[3:0]	R channel comparator gain control bias 2
D3-0	Rbgc1[3]0]	R channel comparator gain control bias 1

Default：0000 0000B

EDH: DC readout control for VGA and comparator control for G channel (R/W)

Bits	Name	Description
D7		Reserved
D6-5	SEL_TP_vga[1:0]	Select DC output in VGA from R,G,B channels 00 : no output 01 : R channel 10 : G channel 11 : B channel
D4-3	MONT_vga[1:0]	Select DC output in VGA 00 : OUTP 01 : OUTM 10 : mvga4op 11 : mvga4om
D2	Ggc_sw	Comparator gain control for G channel

D1-0	Grf_mg[1:0]	Reference voltage control G channel resistor ladder 00 : 0.75v~1.25v 01 : 0.70v~1.30v 10 : 0.65v~1.35v 11 : 0.60v~1.40v

Default：X000 0000B

EEH: ADC G channel gain control (R/W)

Bits	Name	Description
D7-4	Gbgc2[3:0]	G channel comparator gain control bias 2
D3-0	Gbgc1[3:0]	G channel comparator gain control bias 1

Default：0000 0000B

EFH: (R/W)

Bits	Name	Description
D7	EN_ckcopad	
D6-5	SEL_TP_adc[1:0]	Select DC output in ADC from R,G,B channel 00 : no output 01 : R channel 10 : G channel 11 : B channel
D4-3	Mont_adc[1:0]	Select DC output in ADC 00 : none 01 : azcm<1> 10 : azcm<0> 11 : none
D2	Bgc_sw	Comparator gain control for B channel
D1-0	Brf_mg[1:0]	Reference voltage control for B channel resistor ladder 00 : 0.75v~1.25v 01 : 0.70v~1.30v 10 : 0.65v~1.35v 11 : 0.60v~1.40v

Default：0000 0000B

F0H: ADC B channel gain control (R/W)

Bits	Name	Description
D7-4	Bbgc2[3:0]	B channel comparator gain control bias 2
D3-0	Bbgc1[3:0]	B channel comparator gain control bias 1

Default：0000 0000B

F1H: Tri-state output and power up ADC bias control (R/W)

Bits	Name	Description
D7	EN_Rdatapad	Enable ADC R channel.
D6	EN_Gdatapad	Enable ADC G channel.
D5	PU_compa_R1	Power up A part bias for R channel.
D4	PU_compb_R1	Power up B part bias for R channel.
D3	PU_compa_G1	Power up A part bias for G channel.
D2	PU_compb_G1	Power up B part bias for G channel.
D1	PU_compa_B1	Power up A part bias for B channel.
D0	PU_compb_B1	Power up B part bias for B channel.

Default：0011 1111B

F2H: PLL and IV source DC readout (R/W)

Bits	Name	Description
D7	EN_Bdatapad	
D6	EN_Ivmont	
D5-4	IV_mont[1:0]	Select DC output in ibblk.
D3	EN_CPO	
D2-1	PLLmont[1:0]	
D0		Reserved

Default：0000 000XB

F3H: ADC data select control (R/W)

Bits	Name	Description
D7	TST_data_R	Data output either A part or B part in R channel enable 0 : Disable 1 : Enable
D6	SEL_data_R	R channel data output 0 : Select A part data output 1 : Select B part data output
D5	TST_data_G	Data output either A part or B part in G channel enable 0 : Disable 1 : Enable
D4	SEL_data_G	G channel data output 0 : Select A part data output

		1 : Select B part data output
D3	TST_data_B	Data output either A part or B part in B channel enable 0 : Disable 1 : Enable
D2	SEL_data_B	B channel data output 0 : Select A part data output 1 : Select B part data output
D1		Reserved
D0		Reserved

Default：0000 00XXB

F4H: CKCO output select (R/W)

Bits	Name	Description
D7	Bypass	
D6	CAPTURE_CLK	0:Capture clock from Internal PLL 1:Capture clock from YUV_CLK
D5		Reserved
D4	EN_CKCO	CKCO clock enable 0 : Disable 1 : Enable
D3-2		Reserved
D1	EN_CKBO	CKBO clock enable 0 : Disable 1 : Enable
D0	EN_CKAO	CKAO clock enable 0 : Disable 1 : Enable

Default：0XX0 XX10B

F5H: Test Mode Control 2 (R/W)

Bits	Name	Description
D7-6	TESR_MODE_SEL	
D5	TEST_MODE	Logic test mode enable
D4	CKAO_EN	ADC CKAO output enable
D3	FLASH NOISE	1:Flash noise detect function enable
D2	SERIAL_OUT	FIFO test serial output enable
D1	DCLK_SEL	0 : Internal source. 1 : External source.
D0	I2C_START	I2C start for Pbus. 0 : None 1 : Send start condition.

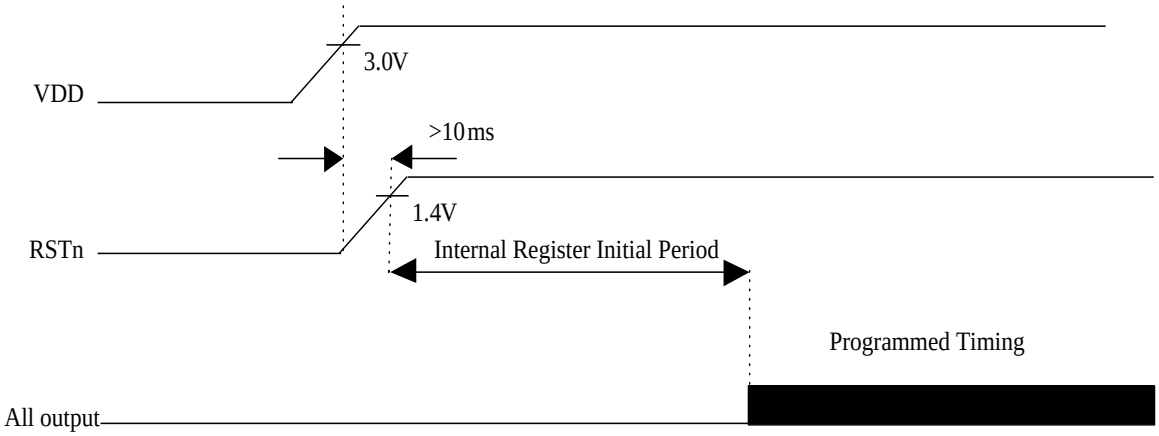
Default：0000 0X00B

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min.	Typ.	Max.	Unit
DVDD,ADC_VAA,PLL_VCC	Supply voltage analog 3.3V , digital 3.3V	-0.3		3.6	V
Vin	Input Voltage (5V Tolerant)	-0.3		5.5	V
V_{ESD}	Electrostatic Discharge			±2.5	KV
T_A	Ambient Operating Temperature	0		70	℃
T_{ST}	Storage Temperature	-40		125	℃

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VCC		DVDD,CVDD,VDD,RVAA, GVAA,BVAA,ADC_RVAA, ADC_GVAA,ADC_BVAA, BIAS_VAA,DPP_VAA, VCC	3.15	3.3	3.47	V
I_{DD}	Operating current	No Loading			600	mA
I_{DDPD}	Power down current	No Loading		20		mA
I_{OH1}	Output high current	(V_{OH} = 2.5V) DCLK,RA,GA,BA,RB,GB, BB,DISP_DE,DISP_HS,D ISP_VS	-16		-2	mA
I_{OL1}	Output low current	(V_{OL} = 0.4V) DCLK,RA,GA,BA,RB,GB BB,DISP_DE,DISP_HS,D ISP_VS	2		16	mA
I_{OH2}	Output high current	(V_{OH} = 2.5V) IRQn			-4	mA
I_{OL2}	Output low current	(V_{OL} = 0.4V) IRQn	4			mA
V_{IH}	Input high voltage		2.0			V
V_{IL}	Input low voltage				0.8	V
T_A	Ambient Operating Temperature		0		70	℃
T_C	Storage Temperature		-55		125	℃
T_J	Operating Junction Temperature				100	℃



Power -up Sequence

AC ELECTRICAL CHARACTERISTICS

(VDD=3.3V, TA=25°C, Oscillator freq.=12MHz, unless otherwise specified)

ADCPLL

Phase-locked loop						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
j_{PLL}	short term jitter	fclkout=135Mhz			500	ps
	long term jitter	fclkout=135Mhz			1.2	ns
DR	divider ratio	–	1		2048	
f_{CLKIN}	input clock frequency range	–	16		135	kHz
f_{CLKOUT}	output clock frequency range	–	16		135	MHz
t_{COAST}	maximum coast mode time	–		3		ms
δ	Clock out duty cycle	135 MHz output	45	50	55	%

Clamping Pulse						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
t_{DELAY}	clamp pulse delay time	CPC_delay<3:0>=0x00		0		CKOUT
		CPC_delay<3:0>=0x0F		15		CKOUT
t_{WIDTH}	clamp pulse width	CPC_width<3:0>=0x00		0		CKOUT
		CPC_width<3:0>=0x0F		15		CKOUT
tCOR1	clamp correction time to within ±10 mV	±100mV black level input variation; clamp capacitor=4.7nF		300		ns
tCOR2	clamp correction time to less than 1 LSB	±100mV black level input variation; clamp capacitor=4.7nF		10		Lines

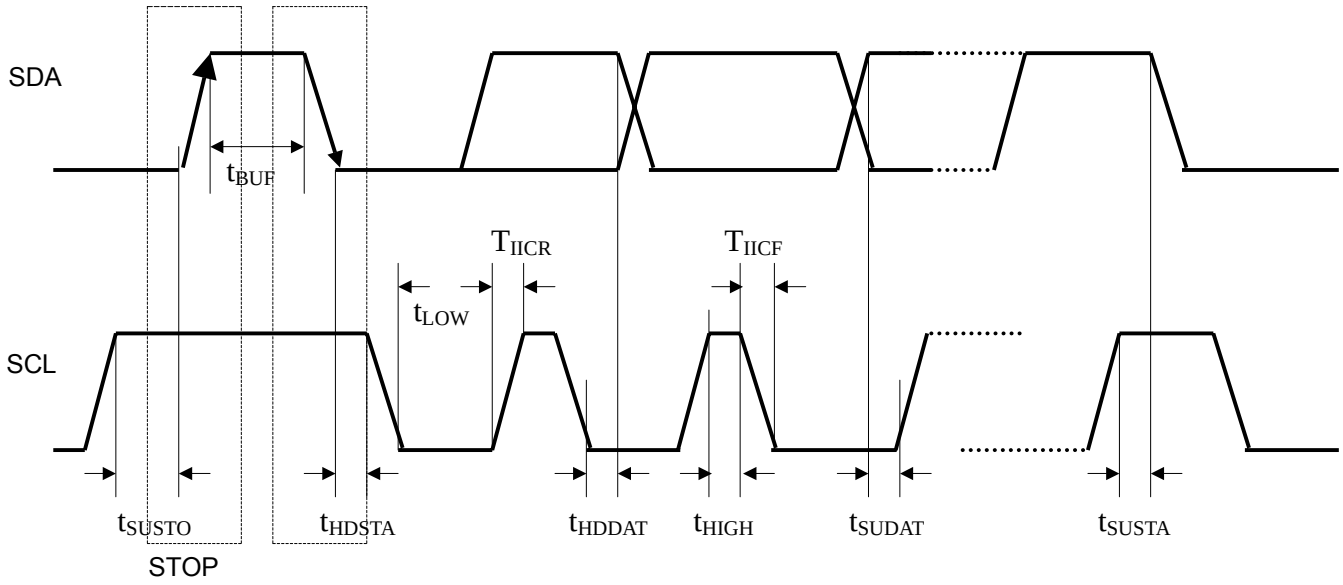
Variation Gain Amplifier						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
B	Bandwidth	—	150			Mhz
G	gain range	—	0.8		2.0	V/V
G_{STEP}	gain step size	—		1.7/255		V/V
G_{ERROR}	gain step size error	—			1/4	Step
G_{MATCH}	channel to channel match	—		5		%
Vin(p-p)	input signal voltage (peak-peak)	corresponding to full scale output	0.5	0.7	1.0	V
t_{STAB}	amplifier gain adjustment speed	Hsync active		25		mdb/μs

Analog-to-Digital Converter						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
fs	maximum sampling frequency		135			MHz
DNL	DC differential non-linearity	from analog input to digital output; ramp input f_{CLK} = 135MHz		±1.0		LSB
INL	DC integral non linearity	from analog input to digital output; ramp input f_{CLK} = 135MHz		±1.5		LSB
ENOB	effective number of bits	from analog input to digital output; 10KHz sine wave input; ramp input; f_{CLK}=135MHz		7		bits
THD	total harmonic distortion	Input 1V(p-p) and 10MHz		1		%

Signal-to-Noise Ratio						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
S/N	signal-to-noise ratio	maximum gain f_{CLK}=135MHz	—	45	—	dB
		Minimum gain f_{CLK}=135MHz	—	44	—	dB

I2C Bus

I2C Bus Timing				
symbol	Parameter	Min	Max	Unit
fSCL	SCL clock frequency	0.00	400	kHZ
tSUSTO	STOP setup time	0.60		us
tBUF	Bus free time between a STOP and START	1.30		us
tHDSTA	START hold time	0.60		us
tLOW	SCL clock pulse width low	1.30		us
tIICR	IIC bus rise time		300	ns
tHDDAT	DATA hold time	0.00		us
tHIGH	SCL clock pulse width high	0.60		us
tIICF	IIC bus fall time		300	ns
tSUDAT	Data setup time	100		ns
tSUSTA	START setup	0.60		us



BONDING DIAGRAM

	PAD	X	Y	QFP		PAD	X	Y	QFP
1	GND:G	-2639.23	2340.98	1	48	PAD_FASTMUTE	-2302.22	-2639.45	41
2	VCC:P	-2639.23	2238.64	2	49	VCC:P	-2179.24	-2639.45	42
3	VCC:P	-2639.23	2137.16	3	50	VCC:P	-2053.68	-2639.45	42
4	PAD_VCON	-2639.23	2034.82	4	51	'AD_TCON_ENABL	-1932.42	-2639.45	44
5	PAD_CZ	-2639.23	1932.48	5	52	GND:G	-1812.02	-2639.45	44
6	GND:G	-2639.23	1831	6	53	GND:G	-1699.36	-2639.45	44
7	GND:G	-2639.23	1728.66	7	54	VCC:P	-1554.02	-2639.45	45
8	VCC:P	-2639.23	1627.18	8	55	VCC:P	-1405.24	-2639.45	45
9	PAD_VREF	-2639.23	1524.84	9	56	VCC:P	-1257.32	-2639.45	46
10	PAD_TESTP	-2639.23	1423.36	10	57	PAD_BB_0	-1162.32	-2639.45	47
11	PAD_TESTN	-2639.23	1321.02	11	58	PAD_BB_1	-1067.32	-2639.45	48
12	VCC:P	-2639.23	1219.54	12	59	PAD_BB_2	-972.32	-2639.45	49
13	VCC:P	-2639.23	1118.06	12	60	PAD_BB_3	-877.32	-2639.45	50
14	GND:G	-2639.23	1015.72	13	61	PAD_BB_4	-782.32	-2639.45	51
15	GND:G	-2639.23	914.24	13	62	PAD_BB_5	-687.32	-2639.45	52
16	VCC:P	-2639.23	811.9	14	63	PAD_BB_6	-592.32	-2639.45	53
17	PAD_RIN	-2639.23	710.42	15	64	PAD_BB_7	-497.32	-2639.45	54
18	GND:G	-2639.23	608.08	16	65	GND:G	-402.32	-2639.45	55
19	VCC:P	-2639.23	506.6	17	66	GND:G	-307.32	-2639.45	55
20	VCC:P	-2639.23	405.12	17	67	PAD_GB_0	-212.32	-2639.45	56
21	GND:G	-2639.23	302.78	18	68	PAD_GB_1	-117.32	-2639.45	57
22	GND:G	-2639.23	201.3	18	69	PAD_GB_2	-22.32	-2639.45	58
23	PAD_VTOP	-2639.23	98.96	19	70	PAD_GB_3	72.68	-2639.45	59
24	PAD_VMID	-2639.23	-3.38	20	71	PAD_GB_4	167.68	-2639.45	60
25	PAD_VBOT	-2639.23	-104.86	21	72	PAD_GB_5	262.68	-2639.45	61
26	VCC:P	-2639.23	-207.2	22	73	PAD_GB_6	357.68	-2639.45	62
27	PAD_GIN	-2639.23	-308.68	23	74	PAD_GB_7	452.68	-2639.45	63
28	GND:G	-2639.23	-411.02	24	75	VCC:P	547.68	-2639.45	64
29	VCC:P	-2639.23	-512.5	25	76	VCC:P	642.68	-2639.45	64
30	VCC:P	-2639.23	-613.98	25	77	PAD_RB_0	737.68	-2639.45	65
31	GND:G	-2639.23	-716.32	26	78	PAD_RB_1	832.68	-2639.45	66
32	GND:G	-2639.23	-817.8	26	79	PAD_RB_2	927.68	-2639.45	67
33	VCC:P	-2639.23	-920.14	27	80	PAD_RB_3	1022.68	-2639.45	68
34	PAD_BIN	-2639.23	-1022.48	28	81	PAD_RB_4	1117.68	-2639.45	69
35	GND:G	-2639.23	-1123.96	29	82	PAD_RB_5	1212.68	-2639.45	70
36	VCC:P	-2639.23	-1225.44	30	83	PAD_RB_6	1307.68	-2639.45	71
37	GND:G	-2639.23	-1326.92	31	84	PAD_RB_7	1402.68	-2639.45	72
38	VCC:P	-2639.23	-1428.4	32	85	PAD_DISP_POLA	1497.68	-2639.45	73
39	GND:G	-2639.23	-1529.88	33	86	PAD_DISP_POLB	1592.68	-2639.45	74
40	GND:G	-2639.22	-1631.36	34	87	GND:G	1687.68	-2639.45	75
41	GND:G	-2639.23	-1732.84	34	88	GND:G	1807.68	-2639.45	76
42	PAD_OSCI	-2639.23	-1830.36	35	89	VCC:P	1927.68	-2639.45	77
43	PAD_OSCO	-2639.23	-1901.74	36	90	VCC:P	2047.68	-2639.45	78
44	PAD_NC8	-2639.23	-2001.16	37	91	PAD_DISP_DE	2167.68	-2639.45	79
45	PAD_VSYNCI	-2639.23	-2305.6	38	92	PAD_DISP_VS	2287.68	-2639.45	80
46	PAD_HSYNCI	-2639.23	-2102.64	39					
47	PAD_SOGI	-2639.22	-2204.11	40					

	PAD	X	Y	QFP
93	VCC:P	2640.09	-2306.46	81
94	VCC:P	2640.09	-2205.84	81
95	VCC:P	2640.09	-2105.22	82
96	VCC:P	2640.09	-2004.6	82
97	PAD_DISP_HS	2640.09	-1903.12	83
98	PAD_DISP_SPA	2640.09	-1802.5	84
99	PAD_DISP_SPB	2640.09	-1701.02	85
100	GND:G	2640.09	-1600.4	86
101	VCC:P	2640.09	-1498.92	87
102	GND:G	2640.09	-1398.3	88
103	GND:G	2640.09	-1296.82	89
104	PAD_DISP_CLKB	2640.09	-1196.32	90
105	PAD_DISP_CLKA	2640.09	-1101.32	91
106	PAD_RA_7	2640.09	-1006.32	92
107	PAD_RA_6	2640.09	-911.32	93
108	PAD_RA_5	2640.09	-816.32	94
109	PAD_RA_4	2640.09	-721.32	95
110	PAD_RA_3	2640.09	-626.32	96
111	PAD_RA_2	2640.09	-531.32	97
112	PAD_RA_1	2640.09	-436.32	98
113	PAD_RA_0	2640.09	-341.32	99
114	VCC:P	2640.09	-246.32	100
115	VCC:P	2640.09	-151.32	100
116	PAD_GA_7	2640.09	-56.32	101
117	PAD_GA_6	2640.09	38.68	102
118	PAD_GA_5	2640.09	133.68	103
119	PAD_GA_4	2640.09	228.68	104
120	PAD_GA_3	2640.09	323.68	105
121	PAD_GA_2	2640.09	418.68	106
122	PAD_GA_1	2640.09	513.68	107
123	PAD_GA_0	2640.09	608.68	108
124	GND:G	2640.09	703.68	109
125	GND:G	2640.09	798.68	109
126	PAD_BA_7	2640.09	893.68	110
127	PAD_BA_6	2640.09	988.68	111
128	PAD_BA_5	2640.09	1083.68	112
129	PAD_BA_4	2640.09	1178.68	113
130	PAD_BA_3	2640.09	1273.68	114
131	PAD_BA_2	2640.09	1368.68	115
132	PAD_BA_1	2640.09	1463.68	116
133	PAD_BA_0	2640.09	1558.68	117
134	VCC:P	2640.09	1653.68	118
135	GND:G	2640.09	1815.52	119
136	GND:G	2640.09	1935.06	119
137	VCC:P	2640.09	2075.24	120
138	VCC:P	2640.09	2186.18	120

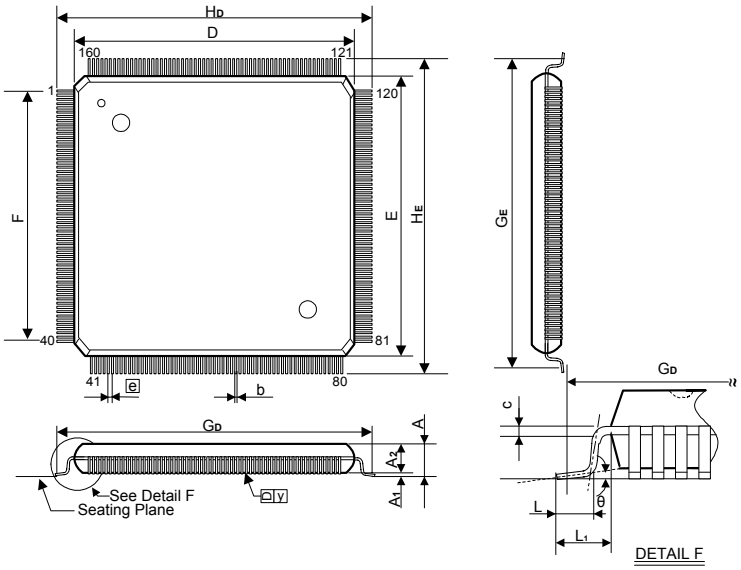
	PAD	X	Y	QFP
139	VCC:P	2640.09	2297.12	121
140	VCC:P	2342.64	2639.97	121
141	PAD_GPO0	2242.88	2639.97	122
142	PAD_GPO1	2143.98	2639.97	123
143	PAD_GPO2	2045.08	2639.97	124
144	PAD_GPO3	1946.18	2639.97	125
145	PAD_GPO4	1847.28	2639.97	126
146	PAD_GPO5	1748.38	2639.97	127
147	PAD_GPO6	1649.48	2639.97	128
148	PAD_GPO7	1550.58	2639.97	129
149	PAD_GPO8	1451.68	2639.97	130
150	PAD_GPO9	1352.78	2639.97	131
151	PAD_GPO10	1253.88	2639.97	132
152	PAD_GPO11	1154.98	2639.97	133
153	VCC:P	1054.36	2639.98	134
154	VCC:P	955.46	2639.98	134
155	GND:G	856.56	2639.97	135
156	GND:G	757.66	2639.97	135
157	GND:G	658.76	2639.97	135
158	GND:G	559.86	2639.97	135
159	PAD_Y_0	460.96	2639.97	136
160	PAD_Y_1	362.06	2639.97	137
161	PAD_Y_2	263.16	2639.97	138
162	PAD_Y_3	164.26	2639.97	139
163	PAD_Y_4	65.36	2639.97	140
164	PAD_Y_5	-33.54	2639.97	141
165	PAD_Y_6	-132.44	2639.97	142
166	PAD_Y_7	-231.34	2639.97	143
167	PAD_YUV_CLK	-330.24	2639.97	144
168	VCC:P	-429.12	2639.99	145
169	VCC:P	-528.04	2639.97	145
170	VCC:P	-626.94	2639.97	145
171	VCC:P	-725.84	2639.97	146
172	VCC:P	-824.74	2639.97	146
173	VCC:P	-923.64	2639.97	147
174	VCC:P	-1022.54	2639.97	147
175	PAD_NC1	-1121.44	2639.97	148
176	PAD_NC2	-1220.34	2639.97	149
177	PAD_NC3	-1319.24	2639.97	150
178	PAD_NC4	-1418.14	2639.97	151
179	PAD_NC5	-1517.04	2639.97	152
180	PAD_NC6	-1615.94	2639.97	153
181	PAD_SDA	-1714.84	2639.97	154
182	PAD_SCL	-1813.74	2639.98	155
183	PAD_IRQN	-1912.64	2639.97	156
184	PAD_NC7	-2011.54	2639.97	157
185	PAD_RSTN	-2110.44	2639.97	158
186	PAD_PBUSSEL	-2209.34	2639.98	159
187	GND:G	-2308.24	2639.97	160

ORDERING INFORMATION

Part No.	Type Function
NT68520XF	For XGA solution
NT68520EF	For SXGA solution

PACKAGE INFORMATION

QFP 160 Outline Dimensions unit: inches/mm



Symbol	Dimensions in inches	Dimensions in mm
A	0.145 Max.	3.68 Max.
A_1	0.004 Min.	0.10 Min.
A_2	0.127±0.005	3.23±0.13
b	0.012 $^{+0.004}_{-0.002}$	0.30 $^{+0.10}_{-0.05}$
c	0.006 $^{+0.004}_{-0.002}$	0.15 $^{+0.10}_{-0.05}$
D	1.102±0.005	28.00±0.13
E	1.102±0.005	28.00±0.13
e	□ 0.026±0.006	0.65±0.15
F	0.998 NOM.	25.35 NOM.
G_D	1.197 NOM.	30.40 NOM.
G_E	1.197 NOM.	30.40 NOM.
H_D	1.228±0.012	31.20±0.30
H_E	1.228±0.012	31.20±0.30
L	0.031±0.008	0.80±0.20
L_1	0.063±0.008	1.60±0.20
y	0.006 Max.	0.15 Max.
q	0° ~ 12°	0° ~ 12°

Notes:

1. Dimensions D and E do not include resin fins.
2. Dimensions F, G_D, G_E are for PC Board surface mount pad pitch
   design reference only.