Low Voltage 1:15 PECL to CMOS Clock Driver

MPC949

LOW VOLTAGE 1:15 PECL TO CMOS CLOCK DRIVER

FA SUFFIX
52–LEAD TQFP PACKAGE
CASE 848D–03

The MPC949 is a low voltage CMOS, 15 output clock buffer. The 15 outputs can be configured into a standard fanout buffer or into 1X and 1/2X combinations. The device features a low voltage PECL input, in addition to its LVCMOS/LVTTL inputs, to allow it to be incorporated into larger clock trees which utilize low skew PECL devices (see the MC100LVE111 data sheet) in the lower branches of the tree. The fifteen outputs were designed and optimized to drive 50Ω series or parallel terminated transmission lines. With output to output skews of 300ps the MPC949 is an ideal clock distribution chip for synchronous systems which need a tight level of skew from a large number of outputs. For a similar product with a smaller fanout and package consult the MPC946 data sheet.

- Clock Distribution for Pentium™ Systems with PCI
- Low Voltage PECL Clock Input
- 2 Selectable LVCMOS/LVTTL Clock Inputs
- 350ps Maximum Output to Output Skew
- Drives up to 30 Independent Clock Lines
- Maximum Output Frequency of 150MHz
- High Impedance Output Enable
- 52–Lead TQFP Packaging
- 3.3V V_{CC} Supply

With an output impedance of approximately 7Ω, in both the HIGH and the LOW logic states, the output buffers of the MPC949 are ideal for driving series terminated transmission lines. More specifically each of the 15 MPC949 outputs can drive two series terminated transmission lines. With this capability, the MPC949 has an effective fanout of 1:30 in applications using point–to–point distribution schemes.

The MPC949 has the capability of generating 1X and 1/2X signals from a 1X source. The design is fully static, the signals are generated and retimed inside the chip to ensure minimal skew between the 1X and 1/2X signals. The device features selectability to allow the user to select the ratio of 1X outputs to 1/2X outputs.

Two independent LVCMOS/LVTTL compatible clock inputs are available. Designers can take advantage of this feature to provide redundant clock sources or the addition of a test clock into the system design. With the TCLK_Sel input pulled HIGH the TCLK1 input is selected. The PCLK_Sel input will select the PECL input clock when driven HIGH.

All of the control inputs are LVCMOS/LVTTL compatible. The Dsel pins choose between 1X and 1/2X outputs. A LOW on the Dsel pins will select the 1X output. The MR/OE input will reset the internal flip flops and tristate the outputs when it is forced HIGH.

The MPC949 is fully 3.3V compatible. The 52 lead TQFP package was chosen to optimize performance, board space and cost of the device. The 52–lead TQFP has a 10x10mm body size with a 0.65mm pin spacing.

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Figure 1. Logic Diagram

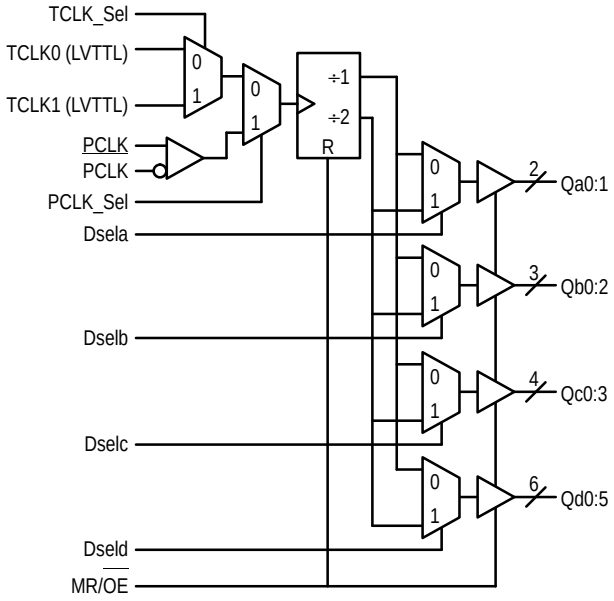
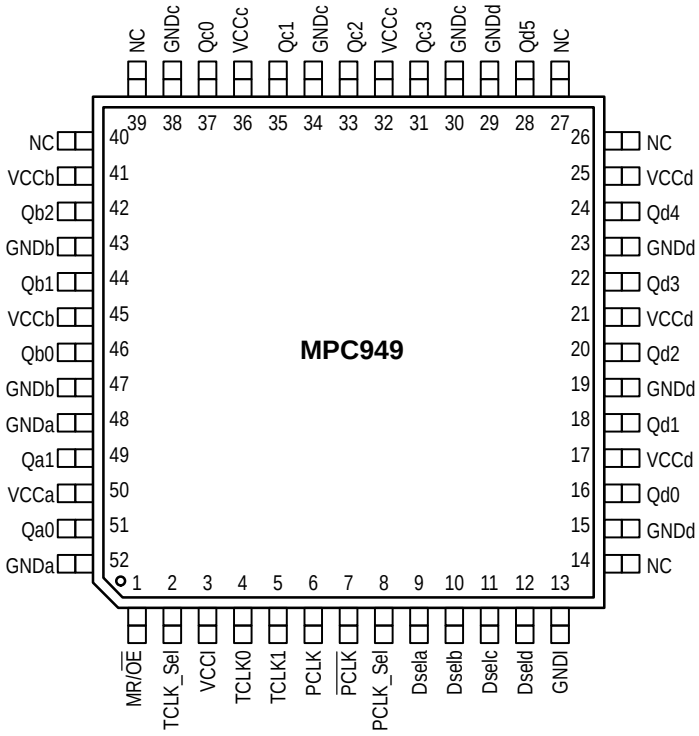


Figure 2. 52–Lead Pinout (Top View)



FUNCTION TABLE

Input	0	1
TCLK_Sel	TCLK0	TCLK1
PCLK_Sel	TCLKn	PCLK
Dseln	÷1	÷2
MR/OE	Enabled	Hi–Z

PIN DESCRIPTION

Pin Name	Function
TCLK_Sel (Int Pulldown)	Select pin to choose TCKL0 or TCLK1
TCLK0:1 (Int Pullup)	LVCMOS/LVTTL clock inputs
PCLK (Int Pulldown)	True PECL clock input
PCLK (Int Pullup)	Compliment PECL clock input
Dseln (Int Pulldown)	1x or 1/2x input divide select pins
MR/OE (Int Pulldown)	Internal reset and output tristate control pin
PCLK_Sel (Int Pulldown)	Select Pin to choose TCLK or PCLK

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	4.6	V
V_I	Input Voltage	–0.3	V_{DD} + 0.3	V
I_{IN}	Input Current	TBD	TBD	mA
T_{Stor}	Storage Temperature Range	–40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

DC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage (Except PECL_CLK)	2.0		3.60	V	
V_{IL}	Input LOW Voltage (Except PECL_CLK)			0.8	V	
V_{PP}	Peak–to–Peak Input Voltage PECL_CLK	300		1000	mV	
V_{CMR}	Common Mode Range PECL_CLK	V_{CC} – 2.0		V_{CC} – 0.6	V	Note 1.
V_{OH}	Output HIGH Voltage	2.5			V	I_{OH} = –20mA (Note 2.)
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 20mA (Note 2.)
I_{IN}	Input Current			±120	µA	Note 3.
C_{IN}	Input Capacitance			4	pF	
C_{pd}	Power Dissipation Capacitance		25		pF	Per Output
I_{CC}	Maximum Quiescent Supply Current		70	85	mA	

1. V_{CMR} is the difference from the most positive side of the differential input signal. Normal operation is obtained when the “HIGH” input is within the V_{CMR} range and the input swing lies within the V_{PP} specification.
2. The MPC949 outputs can drive series or parallel terminated 50Ω (or 50Ω to V_{CC}/2) transmission lines on the incident edge (see Applications Info section).
3. Inputs have pull–up/pull–down resistors which affect input current.

AC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
F_{max}	Maximum Input Frequency	150			MHz	Note 4.
t_{PLH}	Propagation Delay PECL_CLK to Q TTL_CLK to Q	4.0 4.2	6.5 7.5	9.0 10.6	ns	Note 4.
t_{PHL}	Propagation Delay PECL_CLK to Q TTL_CLK to Q	3.8 4.0	6.2 7.2	8.6 10.5	ns	Note 4.
$t_{sk(o)}$	Output–to–Output Skew		300	350	ps	Note 4.
$t_{sk(pr)}$	Part–to–Part Skew PECL_CLK to Q TTL_CLK to Q		1.5 2.0	2.75 4.0	ns	Note 5.
t_{PZL},t_{PZH}	Output Enable Time		3	11	ns	Note 4.
t_{PLZ},t_{PHZ}	Output Disable Time		3	11	ns	Note 4.
t_r, t_f	Output Rise/Fall Time	0.10		1.0	ns	0.8V to 2.0V

4. Driving 50Ω transmission lines terminated to V_{CC}/2.
5. Part–to–part skew at a given temperature and voltage.

APPLICATIONS INFORMATION

Driving Transmission Lines

The MPC949 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user, the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions brochure (BR1333/D).

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to VCC/2. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC949 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 3 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC949 clock driver is effectively doubled due to its capability to drive multiple lines.

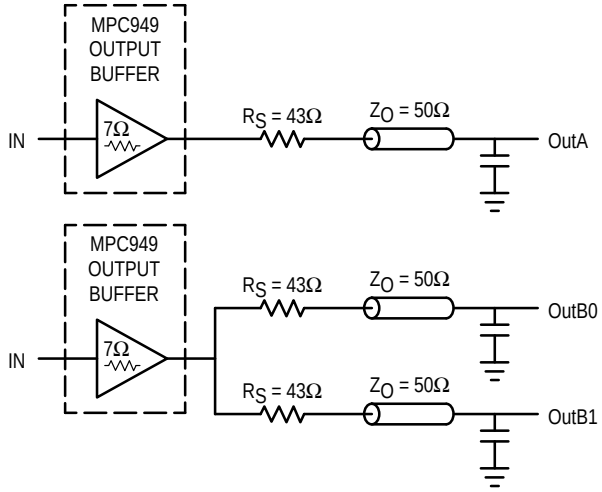


Figure 3. Single versus Dual Transmission Lines

The waveform plots of Figure 4 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC949 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC949. The output waveform in Figure 4 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$VL = VS (Zo / Rs + Ro + Zo) = 3.0 (25/53.5) = 1.40V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

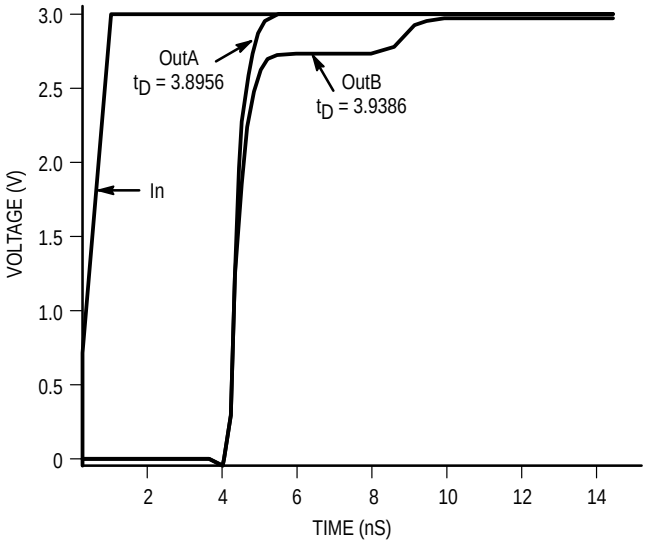
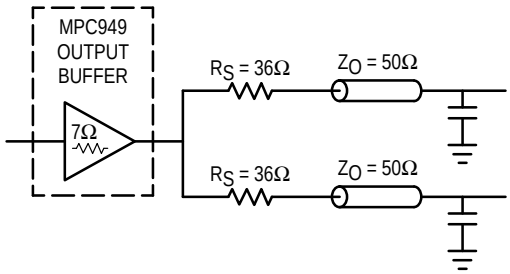


Figure 4. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 5 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



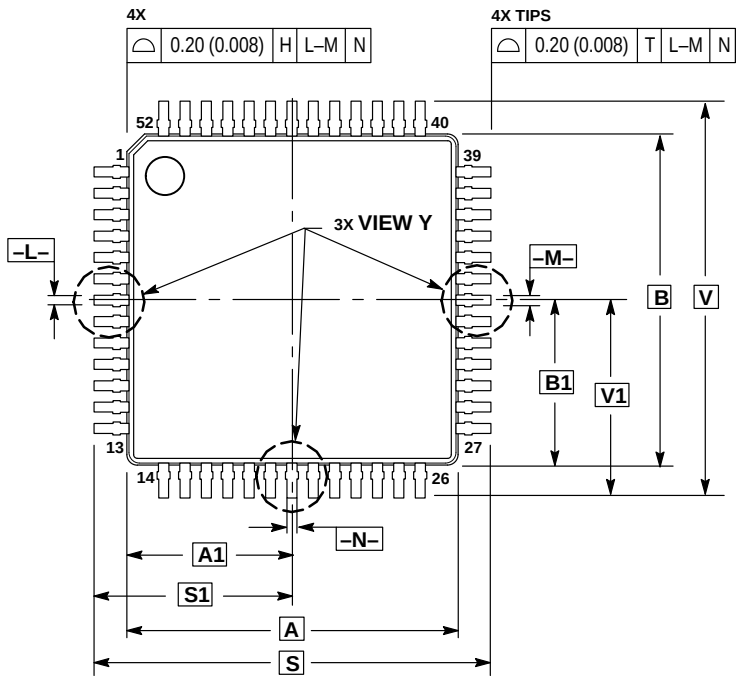
$$7\Omega + 36\Omega \parallel 36\Omega = 50\Omega \parallel 50\Omega$$
$$25\Omega = 25\Omega$$

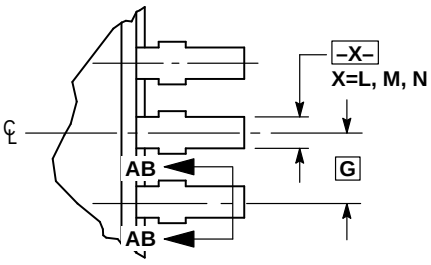
Figure 5. Optimized Dual Line Termination

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

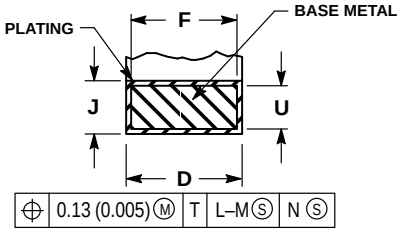
OUTLINE DIMENSIONS

FA SUFFIX
TQFP PACKAGE
CASE 848D–03
ISSUE C

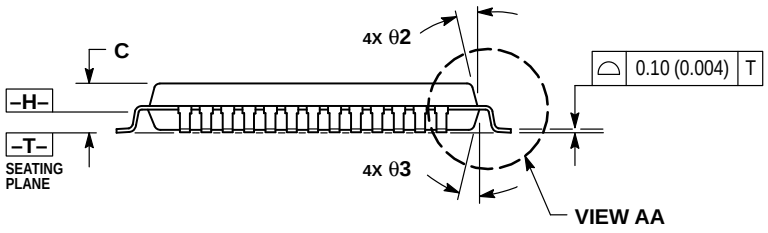




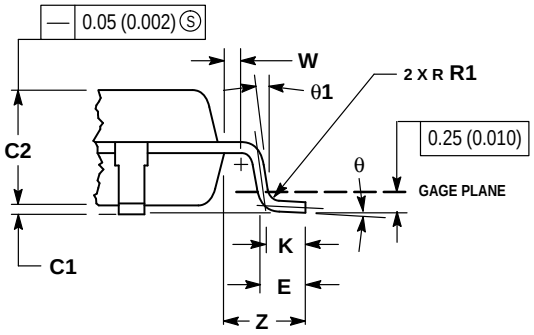
VIEW Y



SECTION AB–AB
ROTATED 90° CLOCKWISE



VIEW AA



VIEW AA

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –L–, –M– AND –N– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –T–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 (0.018). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 (0.003).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.00 BSC		0.394 BSC	
A1	5.00 BSC		0.197 BSC	
B	10.00 BSC		0.394 BSC	
B1	5.00 BSC		0.197 BSC	
C	—	1.70	—	0.067
C1	0.05	0.20	0.002	0.008
C2	1.30	1.50	0.051	0.059
D	0.20	0.40	0.008	0.016
E	0.45	0.75	0.018	0.030
F	0.22	0.35	0.009	0.014
G	0.65 BSC		0.026 BSC	
J	0.07	0.20	0.003	0.008
K	0.50 REF		0.020 REF	
R1	0.08	0.20	0.003	0.008
S	12.00 BSC		0.472 BSC	
S1	6.00 BSC		0.236 BSC	
U	0.09	0.16	0.004	0.006
V	12.00 BSC		0.472 BSC	
V1	6.00 BSC		0.236 BSC	
W	0.20 REF		0.008 REF	
Z	1.00 REF		0.039 REF	
θ	0°	7°	0°	7°
θ1	0°	—	0°	—
θ2	12° REF		12° REF	
θ3	5°	13°	5°	13°

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