Panasonic

Opposing corner 7.17mm(1/2.5type) 3.34 million pixels

CCD Area Image Censor MN39592PJ

Overview

MN39592PJ is a CCD $\frac{1}{2.5}$ 3.34 million pixels area image sensor suits high-quality digital still camera.On-chip color filter presents excellent color repeatability by adopting RGB bayer. It also keeps 3.34 million total number of pixels(Horizontally:2.140 × Vertically: 1.560) to hold stable and high-quality pictures.

$V \phi V 4$ Top view 16 V φ H 2 15 V φ H 1 $V \phi V 6$ 2 3 VРΤ V φ V З 14 13 BSUB $V \phi V 2$ 4 $V \phi V 5$ 5 12 VSUB $V \phi V 1$ 6 11 P W 10 V \u03c6 R G VOG 7 VΟ 8 9 VOD

Features

- •Available pixel number 2.088(horizoontal), 1,550(vertical)
- Supersensitivity
- •Low-smear
- •Square pixel alignment
- •Lower power consumption by adopting horizontal CCD, 3.3V
- •16-pin plastic package

Applications

Digital still camera

The products and specifications are subject to change without notice. Please ask for the latest Product Standards to guarantee the satisfaction of your product requirements.

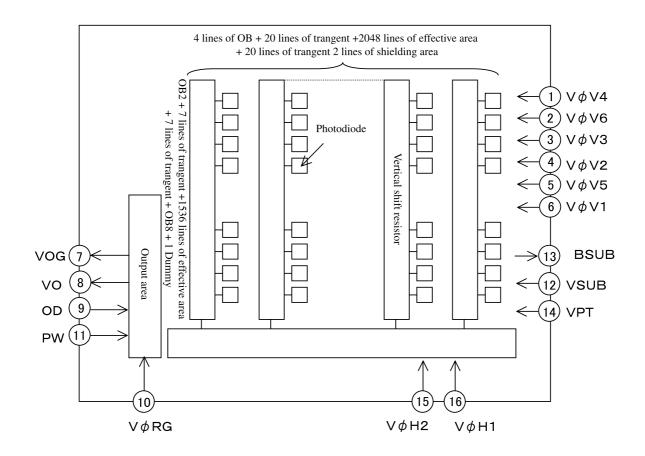
Semiconductor Company, Matsushita Electric Industrial Co., Ltd.

1 Kotari-yakemachi, Nagaokakyo, Kyoto 617-8520, Japan E00125AE

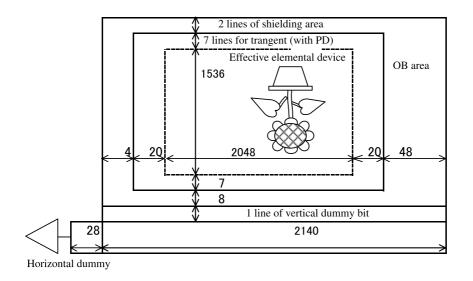
Tel. (075)951-8151

http://www.panasonic.co.jp/semicon/ New publication, effective from Jun.04 2002.

Block Diagram



Elemental device structure

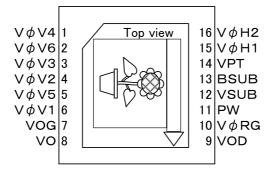


Terminal description

1. Terminal description

Terminal No	Name	Terminal description
1 pin	V¢V4	Vertical shift register clock pulse (4)
2 pin	V¢V6	Vertical shift register clock pulse (6)
3 pin	V¢V3	Vertical shift register clock pulse (3)
4 pin	V¢V2	Vertical shift register clock pulse (2)
5 pin	V _{\$} V5	Vertical shift register clock pulse (5)
6 pin	V¢V1	Vertical shift register clock pulse (1)
7 pin	VOG	Output gate
8 pin	VO	CCD output
9 pin	VOD	Output drain
10 pin	VøRG	Reset pulse
11 pin	PW	GND
12 pin	VSUB	Circuit board
13 pin	BSUB	Breeder SUB
14 pin	VPT	Protection P wel
15 pin	VøH1	Horizontal shift resistor clock pulse (1)
16 pin	VøH2	Horizontal shift resistor clock pulse (2)

2. Alignment of terminals



3. Device parameter

Parameter	Numeric value	Unit
Total pixel number	$2,140(H) \times 1,560(V) = 3,338,400$	pcs
Available pixel number (including trangents)	$2,088(H) \times 1,550(V) = 3,236,400$	\mathbf{pcs}
Effective pixel numbers	$2,048(H) \times 1,536(V) = 3,145,728$	pcs
Pixel size	2.8× 2.8	μm ²
Effective picture size	5.7344(H) × 4.3008(V)	μm ²

Absolute maximum ratings

Terminal 1	Terminal name		PW		РТ		SUB	
	Unit	High	Low	High	Low	High	Low	Note
VOD	V	15.0	-0.2	_		15.0	-25.0	Note 1,2
VPT	V	0.2	-10.0	Stan	dard	0.2	-35.0	
PW	V	Stan	dard	10.0 -0.2		0.2 -25.0		
Vsub	V	25.0	-0.2	35.0 -0.2		Standard		Note 1
BSUB	V	15.0	-0.2	-		15.0	-25.0	
VOG	V	5.0	-0.2	-		5.0	-25.0	
VøRG	V	5.0	-0.2	15.0	-0.2	5.0	-25.0	
VøH1	V	5.0	-0.2	15.0	-0.2	5.0	-25.0	
VøH2	V	5.0	-0.2	15.0	-0.2	5.0	-25.0	
V¢V1, 5	V	15.0	-10.0	25.0	-0.2	15.0	-35.0	
V¢V2	V	12.0	-10.0	22.0 -0.2		12.0	-35.0	
VøV3,6	V	15.0	-10.0	25.0	-0.2	15.0	-35.0	
V¢V4	V	12.0	-10.0	22.0	-0.2	12.0	-35.0	
VO	V	15.0	-10.0		-		-35.0	Note 2

Absolute maximum ratings between gates

Terminal name	Unit	High	Low	Note
Horizontal clock input terminal (between V $\phi V1$ and V $\phi V6)$	V	12.0	-10.0	Note 3
Vertical clock input terminal (between V $\psi V1$ and V $\psi V6)$	V	5.0	-5.0	
V\$H1-V\$V4	V	12.0	-12.0	

■ Operation temperature

Parameter	Unit	High	Low	Note
Operation temperature		60	-10.0	

Note 1. Always keep VOD-Vsub 10V.

Note 2. Always keep VOD-VO 5V.

Note 3. When clock width < 10 μ s, Dudy<0.1%, 25V is guaranteed.

Imaging characteristics

Testing specification (Tentative)

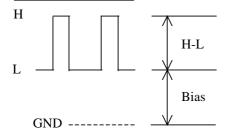
Parameter		Symbol	Condition	Test point	Min.	Standard	Max.	Unit
Saturation	power	Vsat	F1.4:J chart	Signal output		550		mV
	(G)	SoG	F8:J chart (1/7.5	Signal output	200	235	285	
Sensitivity	(R)	SoR	accumulated	Signal output	120	165	205	mV
	(B)	SoB	conversion value)	Signal output	90	110	140	
Sensitivity	R/G		Sensitivity	Signal output	0.42	0.70	1.03	
ratio	B/G		measurement conditions	Signal output	0.31	0.47	0.70	
C	Frame	Sm	1/1011	C signal output		-87	-81	ID
Smear	monitors	Sm	1/10V	G signal output		-77	-71	dB
OB bur	np		60°C light shielding	Signal output	-0.6	0	0.6	mV
Color shading (1)(2)			Standard light sensitivity	Average signal output		4.0	8.0	%
Dark signal			Ta=60°C,1/5.24 second accumulation shielding condition	Signal output		3.0	6.0	mV
Dark signal shading (H, V)			Ta=60°C,1/5.24 second accumulation shielding condition	Signal output		4.0	6.0	mV
Blooming control circuit voltage		Vsub	1000 times more light than normal amount	Monitor	No blooming caused by the inr voltage of Vsub		e inner	
φ VH voltage reliability (Shutter with a scratch)			1/8 times more light than normal amount	Monitor	No scratches under the conditi of \$\$\phi\$ VH voltage operation			
OB transmission			One hundred thousand times more light than normal amount	Signal output	Less	Less than 10mV of OB signal output		

Note: above values are testing values only.

\blacksquare Clock power voltage conditions

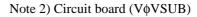
Terminal name			0			
		Unit	Max.	Standard	Min.	Note
VOD		V	12.0	12.0	-11.5	
VPT		V	-7.5	-8.0	-8.5	
PW		V	-	0	-	
VOG		V	Inside			
VøRG	H-L		3.6	3.3	3.0	Note 1
	Bias	V		Inside		Note 1
VøH1	Н	V	3.6	3.3	3.0	
	L	V	0.2	0	-0.2	Note 3
V¢H2	Н	V	3.6	3.3	3.0	Note 3
	L	V	0.2	0	-0.2	
Vsub	Bias	V	Inside			Note2
	φVsub	V	21.0	20.0	19.0	INOLEZ
V¢V1	Н	V	12.5	12.0	11.5	
V¢V5	М	V	0.2	0	-0.2	
	L	V	-7.5	-8.0	-8.5	
V¢V2	М	V	0.2	0	-0.2	
	L	V	-7.5	-8.0	-8.5	Note 4
V¢V3	Н	V	12.5	12.0	11.5	Note 4
V¢V6	М	V	0.2	0	-0.2	
	L	V	-7.5	-8.0	-8.5	
V¢V4	М	V	0.2	0	-0.2	
	L	V	-7.5	-8.0	-8.5	
IOD		mA		43		

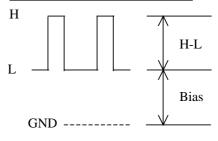
Note 1) Reset (V\u00f6RG)

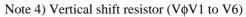


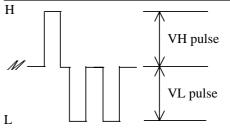
Note 3) Horizontal shift resistor (V ϕ H1, V ϕ H2)



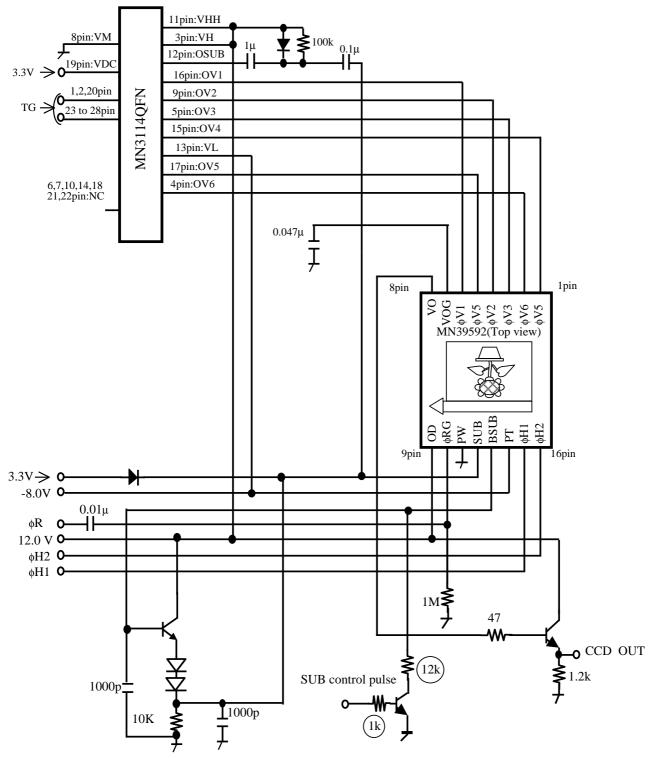






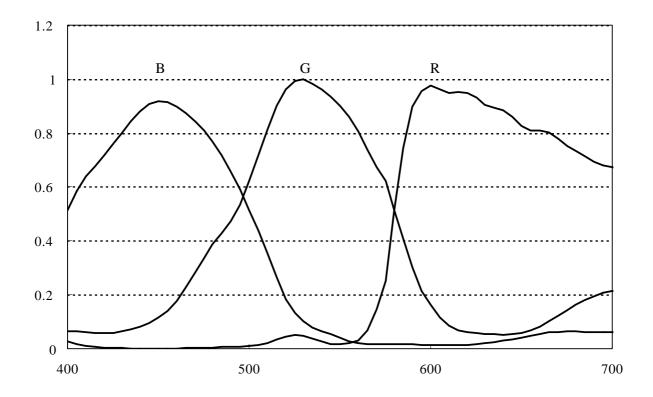


■ Recommended circuit example



Adjustment of Base resistance $1k\Omega$ is required depending on the ability of current supply of SUB control pulse output circuit.

■ Characteristics of prismatic



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