

FEATURES

- 25MHz Gain-Bandwidth
- 600V/ μ s Slew Rate
- 2.5mA Maximum Supply Current per Amplifier
- Unity Gain Stable
- C-Load™ Op Amp Drives All Capacitive Loads
- 8nV/ $\sqrt{\text{Hz}}$ Input Noise Voltage
- 600 μ V Maximum Input Offset Voltage
- 500nA Maximum Input Bias Current
- 120nA Maximum Input Offset Current
- 20V/mV Minimum DC Gain, $R_L=1k$
- 115ns Settling Time to 0.1%, 10V Step
- 220ns Settling Time to 0.01%, 10V Step
- $\pm 12.5\text{V}$ Minimum Output Swing into 500 Ω
- $\pm 3\text{V}$ Minimum Output Swing into 150 Ω
- Specified at $\pm 2.5\text{V}$, $\pm 5\text{V}$, and $\pm 15\text{V}$

APPLICATIONS

- Wideband Amplifiers
- Buffers
- Active Filters
- Data Acquisition Systems
- Photodiode Amplifiers

DESCRIPTION

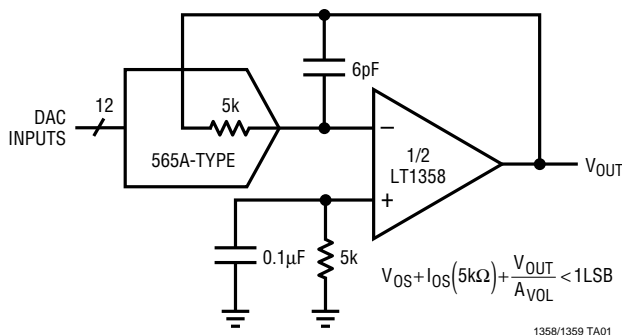
The LT1358/LT1359 are dual and quad low power high speed operational amplifiers with outstanding AC and DC performance. The amplifiers feature much lower supply current and higher slew rate than devices with comparable bandwidth. The circuit topology is a voltage feedback amplifier with matched high impedance inputs and the slewing performance of a current feedback amplifier. The high slew rate and single stage design provide excellent settling characteristics which make the circuit an ideal choice for data acquisition systems. Each output drives a 500 Ω load to $\pm 12.5\text{V}$ with $\pm 15\text{V}$ supplies and a 150 Ω load to $\pm 3\text{V}$ on $\pm 5\text{V}$ supplies. The amplifiers are stable with any capacitive load making them useful in buffer applications.

The LT1358/LT1359 are members of a family of fast, high performance amplifiers using this unique topology and employing Linear Technology Corporation's advanced bipolar complementary processing. For a single amplifier version of the LT1358/LT1359 see the LT1357 data sheet. For higher bandwidth devices with higher supply currents see the LT1360 through LT1365 data sheets. For lower supply current amplifiers see the LT1354 and LT1355/LT1356 data sheets. Singles, duals, and quads of each amplifier are available.

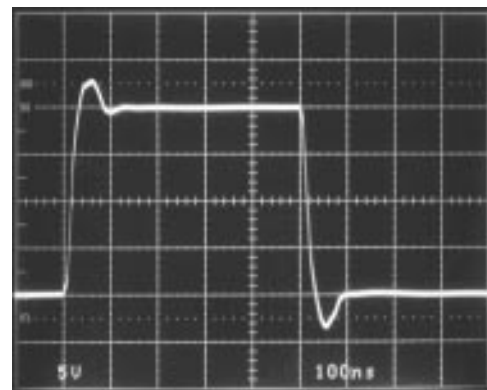
C-Load is a trademark of Linear Technology Corporation

TYPICAL APPLICATION

DAC I-to-V Converter



$A_V = -1$ Large-Signal Response



ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 36V
 Differential Input Voltage $\pm 10V$
 Input Voltage $\pm V_S$
 Output Short-Circuit Duration (Note 1) Indefinite
 Operating Temperature Range $-40^\circ C$ to $85^\circ C$

Specified Temperature Range $-40^\circ C$ to $85^\circ C$
 Maximum Junction Temperature (See Below)
 Plastic Package $150^\circ C$
 Storage Temperature Range $-65^\circ C$ to $150^\circ C$
 Lead Temperature (Soldering, 10 sec) $300^\circ C$

PACKAGE/ORDER INFORMATION

<p>TOP VIEW</p> <p>OUT A 1, -IN A 2, +IN A 3, V^- 4, 5 +IN B, 6 -IN B, 7 OUT B, 8 V^+</p> <p>N8 PACKAGE 8-LEAD PLASTIC DIP $T_{JMAX} = 150^\circ C, \theta_{JA} = 130^\circ C/W$</p>	<p>ORDER PART NUMBER</p> <p>LT1358CN8</p>	<p>TOP VIEW</p> <p>OUT A 1, -IN A 2, +IN A 3, V^- 4, 5 +IN B, 6 -IN B, 7 OUT B, 8 V^+</p> <p>S8 PACKAGE 8-LEAD PLASTIC SOIC $T_{JMAX} = 150^\circ C, \theta_{JA} = 190^\circ C/W$</p>	<p>ORDER PART NUMBER</p> <p>LT1358CS8</p> <p>S8 PART MARKING</p> <p>1358</p>
<p>TOP VIEW</p> <p>OUT A 1, -IN A 2, +IN A 3, V^+ 4, +IN B 5, -IN B 6, OUT B 7, 8 OUT C, 9 -IN C, 10 +IN C, 11 V^-, 12 +IN D, 13 -IN D, 14 OUT D</p> <p>N PACKAGE 14-LEAD PLASTIC DIP $T_{JMAX} = 150^\circ C, \theta_{JA} = 110^\circ C/W$</p>	<p>ORDER PART NUMBER</p> <p>LT1359CN</p>	<p>TOP VIEW</p> <p>OUT A 1, -IN A 2, +IN A 3, V^+ 4, +IN B 5, -IN B 6, OUT B 7, NC 8, 9 NC, 10 OUT C, 11 -IN C, 12 +IN C, 13 V^-, 14 +IN D, 15 -IN D, 16 OUT D</p> <p>S PACKAGE 16-LEAD PLASTIC SOIC $T_{JMAX} = 150^\circ C, \theta_{JA} = 150^\circ C/W$</p>	<p>ORDER PART NUMBER</p> <p>LT1359CS</p>

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS $T_A = 25^\circ C, V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		$\pm 15V$	0.2	0.6		mV
			$\pm 5V$	0.2	0.6		mV
			$\pm 2.5V$	0.3	0.8		mV
I_{OS}	Input Offset Current		$\pm 2.5V$ to $\pm 15V$	40	120		nA
I_B	Input Bias Current		$\pm 2.5V$ to $\pm 15V$	120	500		nA
e_n	Input Noise Voltage	$f = 10kHz$	$\pm 2.5V$ to $\pm 15V$	8			nV/\sqrt{Hz}
i_n	Input Noise Current	$f = 10kHz$	$\pm 2.5V$ to $\pm 15V$	0.8			pA/\sqrt{Hz}
R_{IN}	Input Resistance	$V_{CM} = \pm 12V$	$\pm 15V$	35	80		$M\Omega$
		Differential	$\pm 15V$	6			$M\Omega$
C_{IN}	Input Capacitance		$\pm 15V$	3			pF

ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CM} = 0\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
	Input Voltage Range ⁺		$\pm 15\text{V}$	12.0	13.4		V
			$\pm 5\text{V}$	2.5	3.5		V
			$\pm 2.5\text{V}$	0.5	1.1		V
	Input Voltage Range ⁻		$\pm 15\text{V}$	-13.2	-12.0		V
			$\pm 5\text{V}$	-3.3	-2.5		V
			$\pm 2.5\text{V}$	-0.9	-0.5		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 12\text{V}$	$\pm 15\text{V}$	83	97		dB
		$V_{CM} = \pm 2.5\text{V}$	$\pm 5\text{V}$	78	84		dB
		$V_{CM} = \pm 0.5\text{V}$	$\pm 2.5\text{V}$	68	75		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.5\text{V}$ to $\pm 15\text{V}$		92	106		dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm 12\text{V}$, $R_L = 1\text{k}$	$\pm 15\text{V}$	20	65		V/mV
		$V_{OUT} = \pm 10\text{V}$, $R_L = 500\Omega$	$\pm 15\text{V}$	7	25		V/mV
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 1\text{k}$	$\pm 5\text{V}$	20	45		V/mV
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 500\Omega$	$\pm 5\text{V}$	7	25		V/mV
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 150\Omega$	$\pm 5\text{V}$	1.5	6		V/mV
		$V_{OUT} = \pm 1\text{V}$, $R_L = 500\Omega$	$\pm 2.5\text{V}$	7	30		V/mV
V_{OUT}	Output Swing	$R_L = 1\text{k}$, $V_{IN} = \pm 40\text{mV}$	$\pm 15\text{V}$	13.3	13.8		$\pm\text{V}$
		$R_L = 500\Omega$, $V_{IN} = \pm 40\text{mV}$	$\pm 15\text{V}$	12.5	13.0		$\pm\text{V}$
		$R_L = 500\Omega$, $V_{IN} = \pm 40\text{mV}$	$\pm 5\text{V}$	3.5	4.0		$\pm\text{V}$
		$R_L = 150\Omega$, $V_{IN} = \pm 40\text{mV}$	$\pm 5\text{V}$	3.0	3.3		$\pm\text{V}$
		$R_L = 500\Omega$, $V_{IN} = \pm 40\text{mV}$	$\pm 2.5\text{V}$	1.3	1.7		$\pm\text{V}$
I_{OUT}	Output Current	$V_{OUT} = \pm 12.5\text{V}$	$\pm 15\text{V}$	25	30		mA
		$V_{OUT} = \pm 3\text{V}$	$\pm 5\text{V}$	20	25		mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0\text{V}$, $V_{IN} = \pm 3\text{V}$	$\pm 15\text{V}$	30	42		mA
SR	Slew Rate	$A_V = -2$, (Note 2)	$\pm 15\text{V}$	300	600		V/ μs
			$\pm 5\text{V}$	150	220		V/ μs
	Full Power Bandwidth	10V Peak, (Note 3) 3V Peak, (Note 3)	$\pm 15\text{V}$		9.6		MHz
			$\pm 5\text{V}$		11.7		MHz
GBW	Gain-Bandwidth	$f = 200\text{kHz}$, $R_L = 2\text{k}$	$\pm 15\text{V}$	18	25		MHz
			$\pm 5\text{V}$	15	22		MHz
			$\pm 2.5\text{V}$		20		MHz
t_r , t_f	Rise Time, Fall Time	$A_V = 1$, 10%-90%, 0.1V	$\pm 15\text{V}$		8		ns
			$\pm 5\text{V}$		9		ns
	Overshoot	$A_V = 1$, 0.1V	$\pm 15\text{V}$		27		%
			$\pm 5\text{V}$		27		%
	Propagation Delay	50% V_{IN} to 50% V_{OUT} , 0.1V	$\pm 15\text{V}$		9		ns
			$\pm 5\text{V}$		11		ns
t_s	Settling Time	10V Step, 0.1%, $A_V = -1$	$\pm 15\text{V}$		115		ns
		10V Step, 0.01%, $A_V = -1$	$\pm 15\text{V}$		220		ns
		5V Step, 0.1%, $A_V = -1$	$\pm 5\text{V}$		110		ns
		5V Step, 0.01%, $A_V = -1$	$\pm 5\text{V}$		380		ns
	Differential Gain	$f = 3.58\text{MHz}$, $A_V = 2$, $R_L = 1\text{k}$	$\pm 15\text{V}$		0.1		%
			$\pm 5\text{V}$		0.1		%
	Differential Phase	$f = 3.58\text{MHz}$, $A_V = 2$, $R_L = 1\text{k}$	$\pm 15\text{V}$		0.50		Deg
			$\pm 5\text{V}$		0.35		Deg
R_O	Output Resistance	$A_V = 1$, $f = 100\text{kHz}$	$\pm 15\text{V}$		0.3		Ω
	Channel Separation	$V_{OUT} = \pm 10\text{V}$, $R_L = 500\Omega$	$\pm 15\text{V}$	100	113		dB
I_S	Supply Current	Each Amplifier	$\pm 15\text{V}$		2.0	2.5	mA
			$\pm 5\text{V}$		1.9	2.4	mA

ELECTRICAL CHARACTERISTICS $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$, $V_{CM} = 0\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		$\pm 15\text{V}$	●		0.8	mV
			$\pm 5\text{V}$	●		0.8	mV
			$\pm 2.5\text{V}$	●		1.0	mV
	Input V_{OS} Drift	(Note 4)	$\pm 2.5\text{V}$ to $\pm 15\text{V}$	●	5	8	$\mu\text{V}/^{\circ}\text{C}$
I_{OS}	Input Offset Current		$\pm 2.5\text{V}$ to $\pm 15\text{V}$	●		180	nA
I_B	Input Bias Current		$\pm 2.5\text{V}$ to $\pm 15\text{V}$	●		750	nA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 12\text{V}$ $V_{CM} = \pm 2.5\text{V}$ $V_{CM} = \pm 0.5\text{V}$	$\pm 15\text{V}$	●	81		dB
			$\pm 5\text{V}$	●	77		dB
			$\pm 2.5\text{V}$	●	67		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.5\text{V}$ to $\pm 15\text{V}$		●	90		dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm 12\text{V}$, $R_L = 1\text{k}$ $V_{OUT} = \pm 10\text{V}$, $R_L = 500\Omega$ $V_{OUT} = \pm 2.5\text{V}$, $R_L = 1\text{k}$ $V_{OUT} = \pm 2.5\text{V}$, $R_L = 500\Omega$ $V_{OUT} = \pm 2.5\text{V}$, $R_L = 150\Omega$ $V_{OUT} = \pm 1\text{V}$, $R_L = 500\Omega$	$\pm 15\text{V}$	●	15		V/mV
			$\pm 15\text{V}$	●	5		V/mV
			$\pm 5\text{V}$	●	15		V/mV
			$\pm 5\text{V}$	●	5		V/mV
			$\pm 5\text{V}$	●	1		V/mV
			$\pm 2.5\text{V}$	●	5		V/mV
V_{OUT}	Output Swing	$R_L = 1\text{k}$, $V_{IN} = \pm 40\text{mV}$ $R_L = 500\Omega$, $V_{IN} = \pm 40\text{mV}$ $R_L = 500\Omega$, $V_{IN} = \pm 40\text{mV}$ $R_L = 150\Omega$, $V_{IN} = \pm 40\text{mV}$ $R_L = 500\Omega$, $V_{IN} = \pm 40\text{mV}$	$\pm 15\text{V}$	●	13.2		$\pm\text{V}$
			$\pm 15\text{V}$	●	12.2		$\pm\text{V}$
			$\pm 5\text{V}$	●	3.4		$\pm\text{V}$
			$\pm 5\text{V}$	●	2.8		$\pm\text{V}$
			$\pm 2.5\text{V}$	●	1.2		$\pm\text{V}$
I_{OUT}	Output Current	$V_{OUT} = \pm 12.2\text{V}$ $V_{OUT} = \pm 2.8\text{V}$	$\pm 15\text{V}$	●	24.4		mA
			$\pm 5\text{V}$	●	18.7		mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0\text{V}$, $V_{IN} = \pm 3\text{V}$	$\pm 15\text{V}$	●	25		mA
SR	Slew Rate	$A_V = -2$, (Note 2)	$\pm 15\text{V}$	●	225		V/ μs
			$\pm 5\text{V}$	●	125		V/ μs
GBW	Gain-Bandwidth	$f = 200\text{kHz}$, $R_L = 2\text{k}$	$\pm 15\text{V}$	●	15		MHz
			$\pm 5\text{V}$	●	12		MHz
	Channel Separation	$V_{OUT} = \pm 10\text{V}$, $R_L = 500\Omega$	$\pm 15\text{V}$	●	98		dB
I_S	Supply Current	Each Amplifier Each Amplifier	$\pm 15\text{V}$	●		2.9	mA
			$\pm 5\text{V}$	●		2.8	mA

ELECTRICAL CHARACTERISTICS $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, $V_{CM} = 0\text{V}$ unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		$\pm 15\text{V}$	●		1.3	mV
			$\pm 5\text{V}$	●		1.3	mV
			$\pm 2.5\text{V}$	●		1.5	mV
	Input V_{OS} Drift	(Note 4)	$\pm 2.5\text{V}$ to $\pm 15\text{V}$	●	5	8	$\mu\text{V}/^{\circ}\text{C}$
I_{OS}	Input Offset Current		$\pm 2.5\text{V}$ to $\pm 15\text{V}$	●		300	nA
I_B	Input Bias Current		$\pm 2.5\text{V}$ to $\pm 15\text{V}$	●		900	nA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 12\text{V}$ $V_{CM} = \pm 2.5\text{V}$ $V_{CM} = \pm 0.5\text{V}$	$\pm 15\text{V}$	●	80		dB
			$\pm 5\text{V}$	●	76		dB
			$\pm 2.5\text{V}$	●	66		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.5\text{V}$ to $\pm 15\text{V}$		●	90		dB

ELECTRICAL CHARACTERISTICS $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, $V_{\text{CM}} = 0\text{V}$ unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	V _{SUPPLY}	MIN	TYP	MAX	UNITS
A _{VOL}	Large-Signal Voltage Gain	V _{OUT} = ±12V, R _L = 1k	±15V	● 10.0			V/mV
		V _{OUT} = ±10V, R _L = 500Ω	±15V	● 2.5			V/mV
		V _{OUT} = ±2.5V, R _L = 1k	±5V	● 10.0			V/mV
		V _{OUT} = ±2.5V, R _L = 500Ω	±5V	● 2.5			V/mV
		V _{OUT} = ±2.5V, R _L = 150Ω	±5V	● 0.6			V/mV
		V _{OUT} = ±1V, R _L = 500Ω	±2.5V	● 2.5			V/mV
V _{OUT}	Output Swing	R _L = 1k, V _{IN} = ±40mV	±15V	● 13.0			±V
		R _L = 500Ω, V _{IN} = ±40mV	±15V	● 12.0			±V
		R _L = 500Ω, V _{IN} = ±40mV	±5V	● 3.4			±V
		R _L = 150Ω, V _{IN} = ±40mV	±5V	● 2.6			±V
		R _L = 500Ω, V _{IN} = ±40mV	±2.5V	● 1.2			±V
I _{OUT}	Output Current	V _{OUT} = ±12V	±15V	● 24.0			mA
		V _{OUT} = ±2.6V	±5V	● 17.3			mA
I _{SC}	Short-Circuit Current	V _{OUT} = 0V, V _{IN} = ±3V	±15V	● 24			mA
SR	Slew Rate	A _v = -2, (Note 2)	±15V	● 180			V/μs
			±5V	● 100			V/μs
GBW	Gain-Bandwidth	f = 200kHz, R _L = 2k	±15V	● 14			MHz
			±5V	● 11			MHz
	Channel Separation	V _{OUT} = ±10V, R _L = 500Ω	±15V	● 98			dB
I _S	Supply Current	Each Amplifier	±15V	●		3.0	mA
		Each Amplifier	±5V	●		2.9	mA

The ● denotes specifications that apply over the full operating temperature range.

Note 1: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

Note 2: Slew rate is measured between ±10V on the output with ±6V input for ±15V supplies and ±1V on the output with ±1.75V input for ±5V supplies.

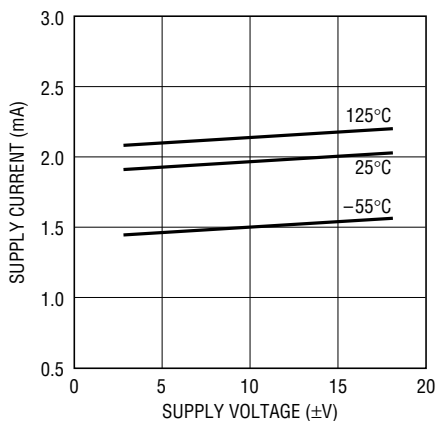
Note 3: Full power bandwidth is calculated from the slew rate measurement: $\text{FPBW} = (\text{SR})/2\pi V_p$.

Note 4: This parameter is not 100% tested.

Note 5: The LT1358/LT1359 are not tested and are not quality-assurance sampled at -40°C and at 85°C. These specifications are guaranteed by design, correlation, and/or inference from 0°C, 25°C, and/or 70°C tests.

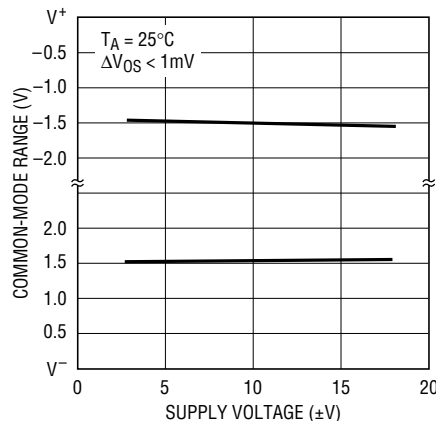
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Supply Voltage and Temperature



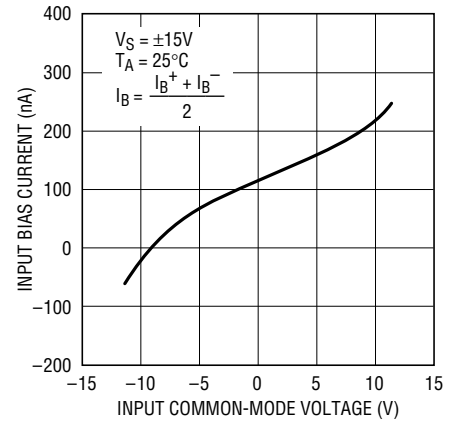
1358/1359 G01

Input Common-Mode Range vs Supply Voltage



1358/1359 G02

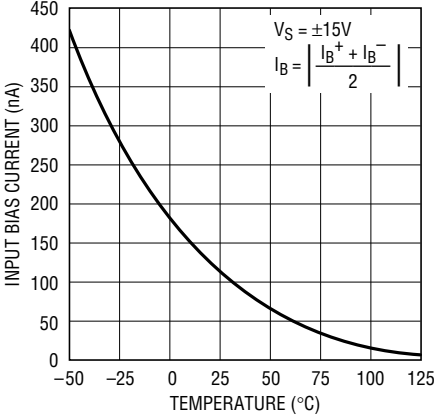
Input Bias Current vs Input Common-Mode Voltage



1358/1359 G03

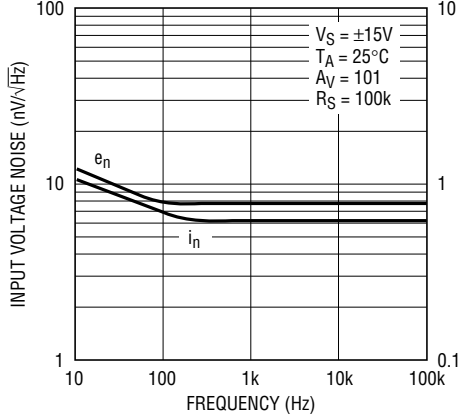
TYPICAL PERFORMANCE CHARACTERISTICS

Input Bias Current vs Temperature



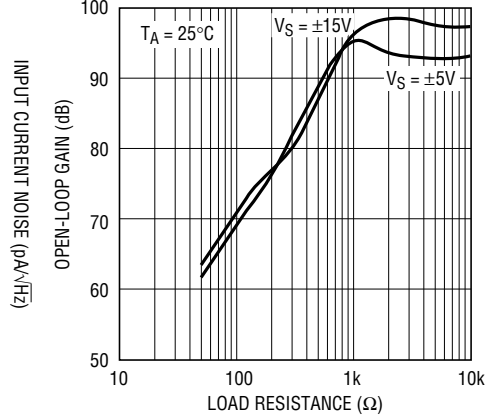
1358/1359 G04

Input Noise Spectral Density



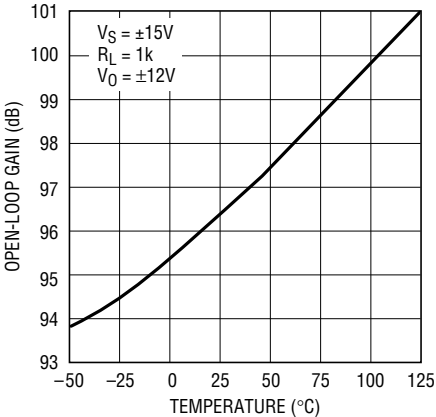
1358/1359 G05

Open-Loop Gain vs Resistive Load



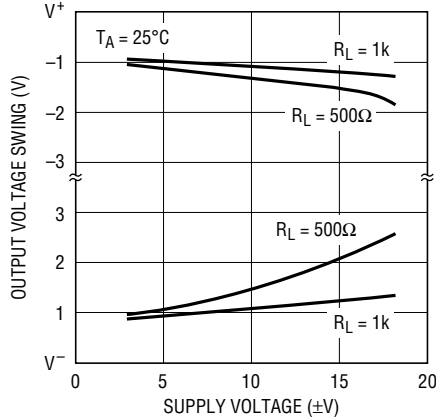
1358/1359 G06

Open-Loop Gain vs Temperature



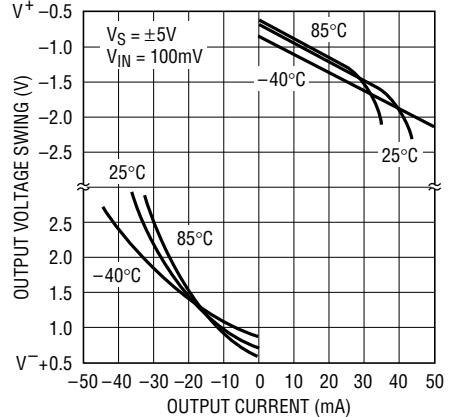
1358/1359 G07

Output Voltage Swing vs Supply Voltage



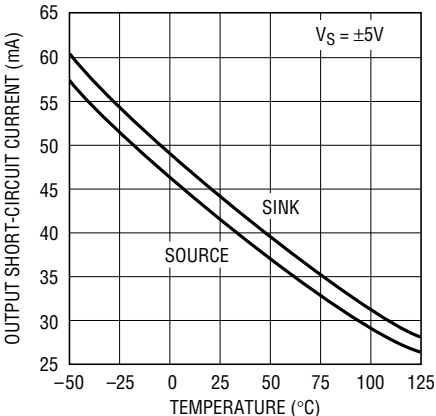
1358/1359 G08

Output Voltage Swing vs Load Current



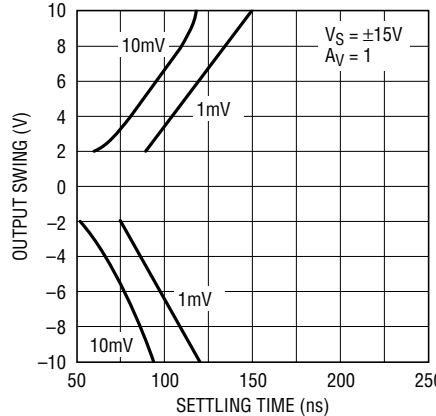
1358/1359 G09

Output Short-Circuit Current vs Temperature



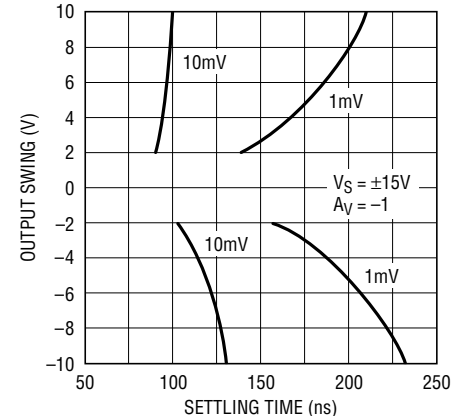
1358/1359 G10

Settling Time vs Output Step (Noninverting)



1358/1359 G11

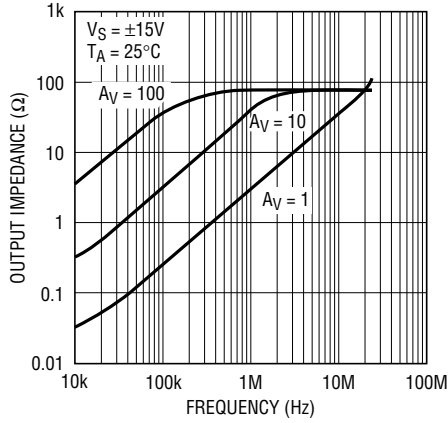
Settling Time vs Output Step (Inverting)



1358/1359 G12

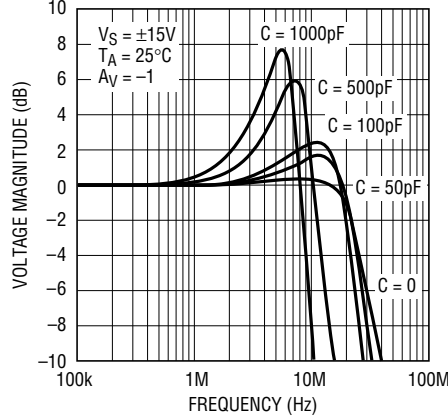
TYPICAL PERFORMANCE CHARACTERISTICS

Output Impedance vs Frequency



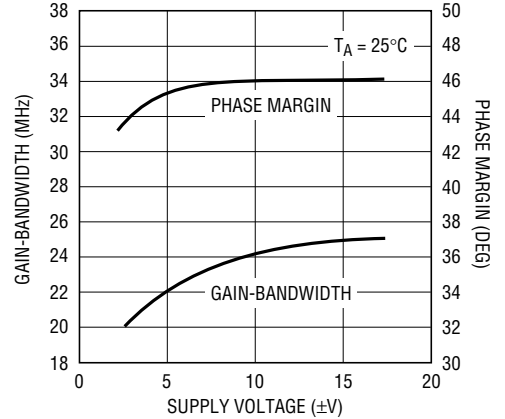
1358/1359 G13

Frequency Response vs Capacitive Load



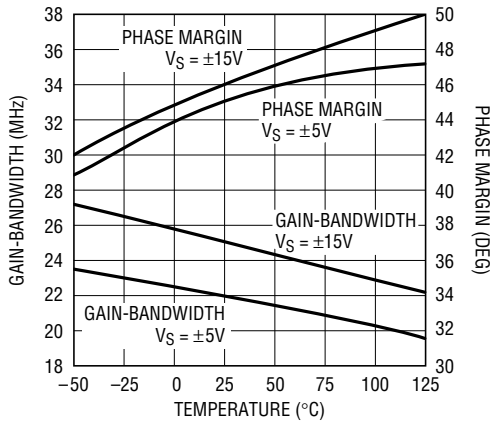
1358/1359 G19

Gain-Bandwidth and Phase Margin vs Supply Voltage



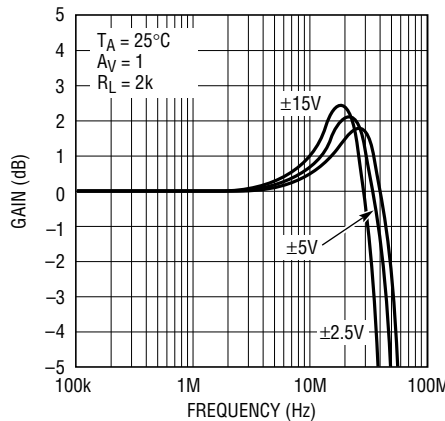
1358/1359 G15

Gain-Bandwidth and Phase Margin vs Temperature



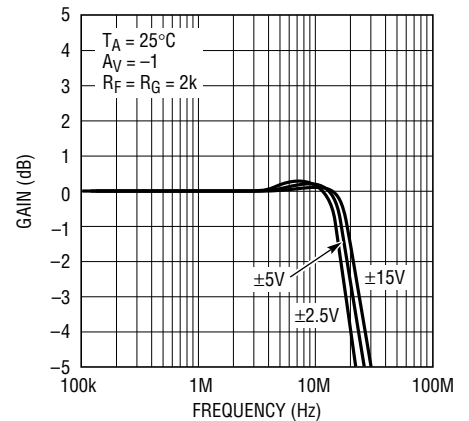
1358/1359 G16

Frequency Response vs Supply Voltage (Av = 1)



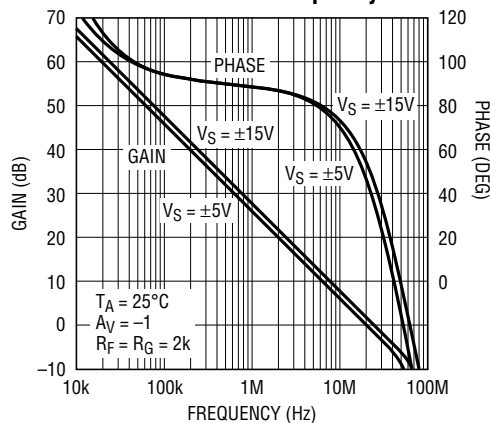
1358/1359 G17

Frequency Response vs Supply Voltage (Av = -1)



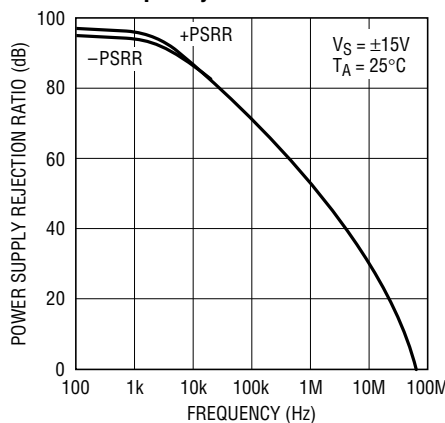
1358/1359 G18

Gain and Phase vs Frequency



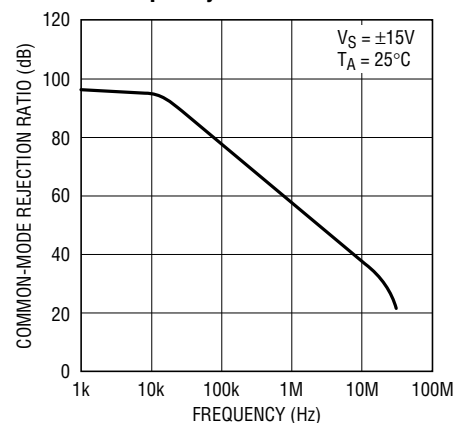
1358/1359 G14

Power Supply Rejection Ratio vs Frequency



1358/1359 G20

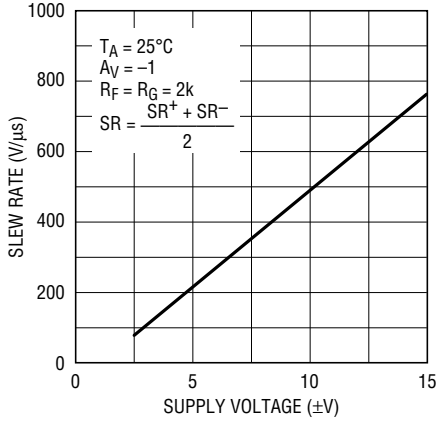
Common-Mode Rejection Ratio vs Frequency



1358/1359 G21

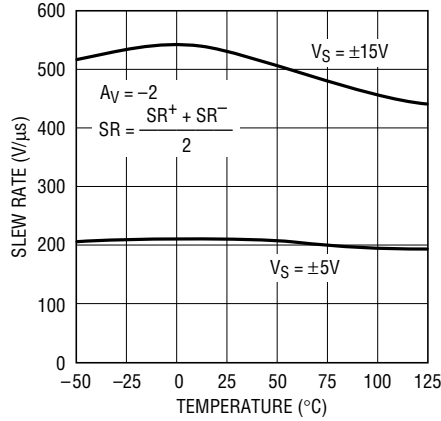
TYPICAL PERFORMANCE CHARACTERISTICS

Slew Rate vs Supply Voltage



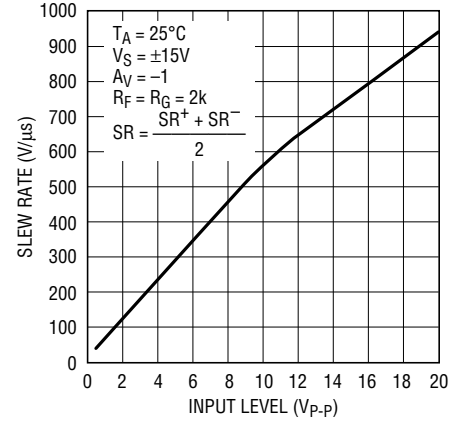
1358/1359 G22

Slew Rate vs Temperature



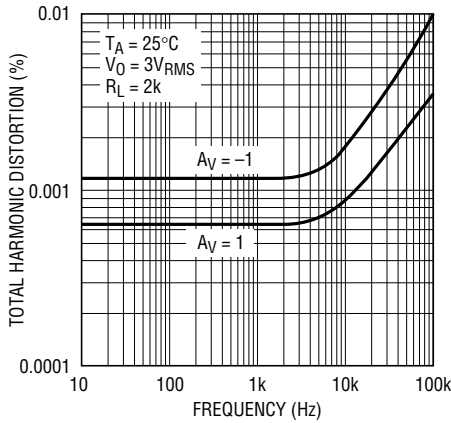
1358/1359 G23

Slew Rate vs Input Level



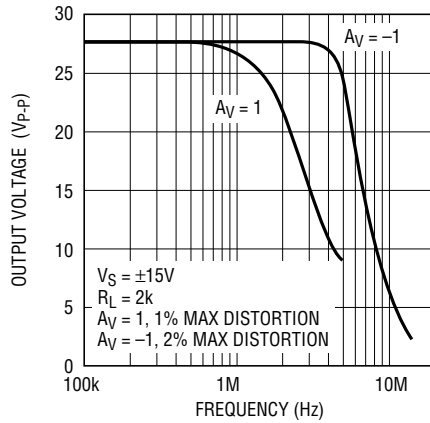
1358/1359 G24

Total Harmonic Distortion vs Frequency



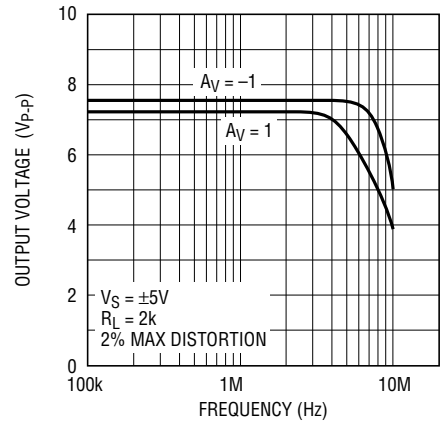
1358/1359 G25

Undistorted Output Swing vs Frequency (±15V)



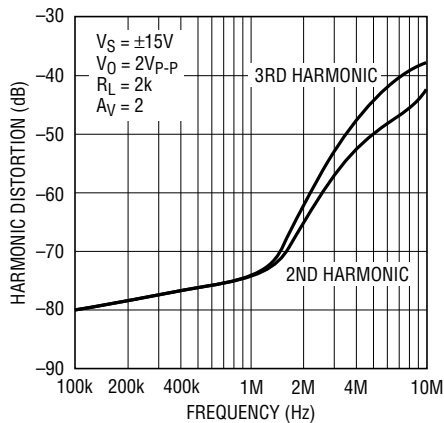
1358/1359 G26

Undistorted Output Swing vs Frequency (±5V)



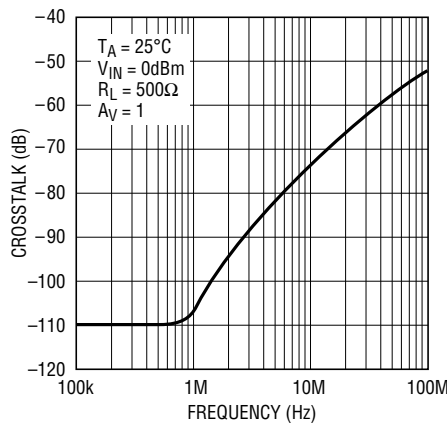
1358/1359 G27

2nd and 3rd Harmonic Distortion vs Frequency



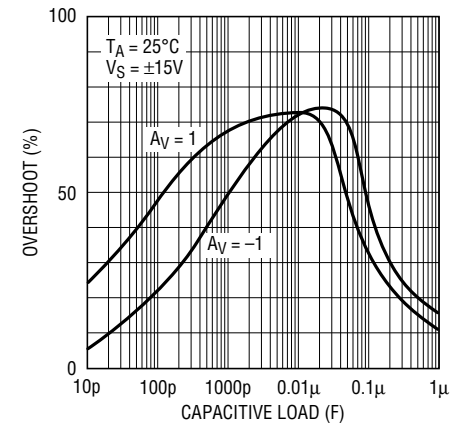
1358/1359 G28

Crosstalk vs Frequency



1358/1359 G29

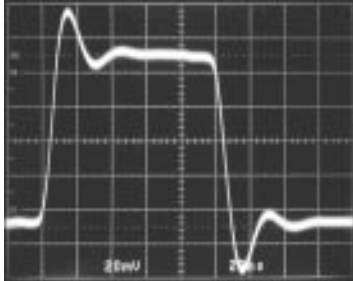
Capacitive Load Handling



1358/1359 G30

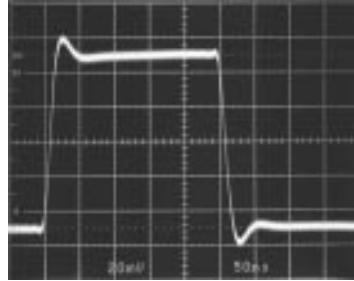
TYPICAL PERFORMANCE CHARACTERISTICS

Small-Signal Transient
($A_V = 1$)



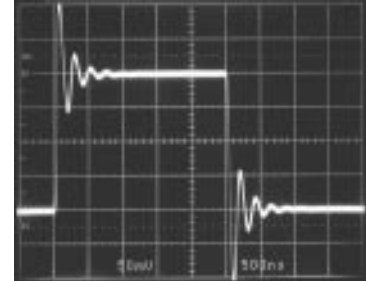
1358/1359 G31

Small-Signal Transient
($A_V = -1$)



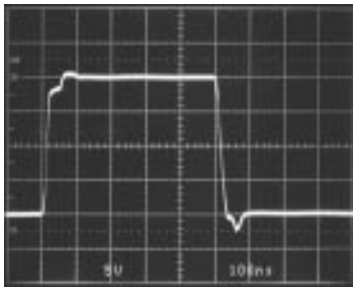
1358/1359 G32

Small-Signal Transient
($A_V = -1, C_L = 1000\text{pF}$)



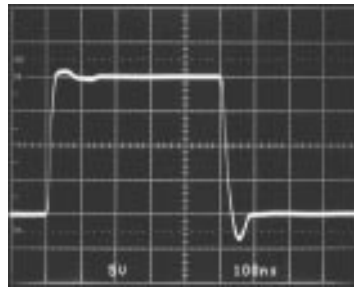
1358/1359 G33

Large-Signal Transient
($A_V = 1$)



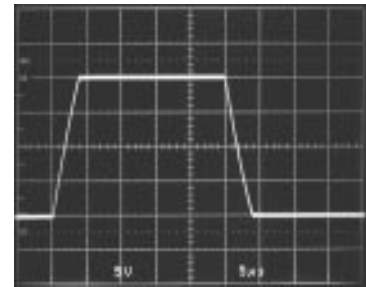
1358/1359 G34

Large-Signal Transient
($A_V = -1$)



1358/1359 G35

Large-Signal Transient
($A_V = 1, C_L = 10,000\text{pF}$)



1358/1359 G36

APPLICATIONS INFORMATION

Layout and Passive Components

The LT1358/LT1359 amplifiers are easy to use and tolerant of less than ideal layouts. For maximum performance (for example, fast 0.01% settling) use a ground plane, short lead lengths, and RF-quality bypass capacitors (0.01 μF to 0.1 μF). For high drive current applications use low ESR bypass capacitors (1 μF to 10 μF tantalum).

The parallel combination of the feedback resistor and gain setting resistor on the inverting input combine with the input capacitance to form a pole which can cause peaking or oscillations. If feedback resistors greater than 5k are used, a parallel capacitor of value

$$C_F > R_G \times C_{IN} / R_F$$

should be used to cancel the input pole and optimize dynamic performance. For unity-gain applications where a large feedback resistor is used, C_F should be greater than or equal to C_{IN} .

Capacitive Loading

The LT1358/LT1359 are stable with any capacitive load. As the capacitive load increases, both the bandwidth and phase margin decrease so there will be peaking in the frequency domain and in the transient response. Coaxial cable can be driven directly, but for best pulse fidelity a resistor of value equal to the characteristic impedance of the cable (i.e., 75 Ω) should be placed in series with the output. The other end of the cable should be terminated with the same value resistor to ground.

APPLICATIONS INFORMATION

Input Considerations

Each of the LT1358/LT1359 amplifier inputs is the base of an NPN and PNP transistor whose base currents are of opposite polarity and provide first-order bias current cancellation. Because of variation in the matching of NPN and PNP beta, the polarity of the input current can be positive or negative. The offset current does not depend on beta matching and is well controlled. The use of balanced source resistance at each input is recommended for applications where DC accuracy must be maximized. The inputs can withstand differential input voltages of up to 10V without damage and need no clamping or source resistance for protection.

Circuit Operation

The LT1358/LT1359 circuit topology is a true voltage feedback amplifier that has the slewing behavior of a current feedback amplifier. The operation of the circuit can be understood by referring to the simplified schematic. The inputs are buffered by complementary NPN and PNP emitter followers which drive a 500Ω resistor. The input voltage appears across the resistor generating currents which are mirrored into the high impedance node. Complementary followers form an output stage which buffers the gain node from the load. The bandwidth is set by the input resistor and the capacitance on the high impedance node. The slew rate is determined by the current available to charge the gain node capacitance. This current is the differential input voltage divided by R1, so the slew rate is proportional to the input. Highest slew rates are therefore seen in the lowest gain configurations. For example, a 10V output step in a gain of 10 has only a 1V input step, whereas the same output step in unity gain has a 10 times greater input step. The curve of Slew Rate vs Input Level illustrates this relationship. The LT1358/LT1359 are tested for slew rate in a gain of -2 so higher slew rates can be expected in gains of 1 and -1, and lower slew rates in higher gain configurations.

The RC network across the output stage is bootstrapped when the amplifier is driving a light or moderate load and has no effect under normal operation. When driving a capacitive load (or a low value resistive load) the network is incompletely bootstrapped and adds to the compensation at the high impedance node. The added capacitance slows down the amplifier which improves the phase margin by moving the unity-gain frequency away from the pole formed by the output impedance and the capacitive load. The zero created by the RC combination adds phase to ensure that even for very large load capacitances, the total phase lag can never exceed 180 degrees (zero phase margin) and the amplifier remains stable.

Power Dissipation

The LT1358/LT1359 combine high speed and large output drive in small packages. Because of the wide supply voltage range, it is possible to exceed the maximum junction temperature under certain conditions. Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) as follows:

$$\text{LT1358CN8: } T_J = T_A + (P_D \times 130^\circ\text{C/W})$$

$$\text{LT1358CS8: } T_J = T_A + (P_D \times 190^\circ\text{C/W})$$

$$\text{LT1359CN: } T_J = T_A + (P_D \times 110^\circ\text{C/W})$$

$$\text{LT1359CS: } T_J = T_A + (P_D \times 150^\circ\text{C/W})$$

Worst case power dissipation occurs at the maximum supply current and when the output voltage is at 1/2 of either supply voltage (or the maximum swing if less than 1/2 supply voltage). For each amplifier $P_{D\text{MAX}}$ is:

$$P_{D\text{MAX}} = (V^+ - V^-)(I_{S\text{MAX}}) + (V^+/2)^2/R_L$$

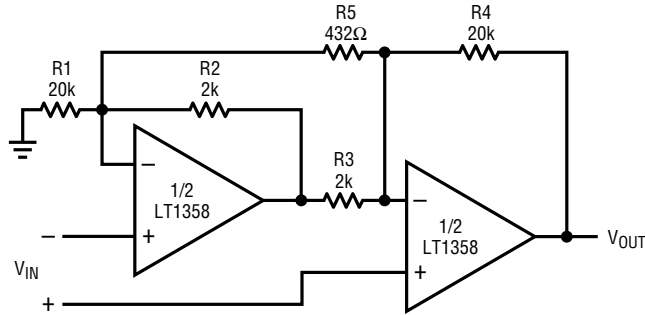
Example: LT1358 in S8 at 70°C, $V_S = \pm 15\text{V}$, $R_L = 500\Omega$

$$P_{D\text{MAX}} = (30\text{V})(2.9\text{mA}) + (7.5\text{V})^2/500\Omega = 200\text{mW}$$

$$T_{J\text{MAX}} = 70^\circ\text{C} + (2 \times 200\text{mW})(190^\circ\text{C/W}) = 146^\circ\text{C}$$

TYPICAL APPLICATIONS

Instrumentation Amplifier

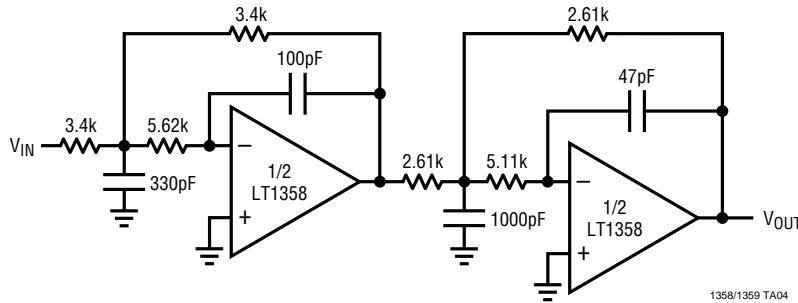


$$A_v = \frac{R_4}{R_3} \left[1 + \frac{1}{2} \left(\frac{R_2}{R_1} + \frac{R_3}{R_4} \right) + \frac{R_2 + R_3}{R_5} \right] = 104$$

TRIM R5 FOR GAIN
 TRIM R1 FOR COMMON-MODE REJECTION
 BW = 250kHz

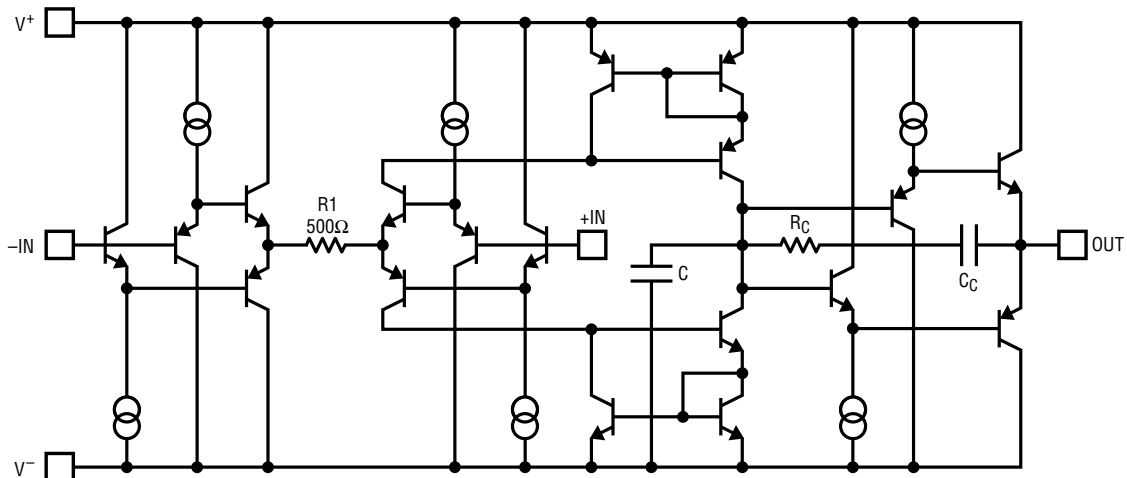
1358/1359 TA03

200kHz, 4th Order Butterworth Filter



1358/1359 TA04

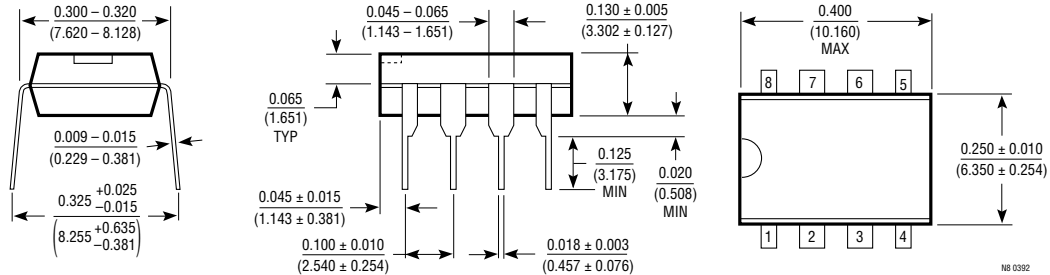
SIMPLIFIED SCHEMATIC



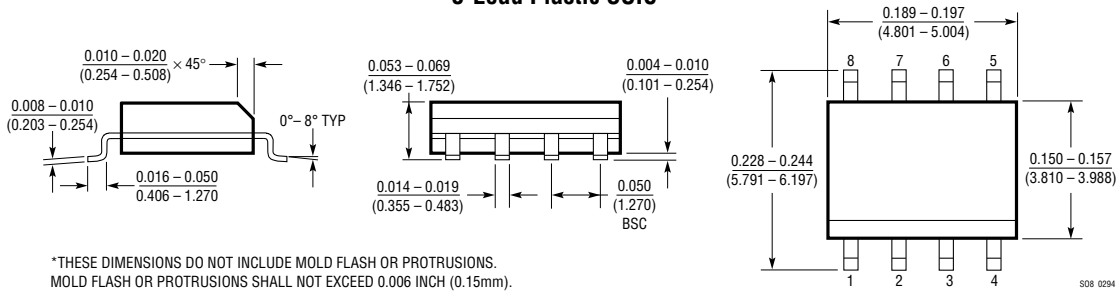
1358/1359 SS01

PACKAGE DESCRIPTION Dimension in inches (millimeters) unless otherwise noted.

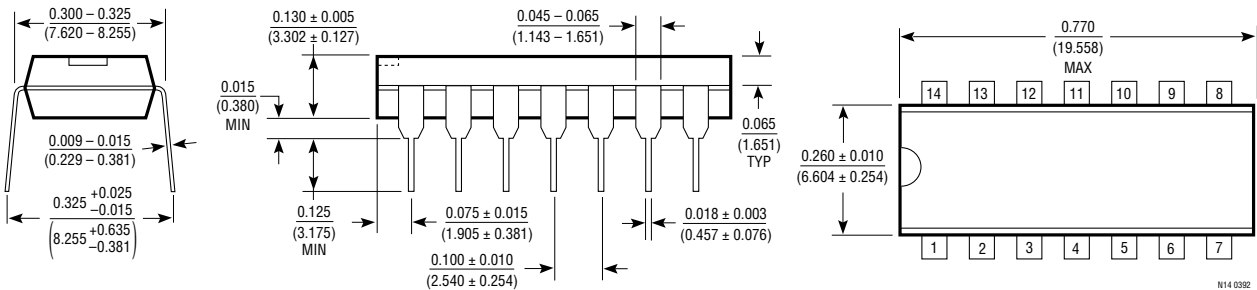
**N8 Package
8-Lead Plastic DIP**



**S8 Package
8-Lead Plastic SOIC**



**N Package
14-Lead Plastic DIP**



**S Package
16-Lead Plastic SOIC**

