

ABSOLUTE MAXIMUM RATINGS

Supply Voltage $\pm 22V$
 Input Voltage Equal to Supply Voltage
 Output Short Circuit Duration Indefinite
 Differential Input Current (Note 5) $\pm 25mA$
 Lead Temperature (Soldering, 10 sec.) $300^{\circ}C$

Operating Temperature Range
 LT1126AM/LT1126M
 LT1127AM/LT1127M $-55^{\circ}C$ to $125^{\circ}C$
 LT1126AC/LT1126C
 LT1127AC/LT1127C $-40^{\circ}C$ to $85^{\circ}C$
 Storage Temperature Range
 All Grades $-65^{\circ}C$ to $150^{\circ}C$

PACKAGE/ORDER INFORMATION

<p>TOP VIEW</p> <p>S8 PACKAGE 8-LEAD PLASTIC SOIC</p> <p>NOTE: THIS PIN CONFIGURATION DIFFERS FROM THE 8-PIN DIP CONFIGURATION. INSTEAD, IT FOLLOWS THE INDUSTRY STANDARD LT1013DS8 SO PACKAGE PIN LOCATIONS</p> <p>LT1126 • POI01</p>	<p>ORDER PART NUMBER</p> <p>LT1126CS8</p> <p>S8 PART MARKING</p> <p>1126</p>	<p>TOP VIEW</p> <p>J8 PACKAGE 8-LEAD CERAMIC DIP</p> <p>N8 PACKAGE 8-LEAD PLASTIC DIP</p> <p>LT1126 • POI02</p>	<p>ORDER PART NUMBER</p> <p>LT1126AMJ8 LT1126MJ8 LT1126CJ8 LT1126ACN8 LT1126CN8</p>
<p>TOP VIEW</p> <p>S PACKAGE 16-LEAD PLASTIC SOL</p> <p>LT1126 • POI03</p>	<p>LT1127CS</p>	<p>TOP VIEW</p> <p>J PACKAGE 14-LEAD CERAMIC DIP</p> <p>N PACKAGE 14-LEAD PLASTIC DIP</p> <p>LT1126 • POI04</p>	<p>LT1127AMJ LT1127MJ LT1127CJ LT1127ACN LT1127CN</p>

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25^{\circ}C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 1)	LT1126AM/AC LT1127AM/AC			LT1126M/C LT1127M/C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	LT1126 LT1127		20 25	70 90		25 30	100 140	μV μV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability			0.3			0.3		$\mu V/Mo$
I_{OS}	Input Offset Current	LT1126 LT1127		5 6	15 20		6 7	20 30	nA nA
I_B	Input Bias Current			± 7	± 20		± 8	± 30	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Notes 7 and 8)		70	200		70		nVp-p

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 1)	LT1126AM/AC LT1127AM/AC			LT1126M/C LT1127M/C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
	Input Noise Voltage Density	$f_0 = 10\text{Hz}$ (Note 3) $f_0 = 1000\text{Hz}$ (Note 2)	3.0	5.5		3.0	5.5		$nV/\sqrt{\text{Hz}}$
			2.7	4.2		2.7	4.2		$nV/\sqrt{\text{Hz}}$
i_n	Input Noise Current Density	$f_0 = 10\text{Hz}$ $f_0 = 1000\text{Hz}$	1.3			1.3			$pA/\sqrt{\text{Hz}}$ $pA/\sqrt{\text{Hz}}$
V_{CM}	Input Voltage Range		± 12.0	± 12.8		± 12.0	± 12.8		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 12V$	112	126		106	124		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4V$ to $\pm 18V$	116	126		110	124		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 10k\Omega$, $V_0 = \pm 10V$ $R_L \geq 2k\Omega$, $V_0 = \pm 10V$	5.0	17.0		3.0	15.0		$V/\mu V$
			2.0	4.0		1.5	3.0		$V/\mu V$
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$	± 13.0	± 13.8		± 12.5	± 13.8		V
SR	Slew Rate	$R_L \geq 2k\Omega$ (Notes 2 and 6)	8.0	11		8.0	11		$V/\mu s$
GBW	Gain-Bandwidth Product	$f_0 = 10\text{kHz}$ (Note 2)	45	65		45	65		MHz
Z_0	Open Loop Output Resistance	$V_0 = 0$, $I_0 = 0$		75			75		Ω
I_S	Supply Current Per Amplifier		2.6	3.1		2.6	3.1		mA
	Channel Separation	$f \leq 10\text{Hz}$ (Note 8) $V_0 = \pm 10V$, $R_L = 2k\Omega$	134	150		130	150		dB

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq 125^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 1)	LT1126AM LT1127AM			LT1126M LT1127M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	LT1126	●	50	170		60	250	μV
		LT1127	●	55	190		70	290	μV
$\frac{\Delta V_{OS}}{\Delta \text{Temp}}$	Average Input Offset Voltage Drift	(Note 4)	●	0.3	1.0		0.4	1.5	$\mu V/^\circ C$
I_{OS}	Input Offset Current	LT1126	●	18	45		20	60	nA
		LT1127	●	18	55		20	70	nA
I_B	Input Bias Current		●	± 18	± 55		± 20	± 70	nA
V_{CM}	Input Voltage Range		●	± 11.3	± 12		± 11.3	± 12	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 11.3V$	●	106	122		100	120	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4V$ to $\pm 18V$	●	110	122		104	120	dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 10k\Omega$, $V_0 = \pm 10V$ $R_L \geq 2k\Omega$, $V_0 = \pm 10V$	●	3.0	10.0		2.0	10.0	$V/\mu V$
			●	1.0	3.0		0.7	2.0	$V/\mu V$
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$	●	± 12.5	± 13.6		± 12.0	± 13.6	V
SR	Slew Rate	$R_L \geq 2k\Omega$ (Notes 2 and 6)	●	7.2	10		7.0	10	$V/\mu s$
I_S	Supply Current Per Amplifier		●	2.8	3.5		2.8	3.5	mA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Typical parameters are defined as the 60% yield of parameter distributions of individual amplifiers; i.e., out of 100 LT1127s (or 100 LT1126s) typically 240 op amps (or 120) will be better than the indicated specification.

Note 2: This parameter is 100% tested for each individual amplifier.

Note 3: This parameter is sample tested only.

Note 4: This parameter is not 100% tested.

Note 5: The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds $\pm 1.4V$, the input current should be limited to 25mA.

Note 6: Slew rate is measured in $A_V = -10$; input signal is $\pm 1V$, output measured at $\pm 5V$.

Note 7: 0.1Hz to 10Hz noise can be inferred from the 10Hz noise voltage density test. See the test circuit and frequency response curve for 0.1Hz to 10Hz tester in the Applications Information section of the LT1007 or LT1028 datasheets.

Note 8: This parameter is guaranteed but not tested.

Note 9: The LT1126 and LT1127 are not tested and are not quality assurance sampled at $-40^\circ C$ and at $85^\circ C$. These specifications are guaranteed by design, correlation and/or inference from $-55^\circ C$, $0^\circ C$, $25^\circ C$, $70^\circ C$ and/or $125^\circ C$ tests.

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, 0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 1)	LT1126AC LT1127AC			LT1126C LT1127C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	LT1126 LT1127	● ●	35 40	120 140	45 50	170 210	μV μV	
$\Delta V_{OS}/\Delta T$	Average Input Offset Voltage Drift	(Note 4)	●	0.3	1.0	0.4	1.5	$\mu V/^\circ C$	
I_{OS}	Input Offset Current	LT1126 LT1127	● ●	6 7	25 35	7 8	35 45	nA nA	
I_B	Input Bias Current		●	± 8	± 35	± 9	± 45	nA	
V_{CM}	Input Voltage Range		●	± 11.5	± 12.4	± 11.5	± 12.4	V	
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 11.5V$	●	109	125	102	122	dB	
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4V$ to $\pm 18V$	●	112	125	107	122	dB	
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 10k\Omega, V_O = \pm 10V$ $R_L \geq 2k\Omega, V_O = \pm 10V$	● ●	4.0 1.5	15.0 3.5	2.5 1.0	14.0 2.5	$V/\mu V$ $V/\mu V$	
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$	●	± 12.5	± 13.7	± 12.0	± 13.7	V	
SR	Slew Rate	$R_L \geq 2k\Omega$ (Notes 2 and 6)	●	7.5	10.5	7.3	10.5	$V/\mu s$	
I_S	Supply Current Per Amplifier		●	2.7	3.3	2.7	3.3	mA	

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, -40^\circ C \leq T_A \leq 85^\circ C$, unless otherwise noted. (Note 9)

SYMBOL	PARAMETER	CONDITIONS (Note 1)	LT1126AC LT1127AC			LT1126C LT1127C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	LT1126 LT1127	● ●	40 45	140 160	50 55	200 240	μV μV	
$\Delta V_{OS}/\Delta T$	Average Input Offset Voltage Drift		●	0.3	1.0	0.4	1.5	$\mu V/^\circ C$	
I_{OS}	Input Offset Current	LT1126 LT1127	● ●	15 15	40 50	17 17	55 65	nA nA	
I_B	Input Bias Current		●	± 15	± 50	± 17	± 65	nA	
V_{CM}	Input Voltage Range		●	± 11.4	± 12.2	± 11.4	± 12.2	V	
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 11.4V$	●	107	124	101	121	dB	
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4V$ to $\pm 18V$	●	111	124	106	121	dB	
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 10k\Omega, V_O = \pm 10V$ $R_L \geq 2k\Omega, V_O = \pm 10V$	● ●	3.5 1.2	12.0 3.2	2.2 0.8	12.0 2.3	$V/\mu V$ $V/\mu V$	
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$	●	± 12.5	± 13.6	± 12.0	± 13.6	V	
SR	Slew Rate	$R_L \geq 2k\Omega$ (Note 6)	●	7.3	10.2	7.1	10.2	$V/\mu s$	
I_S	Supply Current Per Amplifier		●	2.8	3.4	2.8	3.4	mA	

TYPICAL PERFORMANCE CHARACTERISTICS

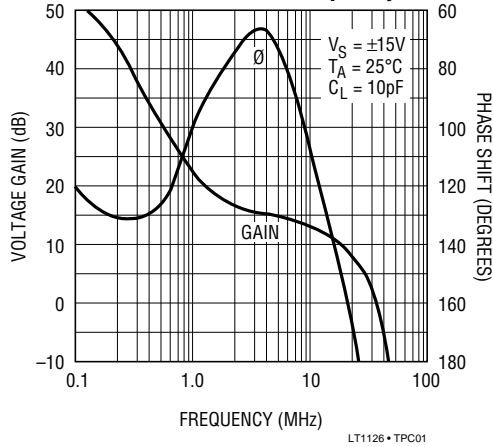
The typical behavior of many LT1126/LT1127 parameters is identical to the LT1124/LT1125. Please refer to the LT1124/LT1125 data sheet for the following performance characteristics:

- 0.1Hz to 10Hz Voltage Noise
- 0.01Hz to 1Hz Voltage Noise
- Current Noise vs Frequency
- Input Bias or Offset Current vs Temperature
- Output Short Circuit Current vs Time

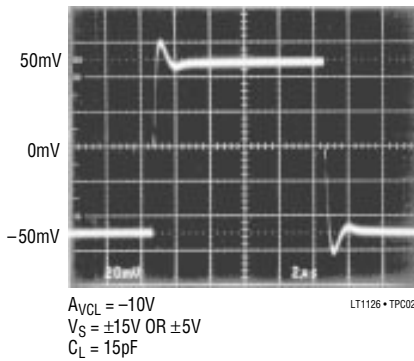
- Input Bias Current Over the Common Mode Range
- Voltage Gain vs Temperature
- Input Offset Voltage Drift Distribution
- Offset Voltage Drift with Temperature of Representative Units
- Output Voltage Swing vs Load Current
- Common Mode Limit vs Temperature
- Channel Separation vs Frequency
- Warm-Up Drift
- Power Supply Rejection Ratio vs Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

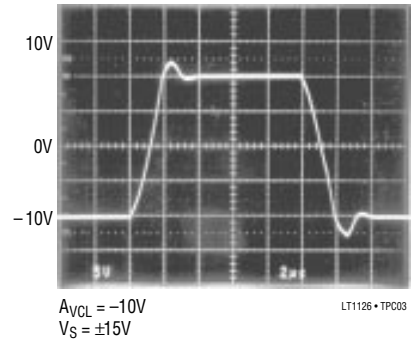
Gain, Phase Shift vs Frequency



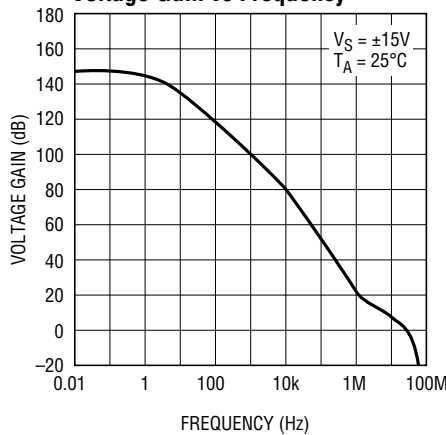
Small-Signal Transient Response



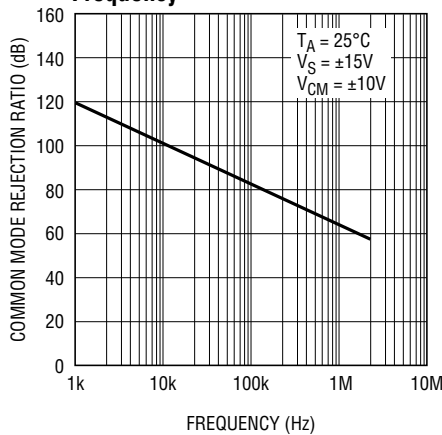
Large-Signal Transient Response



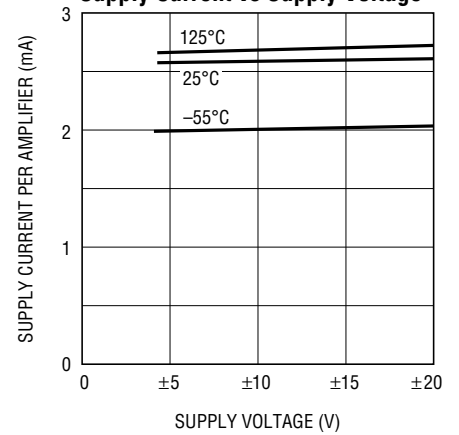
Voltage Gain vs Frequency



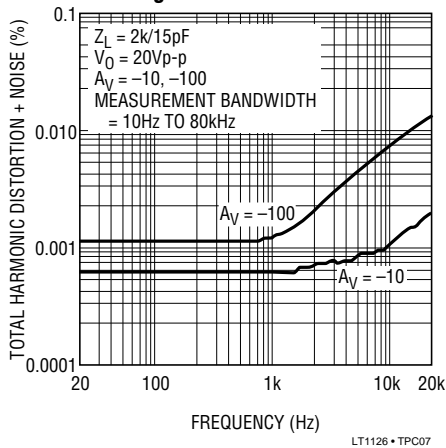
Common Mode Rejection Ratio vs Frequency



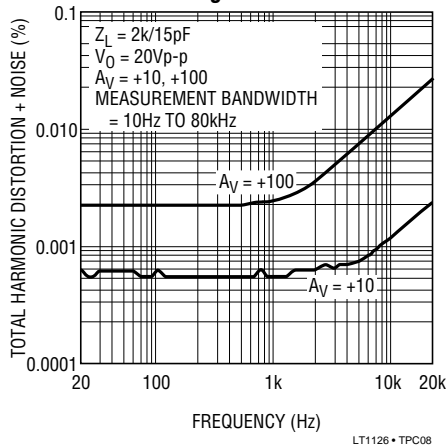
Supply Current vs Supply Voltage



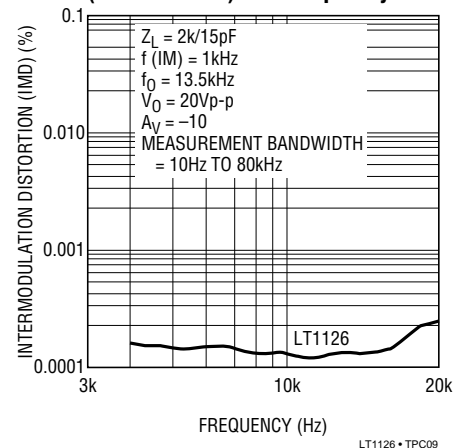
Total Harmonic Distortion and Noise vs Frequency for Inverting Gain



Total Harmonic Distortion and Noise vs Frequency for Non-Inverting Gain



Intermodulation Distortion (CCIF Method)* vs Frequency



* See LT1115 data sheet for definition of CCIF testing

APPLICATIONS INFORMATION

Matching Specifications

In many applications the performance of a system depends on the matching between two op amps, rather than the individual characteristics of the two devices. The three op amp instrumentation amplifier configuration shown in this data sheet is an example. Matching characteristics are not 100% tested on the LT1126/LT1127.

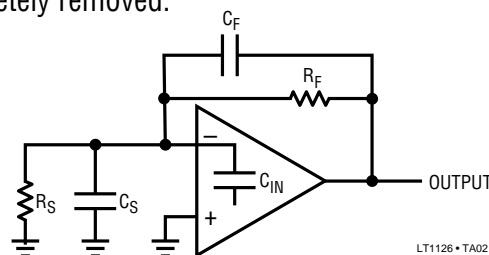
Some specifications are guaranteed by definition. For example, 70 μ V maximum offset voltage implies that mismatch cannot be more than 140 μ V. 112dB (= 2.5 μ V/V) CMRR means that worst case CMRR match is 106dB (5 μ V/V). However, the following table can be used to estimate the expected matching performance between the two sides of the LT1126, and between amplifiers A and D, and between amplifiers B and C of the LT1127.

Expected Match

PARAMETER		LT1126AM/AC LT1127AM/AC		LT1126M/C LT1127M/C		UNITS
		50% YIELD	98% YIELD	50% YIELD	98% YIELD	
V _{OS} Match, Δ V _{OS}	LT1126	20	110	30	130	μ V
	LT1127	30	150	50	180	μ V
Temperature Coefficient Match		0.35	1.0	0.5	1.5	μ V/ $^{\circ}$ C
Average Non-Inverting I _B		6	18	7	25	nA
Match of Non-Inverting I _B		7	22	8	30	nA
CMRR Match		126	115	123	112	dB
PSRR Match		127	118	127	114	dB

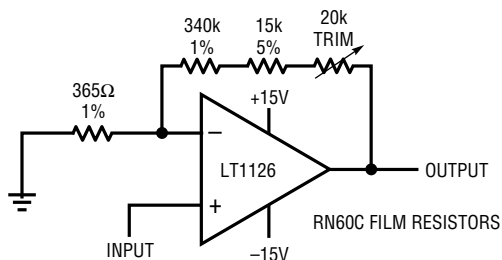
High Speed Operation

When the feedback around the op amp is resistive (R_F), a pole will be created with R_F, the source resistance and capacitance (R_S, C_S), and the amplifier input capacitance (C_{IN} \approx 2pF). In low closed loop gain configurations and with R_S and R_F in the kilohm range, this pole can create excess phase shift and even oscillation. A small capacitor (C_F) in parallel with R_F eliminates this problem. With R_S (C_S + C_{IN}) = R_F C_F, the effect of the feedback pole is completely removed.



TYPICAL APPLICATIONS

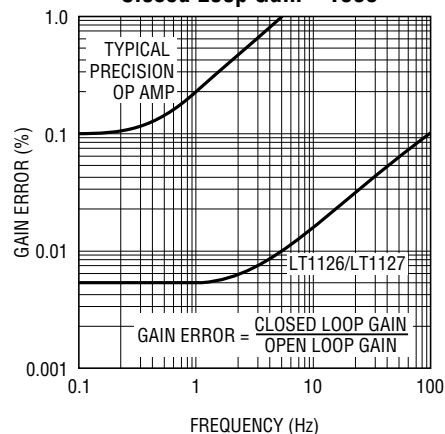
Gain 1000 Amplifier with 0.01% Accuracy, DC to 5Hz



THE HIGH GAIN AND WIDE BANDWIDTH OF THE LT1126/LT1127 IS USEFUL IN LOW FREQUENCY HIGH CLOSED LOOP GAIN AMPLIFIER APPLICATIONS. A TYPICAL PRECISION OP AMP MAY HAVE AN OPEN LOOP GAIN OF ONE MILLION WITH 500kHz BANDWIDTH. AS THE GAIN ERROR PLOT SHOWS, THIS DEVICE IS CAPABLE OF 0.1% AMPLIFYING ACCURACY UP TO 0.3Hz ONLY. EVEN INSTRUMENTATION RANGE SIGNALS CAN VARY AT A FASTER RATE. THE LT1126/LT1127 "GAIN PRECISION — BANDWIDTH PRODUCT" IS 330 TIMES HIGHER, AS SHOWN.

LT1126 • TA03

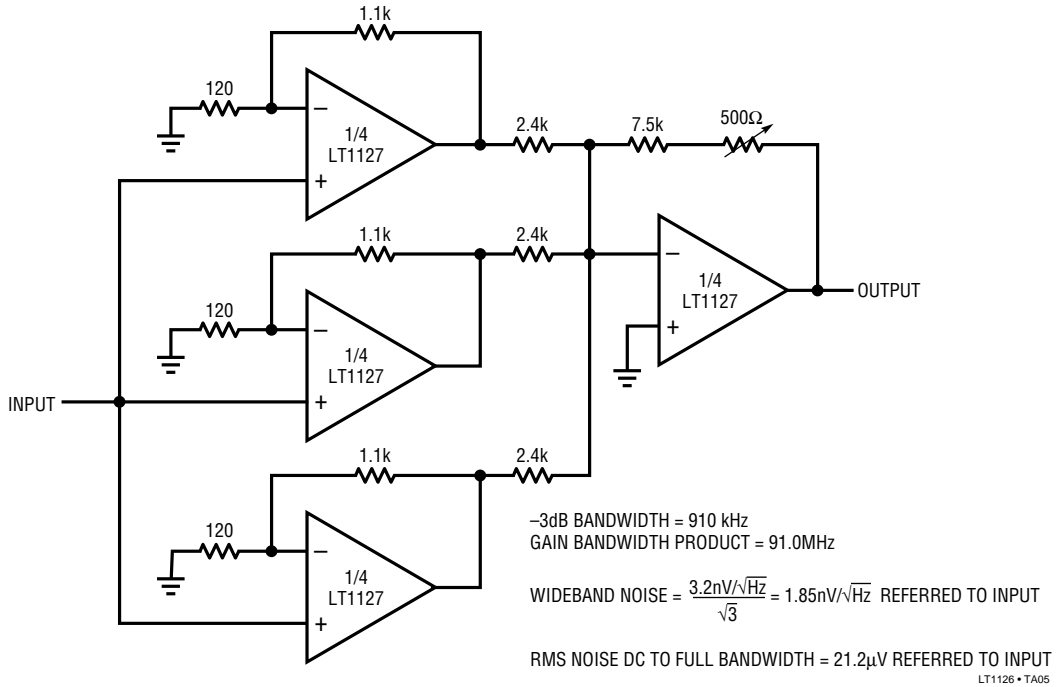
Gain Error vs Frequency Closed Loop Gain = 1000



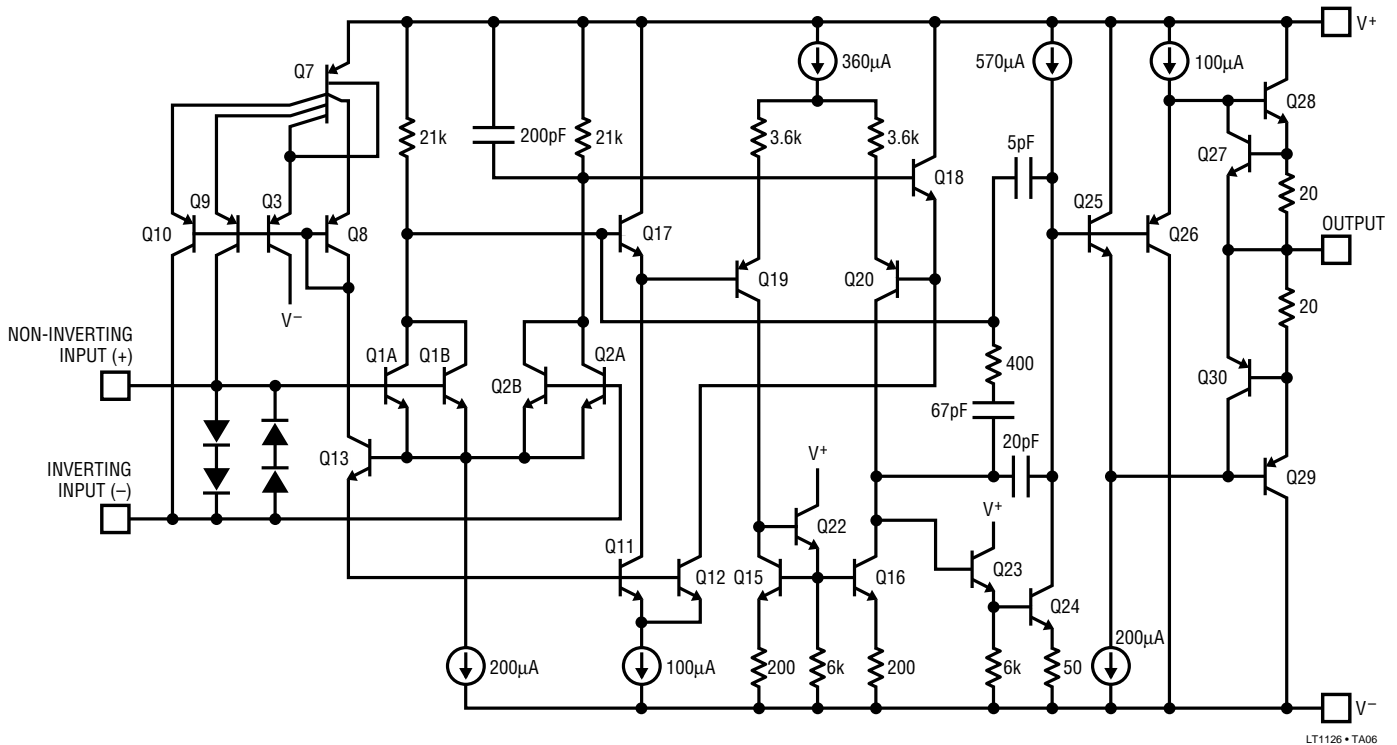
LT1126 • TA04

TYPICAL APPLICATIONS

Low Noise, Wideband, Gain = 100 Amplifier with High Input Impedance



SCHEMATIC DIAGRAM (1/2 LT1126, 1/4 LT1127)

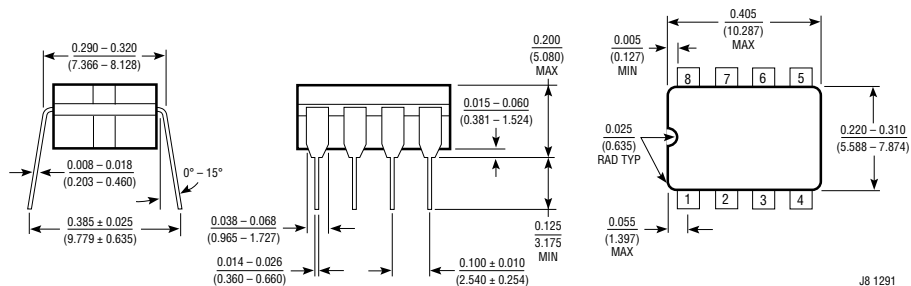


PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

J8 Package 8-Lead Ceramic DIP

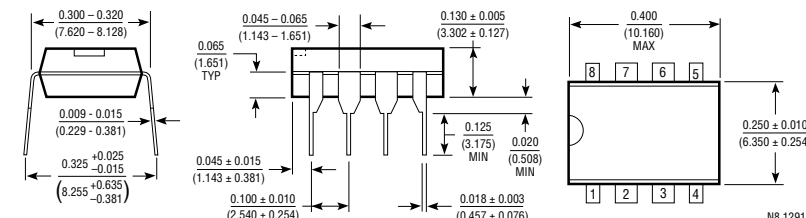
T_J MAX	θ_{JA}
160°C	100°C/W



J8 1291

N8 Package 8-Lead Plastic DIP

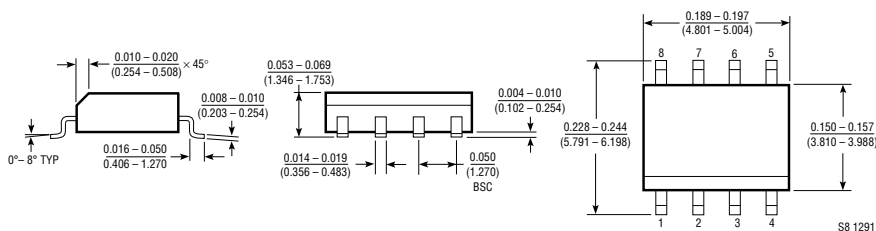
T_J MAX	θ_{JA}
140°C	130°C/W



N8 1291

S8 Package 8-Lead Plastic SOIC

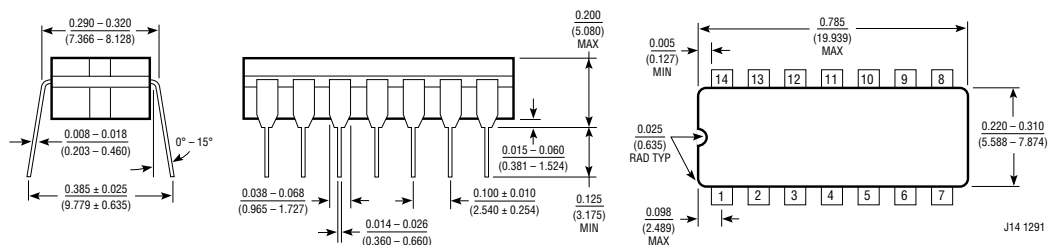
T_J MAX	θ_{JA}
140°C	190°C/W



S8 1291

J Package 14-Lead Ceramic DIP

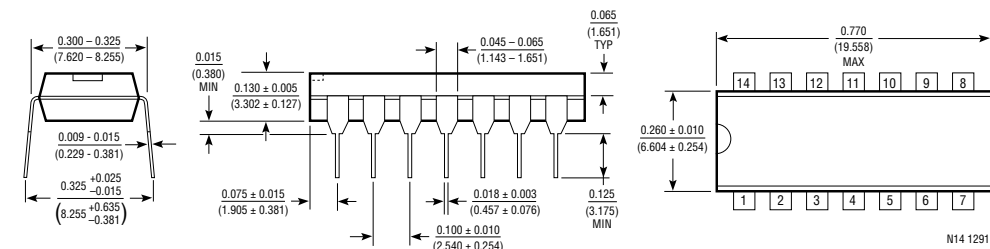
T_J MAX	θ_{JA}
160°C	80°C/W



J14 1291

N Package 14-Lead Plastic DIP

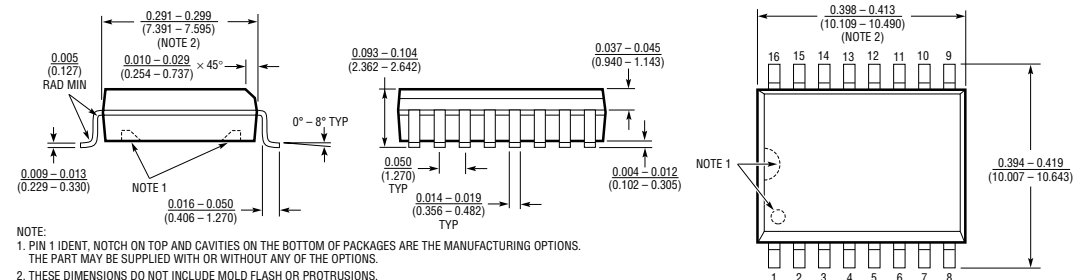
T_J MAX	θ_{JA}
140°C	110°C/W



N14 1291

SOL Package 16-Lead Plastic SOL

T_J MAX	θ_{JA}
140°C	130°C/W



NOTE:
1. PIN 1 IDENT. NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS.
2. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCH (0.15mm).