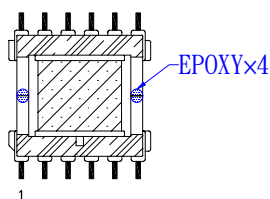
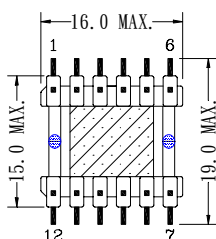
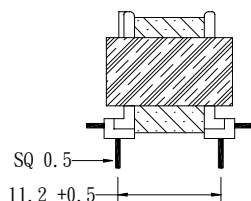
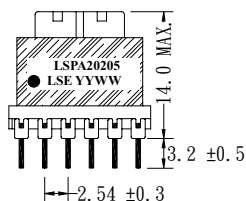


Mechanical

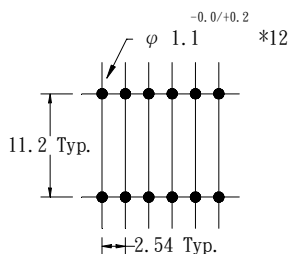


TOP VIEW

- Note :
- Unit : mm
 - Scale : F
 - 【YYWW】: Date Code



BOTTOB VIEW

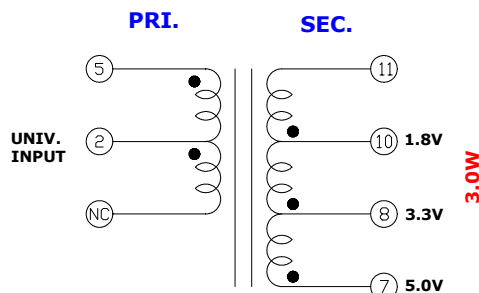


Hole Arrangement
View in soldering direction

Feature

- ◆ Deigned to intent of UL 60950
- ◆ Universal Input 85~265 Volts
- ◆ Designed for Power Integrations TNY Switch II Chip Sets

Schematic



Electrical Characteristics

A. D.C. Resistance : (25°C)

- R(5-2) : 4.750 Ω max.
R(7-11) : 49.0 mΩ max.
R(7-8) : 24.0 mΩ max.

- R(8-10) : 11.0 mΩ max.
R(10-11) : 14.0 mΩ max.

B. Inductance :

- L(5-2) : 1.492 mH ±10%

@ 132 KHz, 1V, Ls

C. Leakage Inductance :

- Lk(5-2) : 113.0 μH max.

@ 132 KHz, 1V, Ls, shorted P(8+10+11)

D. Turns Ratio :

- P (7-8) ==> 0.030 ± 0.008Vrms
P (8-10) ==> 0.020 ± 0.008Vrms
P (10-11) ==> 0.030 ± 0.008Vrms
P (7-11) ==> 0.080 ± 0.008Vrms

- @ Pins(5-2) Input 20 KHz, 1.2V
@ Pins(5-2) Input 20 KHz, 1.2V
@ Pins(5-2) Input 20 KHz, 1.2V
@ Pins(5-2) Input 20 KHz, 1.2V

E. Isolation Voltage (Hi-Pot) :

- Pri. To Sec. ==> 3000 Vac, 3mA, 60 Sec
Sec. To Core ==> 500 Vac, 3mA, 60 Sec

| Approved | Checked | Prepare | Date | Page | Rev. |
|--------------------|--------------------|--------------------|-------------|------|------|
| 許神長 09-DEC-2004 | 蔡金忠 09-DEC-2004 | 胡文秀 09-DEC-2004 | 09-DEC-2004 | 1/1 | 0 |