

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

T6A11A, JT6A11AX-AS

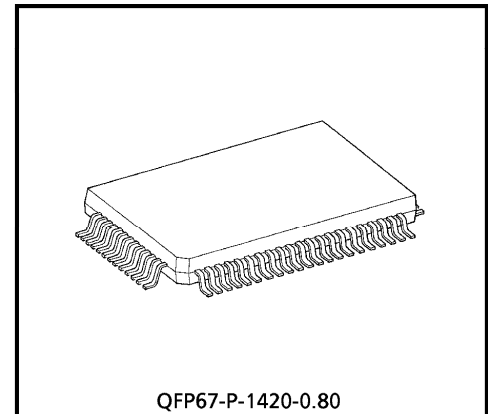
T6A11A, JT6A11AX-AS CMOS 1 CHIP LSI FOR LCD ELECTRONIC CALCULATOR

The T6A11A, JT6A11AX-AS is a 1 chip microcomputer for 12-digits 2-memory or 10-digits 2-memory electronic calculator.

T6A11A, JT6A11AX-AS can drive the liquid crystal display (LCD) with single power supply.

Single power supply operation, wide operating voltage range and low power consumption make it suitable for 1.5V solar battery operated calculator.

Besides T6A11A, JT6A11AX-AS can selectable with a pin-programmable to function of Power timer and Memory hold.



Weight : 1.20g (Typ.)

FEATURES

Operational Features :

- Display : 12-digits or 10-digits (selectable with a pin-programmable) of data, 2-digits of sign, error symbol, memory load symbol.
- Algebraic mode.
- Standard 4 functions (+, -, ×, ÷).
- Memory and grand total (GT) memory calculation.
- Accumulating GT memory register with count up (down) item counter.
- Automatic percentage operation with add-on, discount.
- Automatic delta percentage, mark-up and markdown operations.
- Square root.
- Constant calculation.
- Chain calculation.
- Change sign.
- Floating point or momentary mode (selectable with a switch) .
- Fixed point ("0", "1", "2", "3", "4" or "6" places) or floating point (selectable with a switch) .
- Adding point mode (selectable with a switch) .

980910EBA2

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- Rounding switches (rounding up, down and off) .
- Leading zero suppression.
- Trailing zero suppression.
- Punctuation on display, commas for thousands.
- Memory and GT memory contents indicator, turned on with non-zero in the memory and GT memory.
- Registration overflow, indicating that too many digits are entered (the most significant digit are protected) .
- Result overflow, indicating during calculation (most function key are locked as it happened) .
- Memory overflow indicating to flashing of memory load mark.
- TAX calculation.

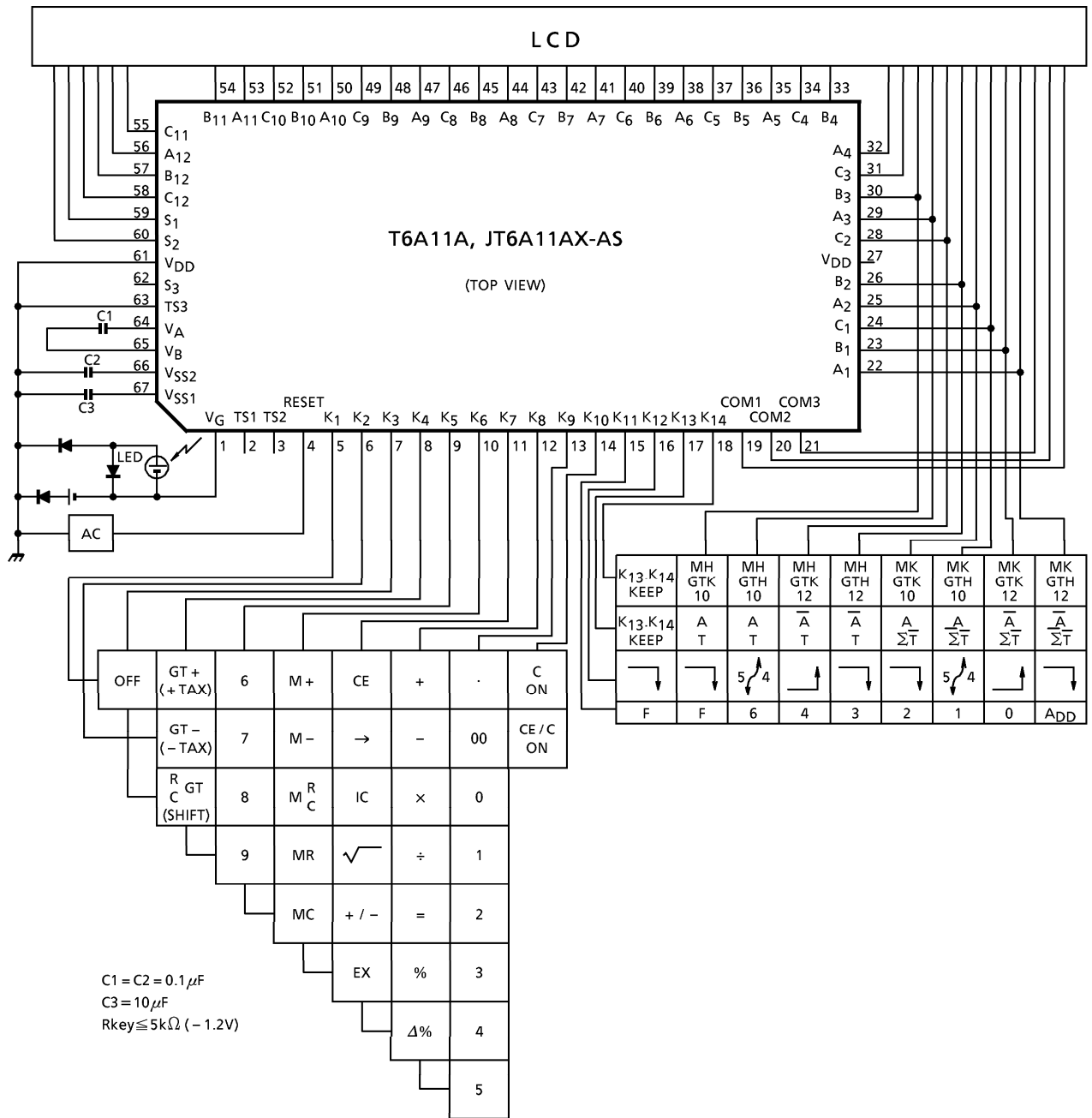
Electrical Features

- Complementary output buffer for direct driving of liquid crystal display (F.E.M LCD) .
- Oscillator / clock generator internal to chip.
- Keyboard encoding internal to chip.
- Keyboard denouncing internal to chip.
- Automatic power on clear.
- Wide supply voltage range (- 1.2 ~ - 2.0V) .
- Very low power consumption (3.3 μ W typ.) .
- Quad in line flat package.

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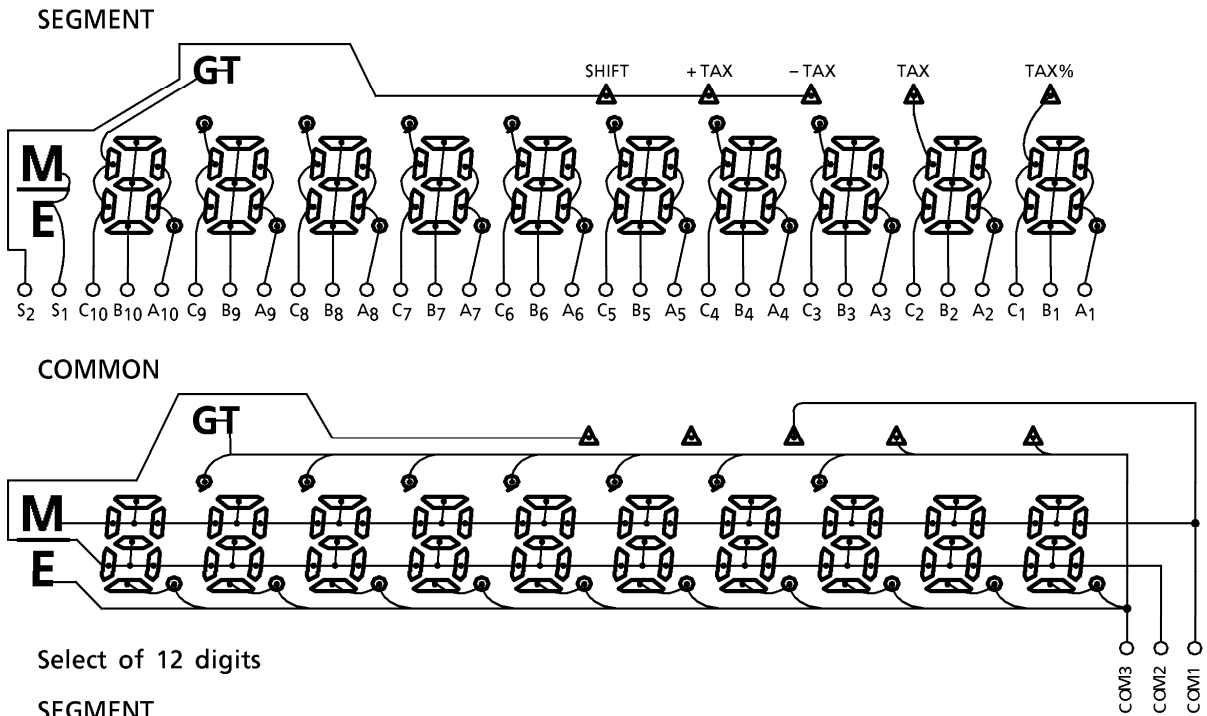
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SYSTEM BLOCK DIAGRAM

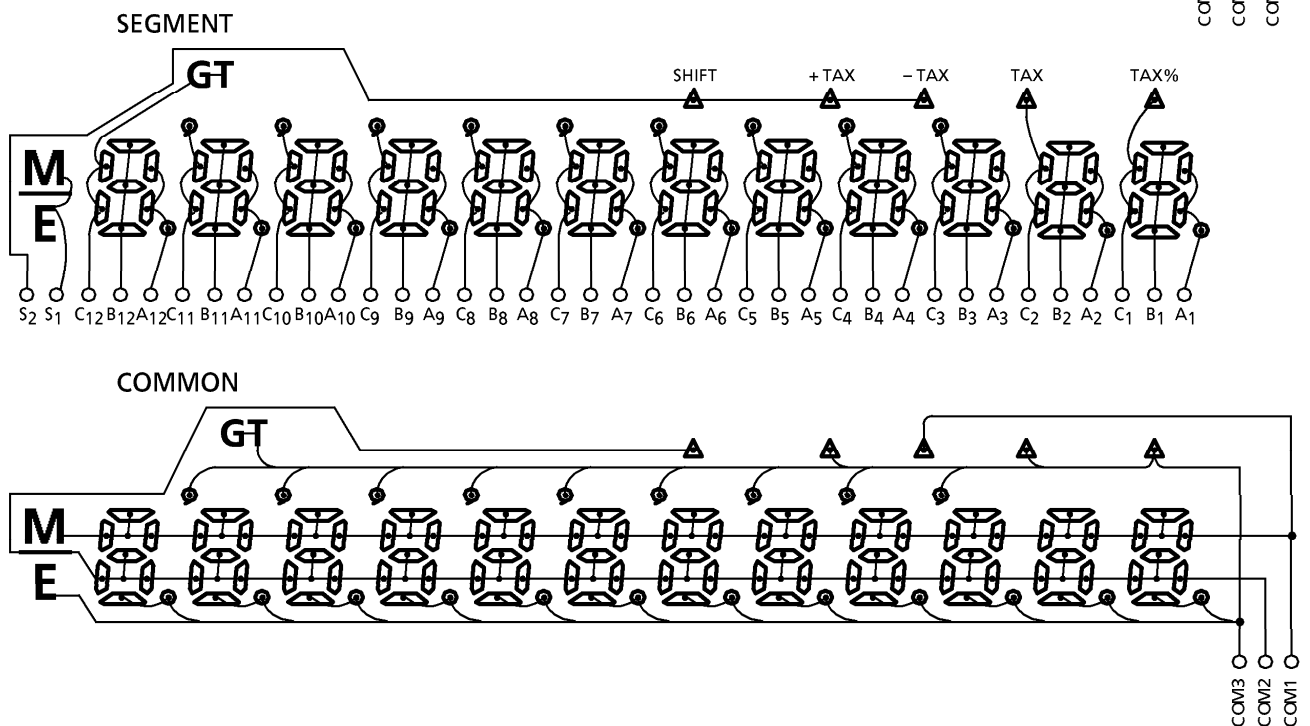


CONNECTION OF LCD

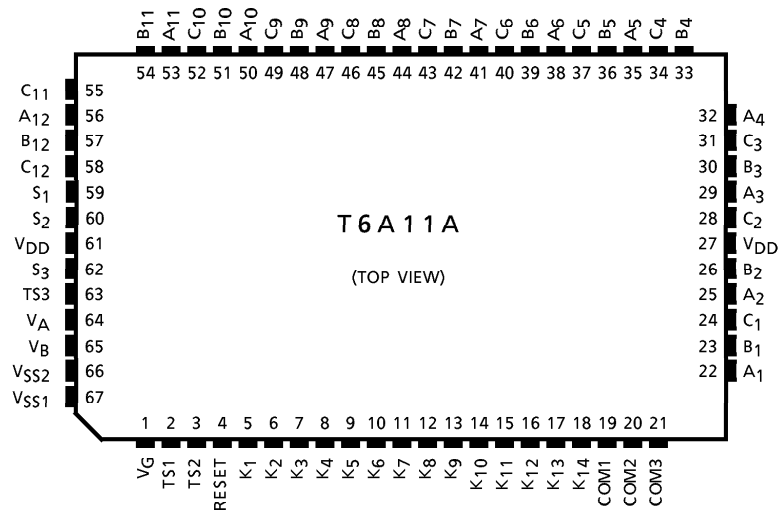
(1) Select of 10 digits



(2) Select of 12 digits

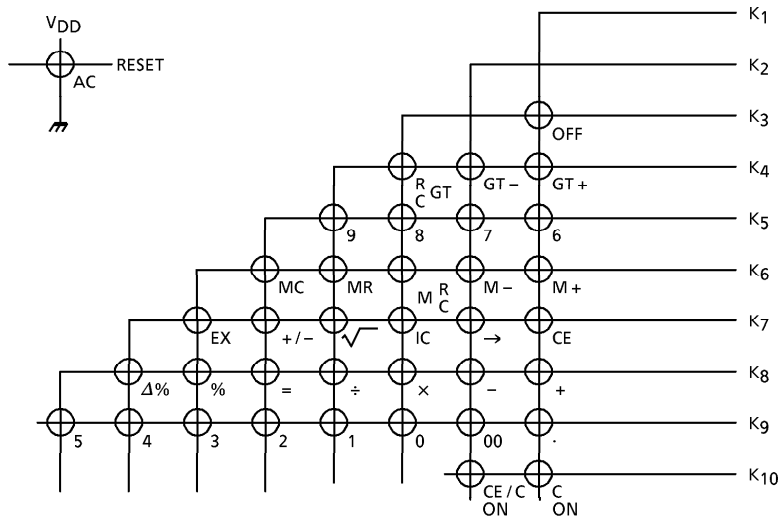


PIN LAYOUT

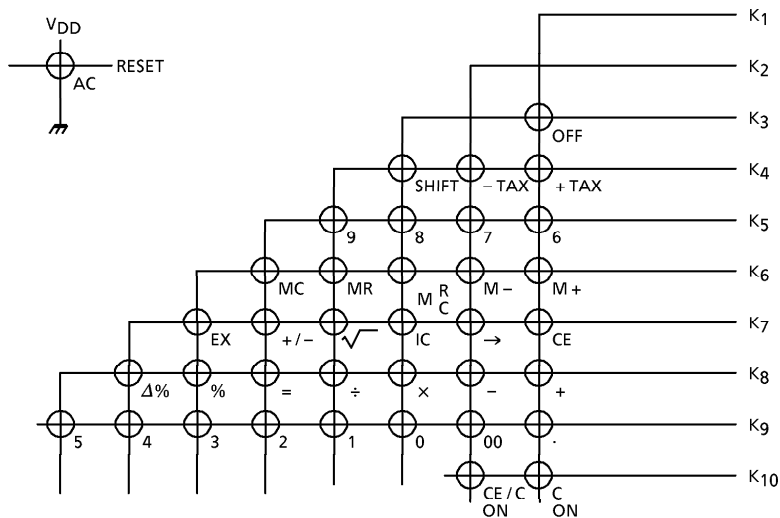


KEY LAYOUT

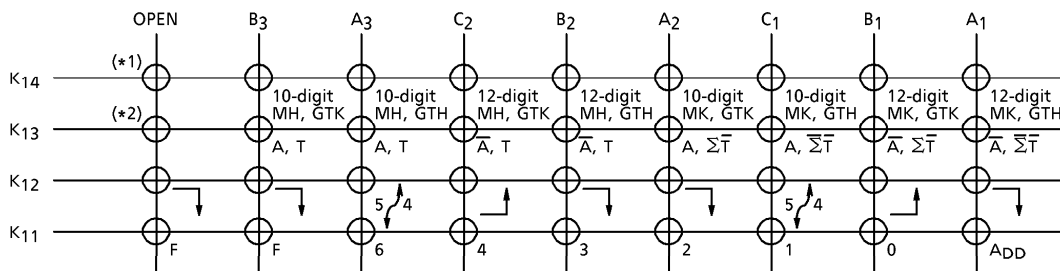
- Touch Key (Grand total memory type)



- Touch Key (TAX calculation type)



● Lock Key



- K14 ... Selectable with calculated digits and memory hold status.
 - 10digit/12digit : Digits of calculation
 - MH : Memory hold at auto power off or off function.
 - MK : Memory kill at auto power off or off function.
 - GTH : GT memory hold at auto power off or off function.
 - GTK : GT memory kill at auto power off or off function.
- K13 ... Selectable with auto power off mode and TAX calculation mode and total (Σ mode) switch.
 - A : Auto power off enable.
 - \bar{A} : Auto power off disable.
 - (*3) T : TAX calculation mode.
 - \bar{T} : GT memory mode.
 - Σ : Σ mode enable.
 - $\bar{\Sigma}$: Σ mode disable.
- K12 ... Rounding switches.
- K11 ... Selectable with fixed point or floating mode.
 - (*1), (*2) : If K13 or K14 get opened, the status before these keys open is hold. In the case of power on with K13 or K14 open, the status 10 digit and $\bar{\Sigma}$, \bar{A} mode is selected automatically.
 - (*3) : If exchange the mode of TAX calculation and GT memory, please reset the system for [AC] key.

SPECIFICATION OF CALCULATOR

Speed of Calculator (standard oscillating frequency $f\phi = 48\text{kHz}$)

- Numeral 11.8~17.7ms
- Function
 - { 1 $\boxed{+}$ 25.6ms
 - { 1 $\boxed{+}$ 2 $\boxed{+}$ 95.2ms
- Addition and Subtract
 - { 1 2 3 $\boxed{+}$ 1 $\boxed{=}$ 89.1ms
 - { 999999999 $\boxed{-}$ 0.00000001 $\boxed{=}$ 111.8ms
- Multiply
 - { 1 2 3 $\boxed{\times}$ 2 $\boxed{=}$ 109.6ms
 - { 1 $\boxed{\times}$ 999999999 $\boxed{=}$ 207.7ms
- Device
 - { 1 2 3 $\boxed{\div}$ 3 $\boxed{=}$ 147.9ms
 - { 999999999 $\boxed{\div}$ 1 $\boxed{=}$ 249.0ms
- Memory calculation
 - { 2 $\boxed{M+}$ 143.3ms
 - { 999999999 $\boxed{\div}$ 1 $\boxed{M+}$ 296.2ms
- Square root
 - { 999999999 $\boxed{\sqrt{\quad}}$ 167.7ms
 - { 2 $\boxed{\sqrt{\quad}}$ 125.0ms

Key for Calculator

- 0 . , 0 ~ 9 : Number
- .
- +/- : Changer Sign
- + - × ÷ : Function
- = √ % Δ%
- M+ M- GT+ GT- : Memory
- MC MR M_R
C R_C
GT
- EX : Exchange
- : Shift
- IC : Item Counter Grand total memory type ... MAX. count 999.
TAX calculation type ... MAX. count 99.
- CE CE/C
(ON) C
(ON) : Clear
- OFF : OFF
- AC : SYSTEM RESET

Operation Example

1. Fixed Point calculation

① Key	Display	Fixed Point Place	② Key	Display	Fixed Point Place
\boxed{C}	0.	DP = 3 (5 / 4)	\boxed{C}	0.	DP = 0 ($\boxed{\uparrow}$)
2	2.		1	1.	
$\boxed{\div}$	2.		$\boxed{\cdot}$	1.	
3	3.		2	1.2	
$\boxed{=}$	0.667		3	1.23	
2	2.		$\boxed{+}$	1.23	
$\boxed{\cdot}$	2.		1	1.	
3	2.3		$\boxed{\cdot}$	1.	
$\boxed{+}$	2.3		1	1.1	
4	4.		$\boxed{=}$	3.	
$\boxed{M+}$	6.300		9	9.	
1	1.		$\boxed{\sqrt{\quad}}$	3.	
$\boxed{\cdot}$	1.		$\boxed{\times}$	3.	
2	1.2		1	1.	
$\boxed{M+}$	1.200		$\boxed{\cdot}$	1.	
			1	1.1	DP = F
\boxed{MR}	7.5		$\boxed{=}$	3.3	

2. Adding Point mode calculation

Key	Display	Key	Display	Key	Display
\boxed{C}	0.	$\boxed{M+}$	0.02M	$\boxed{=}$	33.27M -
1	1.	3	3.M	2	2.M
23	123.	.	3.M	$\boxed{+}$	0.02M
$\boxed{+}$	1.23	123	3.123M	9	9.M
3	3.	$\boxed{M+}$	3.12M	$\boxed{\cdot}$	9.M
$\boxed{=}$	1.26	\boxed{MR}	3.14M	$\boxed{\sqrt{\quad}}$	3.M
3	3.	\boxed{C}	0.M	$\boxed{=}$	3.02M
2	32.	1	1.M		
$\boxed{\times}$	32.	23	123.M		
3	3.	$\boxed{-}$	1.23M		
$\boxed{\cdot}$	3.	3	3.M		
000	3.000	4	34.M		
$\boxed{=}$	96.00	$\boxed{\cdot}$	34.M		
2	2.	5	34.5M		

3. Constant Calculation

① Multiplication

Key	Display	Constant
k	k	
\times	k	
a	a	
$=$	$k \cdot a$	$k \times$
b	b	$k \times$
$=$	$k \cdot b$	$k \times$

③ Addition

a	a	
$+$	a	
k	k	
$=$	$a + k$	$+ k$
b	b	$+ k$
$=$	$b + k$	$+ k$

⑤ Percentage

k	k	
\times	k	
a	a	
$\%$	$k \cdot a / 100$	$k \times$
b	b	$k \times$
$\%$	$k \cdot b / 100$	$k \times$

⑦ Add-on

k	k	
$+$	k	
a	a	
$\%$	$k \cdot (1 + a / 100)$	$k +$
b	b	$k +$
$\%$	$k \cdot (1 + b / 100)$	$k +$

② Division

Key	Display	Constant
a	a	
\div	a	
k	k	
$=$	a / k	$\div k$
b	b	$\div k$
$=$	b / k	$\div k$

④ Subtraction

a	a	
$-$	a	
k	k	
$=$	$a - k$	$- k$
b	b	$- k$
$=$	$b - k$	$- k$

⑥ Percentage

a	a	
\div	a	
k	k	
$\%$	$100 \cdot a / k$	$+ k$
b	b	$\div k$
$\%$	$100 \cdot b / k$	$\div k$

⑧ Discount

k	k	
$-$	k	
a	a	
$\%$	$k \cdot (1 - a / 100)$	$k -$
b	b	$k -$
$\%$	$k \cdot (1 - b / 100)$	$k -$

4. $\Delta\%$ Calculations

① Key	Display
a	a
$\boxed{+}$	a
b	b
$\boxed{\Delta\%}$	$100 \cdot (a + b) / b$

② Key	Display
a	a
$\boxed{-}$	a
b	b
$\boxed{\Delta\%}$	$100 \cdot (a - b) / b$

5. Mark-up, Mark-down Calculations

① Mark-up	
Key	Display
a	a
$\boxed{\div}$	a
b	b
$\boxed{\Delta\%}$	$a / (1 - b / 100)$
$\boxed{\Delta\%}$	$ a / (1 - b / 100) - a $

② Mark-down	
Key	Display
a	a
$\boxed{\div}$	a
b	b
$\boxed{+/-}$	- b
$\boxed{\Delta\%}$	$a / (1 + b / 100)$
$\boxed{\Delta\%}$	$ a / (1 + b / 100) - a $

6. Add-on, Discount Calculations

Add-on	
Key	Display
① a	a
$\boxed{\times}$	a
b	b
$\boxed{\%}$	$a \cdot b / 100$
$\boxed{+}$	$a \cdot b / 100$
$\boxed{=}$	$a (1 + b / 100)$
③ a	a
$\boxed{+}$	a
b	b
$\boxed{\%}$	$a (1 + b / 100)$
⑤ a	a
$\boxed{\times}$	a
b	b
$\boxed{\Delta\%}$	$a (1 + b / 100)$

Discount	
Key	Display
② a	a
$\boxed{\times}$	a
b	b
$\boxed{\%}$	$a \cdot b / 100$
$\boxed{-}$	$a \cdot b / 100$
$\boxed{=}$	$a (1 - b / 100)$
④ a	a
$\boxed{-}$	a
b	b
$\boxed{\%}$	$a (1 - b / 100)$
⑥ a	a
$\boxed{\times}$	a
b	b
$\boxed{+/-}$	- b
$\boxed{\Delta\%}$	$a (1 - b / 100)$

7. Average Operation use of the Item Counter

Key	Display	Item Counter	Key	Display	Item Counter
A	A	0	\square -	A + B + C + D	2
\square +	A	1	D	D	2
B	B	1	\square +	A + B + C	3
\square +	A + B	2	E	E	3
C	C	2	\square =	A + B + C + E	4
\square +	A + B + C	3	\square ÷	A + B + C + E	4
D	D	3	\square IC	4	4
\square +	A + B + C + D	4	\square =	(A + B + C + E) / 4	5

8. TAX Calculation

	Key Op.	Display
(1)	A	A
	\square SHIFT	A \square SHIFT
	\square + TAX	A \square TAX%
(2)	\square SHIFT	0. \square SHIFT
	\square - TAX	A \square TAX%
(3)	B	B
	\square + TAX	B (1 + A / 100) \square + TAX
	\square + TAX	B · A / 100 \square TAX
	\square + TAX	B (1 + A / 100) \square + TAX
	\square + TAX	B · A / 100 \square TAX
(4)	B	B
	\square - TAX	B / (1 + A / 100) \square - TAX
	\square - TAX	B - B / (1 + A / 100) \square TAX
	\square - TAX	B / (1 + A / 100) \square - TAX
	\square - TAX	B - B / (1 + A / 100) \square TAX

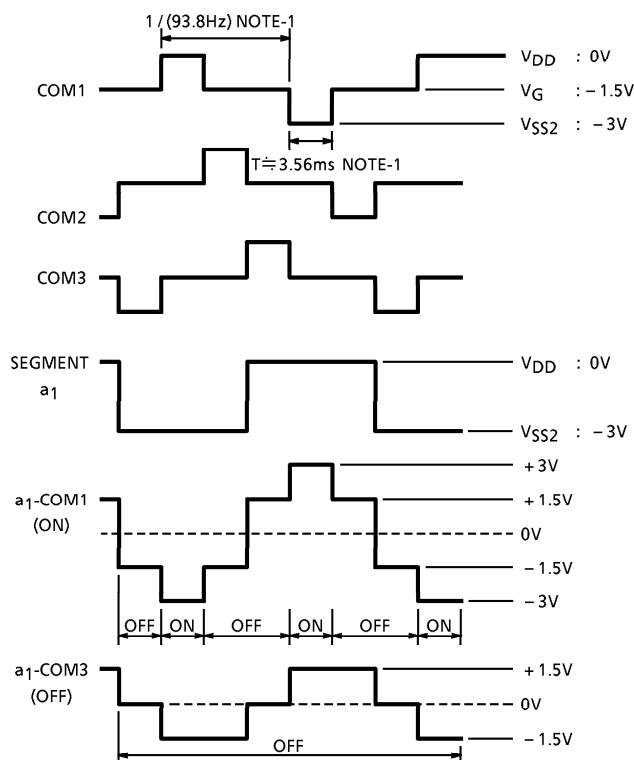
MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_G	+0.3 ~ -2.0	V
Input Voltage	V_{IN}	+0.3 ~ $V_G - 0.3$	V
Operating Temperature	T_{opr}	0 ~ 40	°C
Storage Temperature	T_{stg}	-55 ~ 125	°C

ELECTRICAL CHARACTERISTICS ($V_G = -1.5 \pm 0.2V$, $V_{SS2} = -3.0 \pm 0.4V$, $V_{DD} = 0V$, $T_a = 25^\circ C$)

PARAMETER	SYMBOL	TEST CIRCUIT	PIN NAME	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V_G	—	—	—	-1.2	-1.5	-2.0	V
"1" Input Voltage	$V_{IH} (1)$	—	K ₃ ~K ₁₀ RESET	—	$V_G + 0.4$	—	V_G	V
"1" Input Voltage	$V_{IH} (2)$	—	K ₁₁ ~K ₁₄	—	$V_{SS2} + 0.4$	—	V_{SS2}	V
"0" Input Voltage	V_{IL}	—	K ₃ ~K ₁₄ RESET	—	0	—	-0.4	V
"1" Output Voltage	$V_{OH} (1)$	—	SEGMENT COM1~3	—	$V_{SS2} + 0.2$	—	V_{SS2}	V
"0" Output Voltage	$V_{OL} (1)$	—	SEGMENT COM1~3	—	0	—	-0.2	V
"M" Output Voltage	V_{OM}	—	COM1~3	—	$V_G + 0.2$	—	$V_G - 0.2$	V
"1" Output Voltage	$V_{OH} (2)$	—	K ₁ ~K ₁₀	—	$V_G + 0.2$	—	V_G	V
"0" Output Voltage	$V_{OL} (2)$	—	K ₁ ~K ₁₄	—	0	—	-0.2	V
"1" Output Resistance	R_{OH}	—	SEGMENT COM1~3	$V_{OUT} = V_{SS2} + 0.5V$	—	—	70	k Ω
"0" Output Resistance	R_{OL}	—	SEGMENT COM1~3	$V_{OUT} = -0.5V$	—	—	70	k Ω
Key Pull Up Resistance	$R_{KEYH} (1)$	—	RESET	$V_{OUT} = 0V$	156	—	364	k Ω
	$R_{KEYH} (2)$	—	K ₁ ~K ₁₀	$V_{OUT} = 0V$	240	—	560	
Key Read Pull Up Resistance	$R_{KEYH} (3)$	—	K ₁ ~K ₁₀	$V_{OUT} = 0V$	30	—	600	k Ω
Key Pull Down Resistance	$R_{KEYL} (1)$	—	RESET K ₁ ~K ₁₀	$V_{OUT} = -0.5V$	—	—	10	k Ω
	$R_{KEYL} (2)$	—	K ₁₁ ~K ₁₄	$V_{OUT} = V_{SS2}$	120	—	800	
Oscillating Frequency	(WAIT)	$f_{\phi} WAIT$	—	$V_G = -1.5V$	5.4	9.0	12.6	kHz
	(OPERATE)	$f_{\phi} OP$	—	$V_G = -1.5V$	28.8	48	67.2	
Frame Frequency	f_F	—	SEGMENT COM1~3	$V_G = -1.5V$	56.3	93.8	131	Hz
Supply Current	1 (WAIT)	I_{DDWAIT}	—	$V_G = -1.5V$	—	2.2	3.4	μA
	2 (OPERATE)	I_{DDOP}	—	$V_G = -1.2V$	—	7.0	11.0	
	3 (OFF)	I_{DDOFF}	—	$V_G = -1.5V$	—	—	2.0	
Power Off Timer Times	T	—	—	$V_G = -1.5V$	429	600	1001	s

WAVEFORMS FOR DISPLAY



NOTE-1 at $f_{\phi} = 9\text{kHz}$

PAD LOCATION TABLE

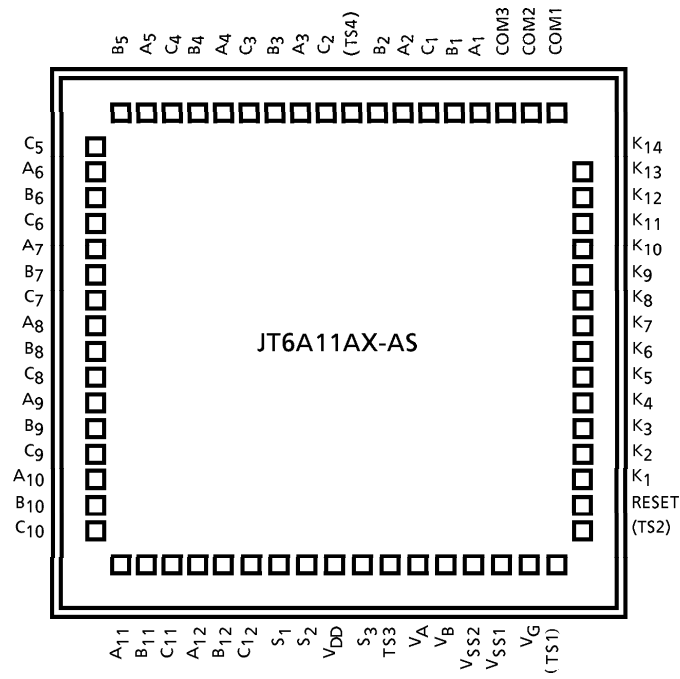
(μm)

NAME	X POINT	Y POINT
VSS1	971	- 1469
VSS2	775	- 1469
VB	609	- 1469
VA	424	- 1469
TS3	252	- 1469
S3	100	- 1469
VDD	- 52	- 1469
S2	- 203	- 1469
S1	- 355	- 1469
C12	- 507	- 1469
B12	- 659	- 1469
A12	- 810	- 1469
C11	- 980	- 1469
B11	- 1162	- 1469
A11	- 1358	- 1469
C10	- 1408	- 1193
B10	- 1408	- 1042
C10	- 1408	- 890
C9	- 1408	- 738
B9	- 1408	- 586
A9	- 1408	- 435
C8	- 1408	- 283
B8	- 1408	- 131
A8	- 1408	20
C7	- 1408	172
B7	- 1408	324
A7	- 1408	475
C6	- 1408	627
B6	- 1408	779
A6	- 1408	936
C5	- 1408	1119
B5	- 1358	1469
A5	- 1169	1469

NAME	X POINT	Y POINT
C4	- 999	1469
B4	- 847	1469
A4	- 696	1469
C3	- 544	1469
B3	- 392	1469
A3	- 240	1469
C2	- 89	1469
*(TS4)	89	1469
B2	241	1469
A2	392	1469
C1	544	1469
B1	696	1469
A1	847	1469
COM3	999	1469
COM2	1166	1469
COM1	1358	1469
K14	1408	1175
K13	1408	1023
K12	1408	871
K11	1408	720
K10	1408	503
K9	1408	352
K8	1408	200
K7	1408	48
K6	1408	- 104
K5	1408	- 255
K4	1408	- 407
K3	1408	- 559
K2	1408	- 710
K1	1408	- 862
RESET	1408	- 1023
*(TS2)	1408	- 1175
*(TS1)	1367	- 1469
VG	1160	- 1469

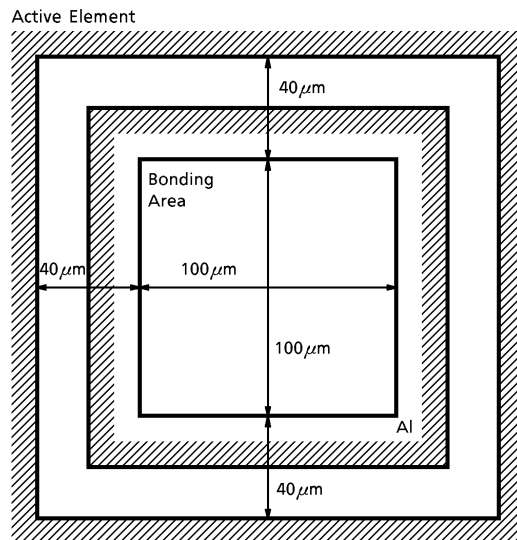
*() Do not connect.

CHIP LAYOUT



Chip size : 3.28×3.46 [mm]
 Chip thickness : 440 ± 30 μm
 Substrate : V_{DD}

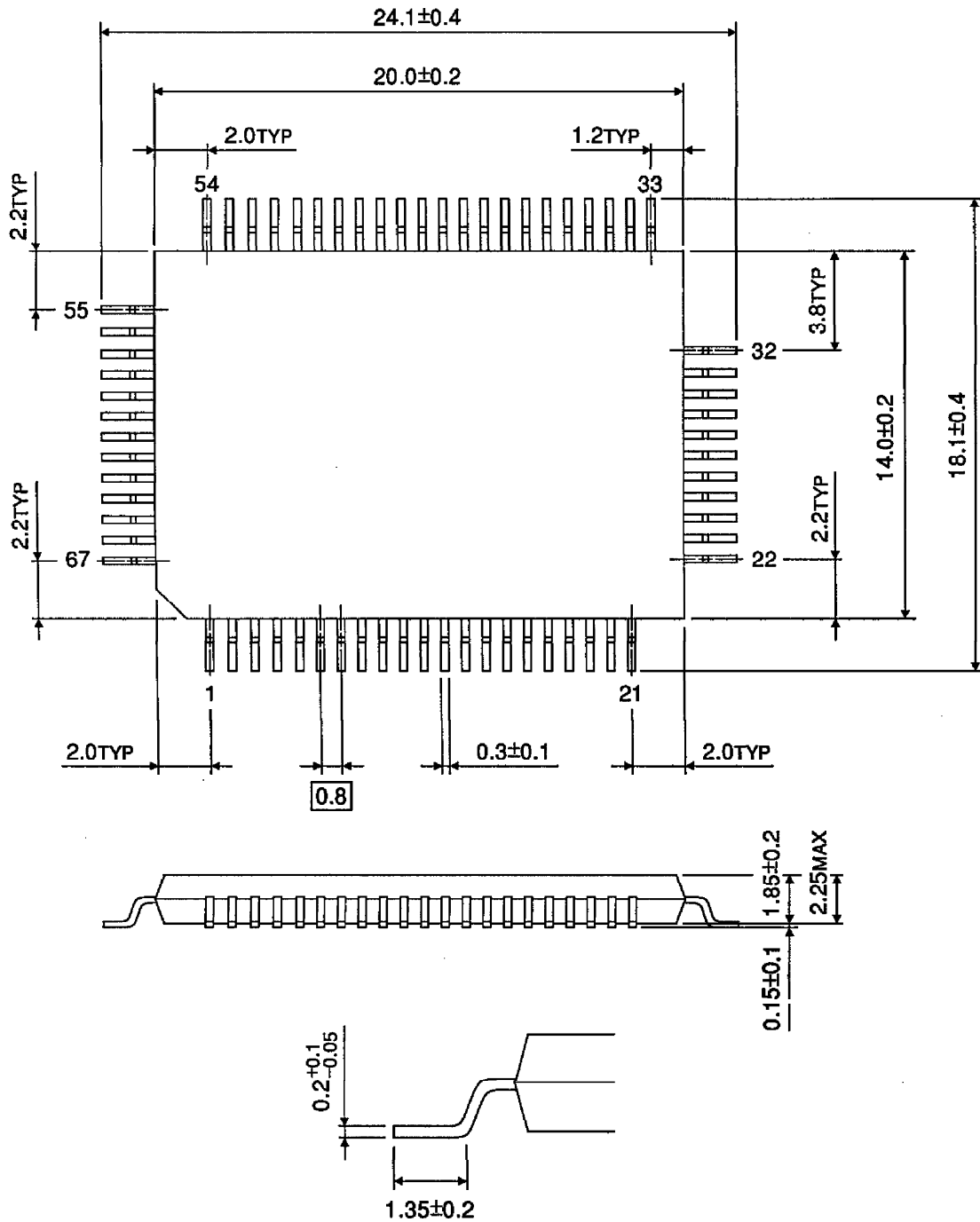
PAD LAYOUT



PAD Pitch 160 μm

OUTLINE DRAWING
QFP67-P-1420-0.80

Unit : mm



Weight : 1.20g (Typ.)

GENERAL SPECIFICATION FOR CALCULATOR LSI BARE CHIP**1. Purpose**

This is to specify the quality standard for the integrated circuit produced by TOSHIBA CORPORATION (hereinafter referred as to VENDOR) to be delivered to PURCHASER.

2. Definition

This specification applies only to the calculator LSI bare chip produced by VENDOR and purchased by PURCHASER and defined the general specification items.

3. Priority of specifications

When the discrepancies or questions happen to the specifications and instructions provided by VENDOR, the priority shall be ranked as follows.

- 1) Individual specification for the calculator LSI bare chip.
(Both PURCHASER and VENDOR are confirmed by the special sheets.)
- 2) General specifications for the calculator LSI bare chip.
- 3) Other related specifications and standards.

4. Characteristics

To be shown in the individual specification sheets.

The individual specification shall consist of the following 4 items in principle.

- 1) Rated specifications.
- 2) Electrical characteristics.
- 3) Pin configuration & mechanical dimensions.
- 4) Others.

5. Inspection of product for delivery**5.1 Inspection lot**

- a) Inspection lot shall consist of products produced by same material under same design, through same production process, and same facilities and assured same quality by same quality assurance method, and lot number shall be put on all trays to be able to trace the lot history.
- b) The quantity of products per Inspection lot shall consist of all the same VENDOR's lot number.

5.2 Sampling plan

Statistical sampling and inspection shall be in accordance with MIL-STD-105D single sampling plans for normal inspections, general inspection level II.

The acceptable quality level (AQL) shall be specified in following table :

TEST ITEM	AQL (%)
Electrical	2.5
Visual	4.0

5.3 Electrical criteria

Criteria of Electrical Characteristics are prescribed in Attachment-1.

5.4 Visual criteria

Visual Criteria are prescribed in Attachment-2.

6. Incoming inspection

6.1 General

- a) PURCHASER's incoming inspection should be done within 15 days after PURCHASER receives the quantity of products in principle.
- b) PURCHASER shall report the results of incoming inspection to VENDOR and provide VENDOR with detailed data in failure rate and items regarding VENDOR's lot number respectively, if VENDOR demands the report from PURCHASER.

6.2 Inspection procedure

PURCHASER should do his incoming inspection according to the following procedure.

- a) First : Visual inspection should be done.
- b) Next : Electrical and other inspection should be done under condition with bare chip before going into PURCHASER's process.

7. Treatment for defective lot and products

Regarding the defective lot and defective products which are found through PURCHASER's incoming inspection, PURCHASER can be returned to VENDOR with detailed description on failures concerned.

However, if VENDOR cannot receive the defective items within 30 days after PURCHASER's incoming inspection, VENDOR should be able to make no reference to the defective problem.

8. Packing and labeling

- a) Dice shall be placed in die tray with the top metalization facing up in order.
- b) In principle, a pile consists of 5 trays and several piles are packed in a package. These piles and packages are indicated with printed labels as shown below.

Date	
Name	
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- c) PURCHASER shall return these packing materials to VENDOR on VENDOR's demand.

9. Storage criteria

Solid state chips, unlike packaged devices, are non-hermetic devices normally fragile and small in physical size, and therefore, require special handling considerations as follows :

- 9.1 Chips must be stored under proper conditions to insure that they are not subjected to a moist and/or contaminated atmosphere that alter their electrical, physical, or mechanical characteristics.
After the shipping container is opened, the chips must be stored under the following conditions :
 - A. Storage temperature, 40°C max.
 - B. Relative humidity, 50% max.
 - C. Clean, dust-free environment.
- 9.2 The user must exercise proper care when handling chips or wafers to prevent even the slightest physical damage to the chip.
- 9.3 During mounting and lead bounding of chips the user must use proper assembly techniques to obtain proper electrical, thermal, and mechanical performance.
- 9.4 After the chip has been mounted and bounded, any necessary procedure must be followed by the user to insure that these non-hermetic chips are not subjected to moist or contaminated atmosphere which might cause the development of electrical conductive paths across the relatively small insulating surfaces.
In addition, proper consideration must be given to the protection of these devices from other harmful environments which could conceivably adversely affect their proper performance.

10. Handling criteria

The user should find the following suggested precautions helpful in handling chips.

In any event, because of the extremely small size and fragile nature of chips, care should be taken in handling these devices.

10.1 Grounding

- a) Bonders, pellet pickup tools, table tops, trim and form tools, sealing equipment, and other equipment used in chip handling should be properly grounded.
- b) Operator should be properly grounded.

10.2 In-process handling

- a) Assemblies or subassemblies of chips should be transported and stored in conductive carriers.
- b) All external leads of the assemblies or subassemblies should be shorted together.

VISUAL INSPECTION CRITERIA

1. Visual inspection magnification shall be 40 × in principle.

2. Defects defined :

2.1 Thickness

See the technical data sheet.

2.2 Chip and crack

A die shall be rejected if :

- a) Any crack of chip extends greater than 35 μ m in length into the inside of the scribble line. (see Fig.1)

2.3 Metallization

A die shall be rejected if :

- a) More than 25% of the designed area of the metallization is missing at any bonding pad.
- b) There is a short or break which affects electrical characteristics in any lead pattern. (see Fig.2)

2.4 Glass protection coat

A die shall be rejected if :

- a) It exhibits glass protection coat which covers more than 25% of any active bonding pad.

2.5 Attached foreign material

A die shall be rejected if :

- a) A die is covered by stains or attached foreign material which size is more than 5 times as large as a bonding pad area.
- b) It exhibits residual ink, stains or attached foreign material which covers more than 20% of any active bonding pad. (see Fig.3)

2.6 Others

A die shall be rejected if :

- a) There have no evident probed impression on the bonding pads.
- b) A inked die, defective die, is intermized.

3. Limit samples should be fized, if necessary.

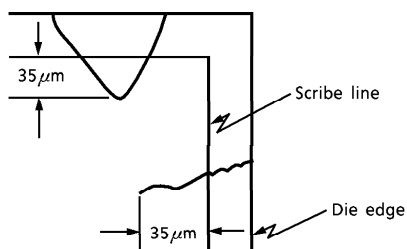


Fig.1

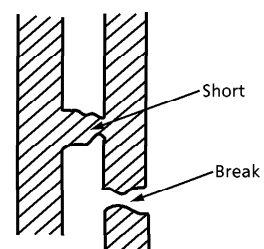


Fig.2 Lead pattern

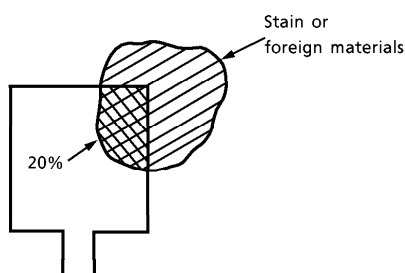
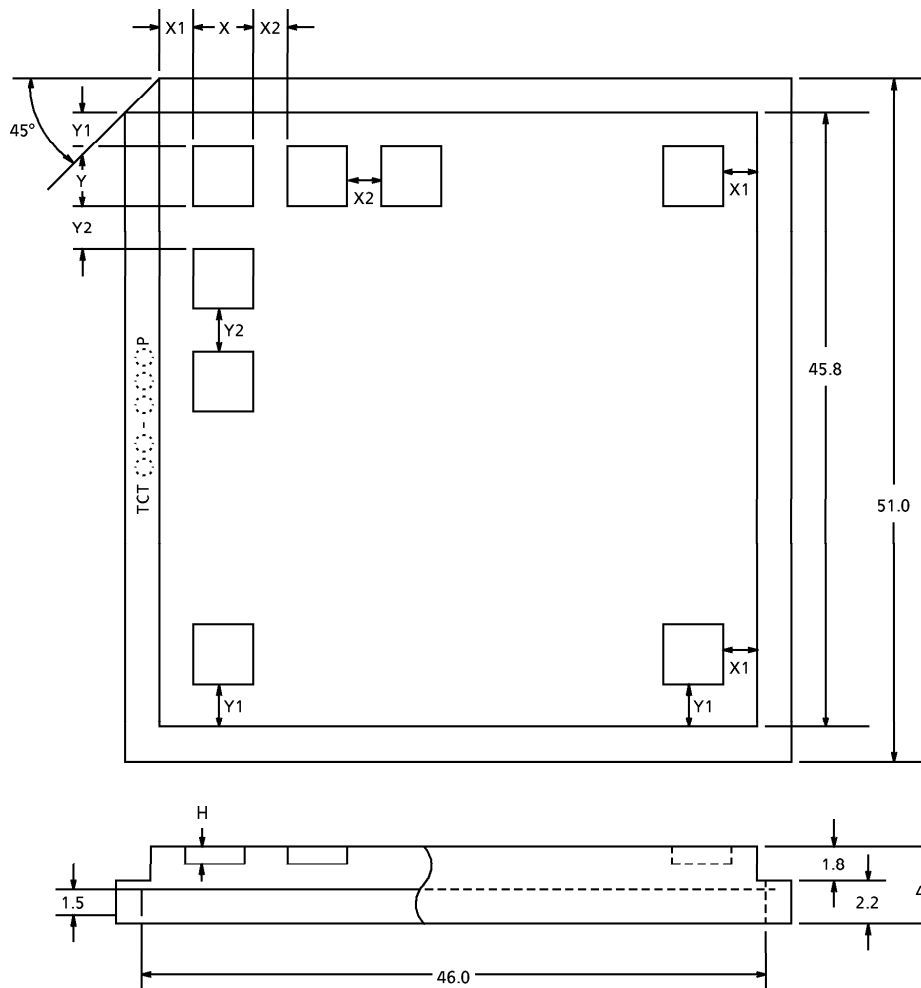


Fig.3

OUTSIDE DIMENSIONS OF CHIP TRAY



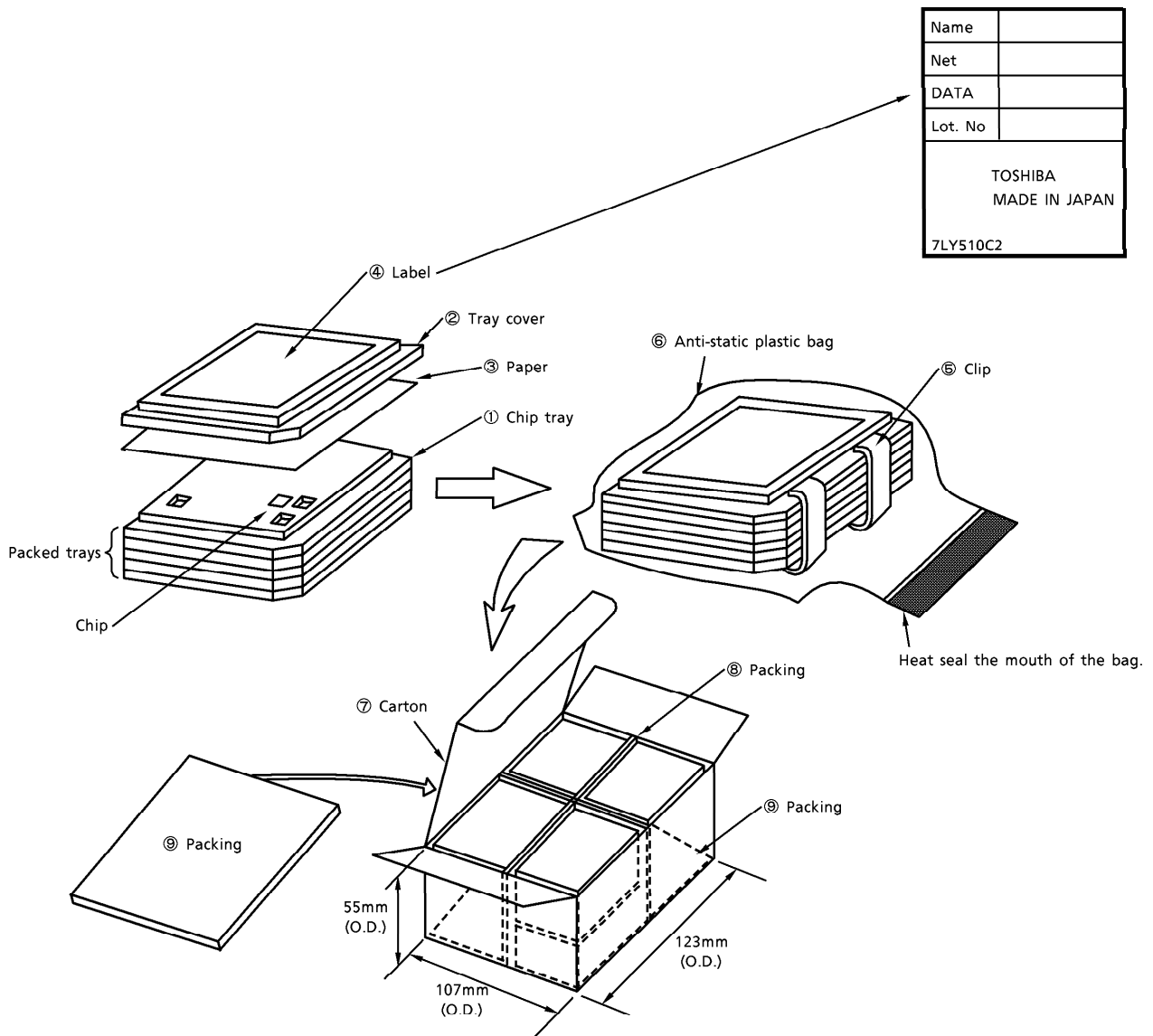
Unit : mm

CHIP NAME	TRAY NAME	X	Y	(H)	No. OF POCKETS	X1	X2	Y1	Y2
JT6A11AX-AS	TCT38-060P	3.80	3.80	0.60	10 × 10 (100)	1.200	0.600	1.200	0.600

Tray material :

Carbon-containing polypropylene

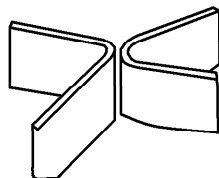
PACKING METHOD-1

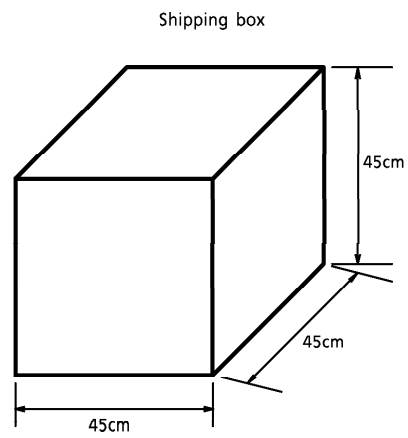


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Place eight bags of chip trays in each carton box ⑦. Lay one sheet of packing ⑨ (7UF44F) before closing the lid of the cart box. (See the diagram above.)

Prepare packing ⑨ by cutting 7UF44F into halves and folding each in half as shown below ; use them as inner partitions.



PACKING METHOD-2

- Inner box : Containing 20 boxes
- Weight : Approx. 15kg (including packing material)
- Material : Corrugated cardboard
- IC contents : $36 \times 5 \times 8 \times 20 = 28.8\text{kpcs}$.