



CYPRESS

CY2278A

# Pentium®/II Clock Synthesizer/Driver for Mobile PCs with Intel 82430TX and No SDRAM

## Features

- Mixed 2.5V and 3.3V operation
- Complete clock solution to meet requirements of mobile Pentium® and Pentium® II motherboards
  - Seven CPU clock outputs (three at 3.3V, and four at 2.5V or 3.3V) with eight selectable clock frequencies.
  - Ten 3.3V synchronous PCI clock outputs
  - Two 3.3V USB/IR clocks at 48 MHz
  - One Keyboard clock at 8 MHz
  - One 2.5V IOAPIC clock at 14.318 MHz
  - Two 3.3V Ref. clocks at 14.318 MHz
- Dedicated power management for portable systems
  - Separate output enable pins for CPU, PCI, and USB/IR clock sets
  - Free-running PCI and CPU clocks (see options)
- Factory-EPROM programmable output drive and slew rate for EMI customization
- Custom configuration with factory-EPROM programmable CPU, PCI, and USB/IR frequencies.
- Low skew and low jitter outputs
- Available in space-saving 48-pin TSSOP package

## Functional Description

The CY2278A is a Clock Synthesizer/Driver chip for Pentium, or Pentium II portable PCs designed with the 82430TX or similar core-logic chipsets. There are four options available as shown in the selector guide.

The CY2278A outputs seven CPU clocks, three of which run at 3.3V and four run at either 2.5V or 3.3V, depending on the

voltage applied on pin 42. There are ten PCI clocks, running at one half the CPU clock frequency. Free-running PCI and CPU clocks are available as options shown in the selector guide. Additionally, the part outputs two 3.3V USB/IR clocks at 48 MHz, one Keyboard clock at 8 MHz, one 2.5V IOAPIC clock at 14.318 MHz, and two 3.3V reference clocks at 14.318 MHz.

The CY2278 family contains several features for output flexibility and power control. The CPU, PCI, USB and IR clock frequencies are all factory EPROM-programmable. Three hardware select inputs support eight CPU clock frequencies from 20 – 75 MHz. Additionally, each of the CPU, PCI, and USB/IR clock sets can be turned on or off with a dedicated enable input pin for power management.

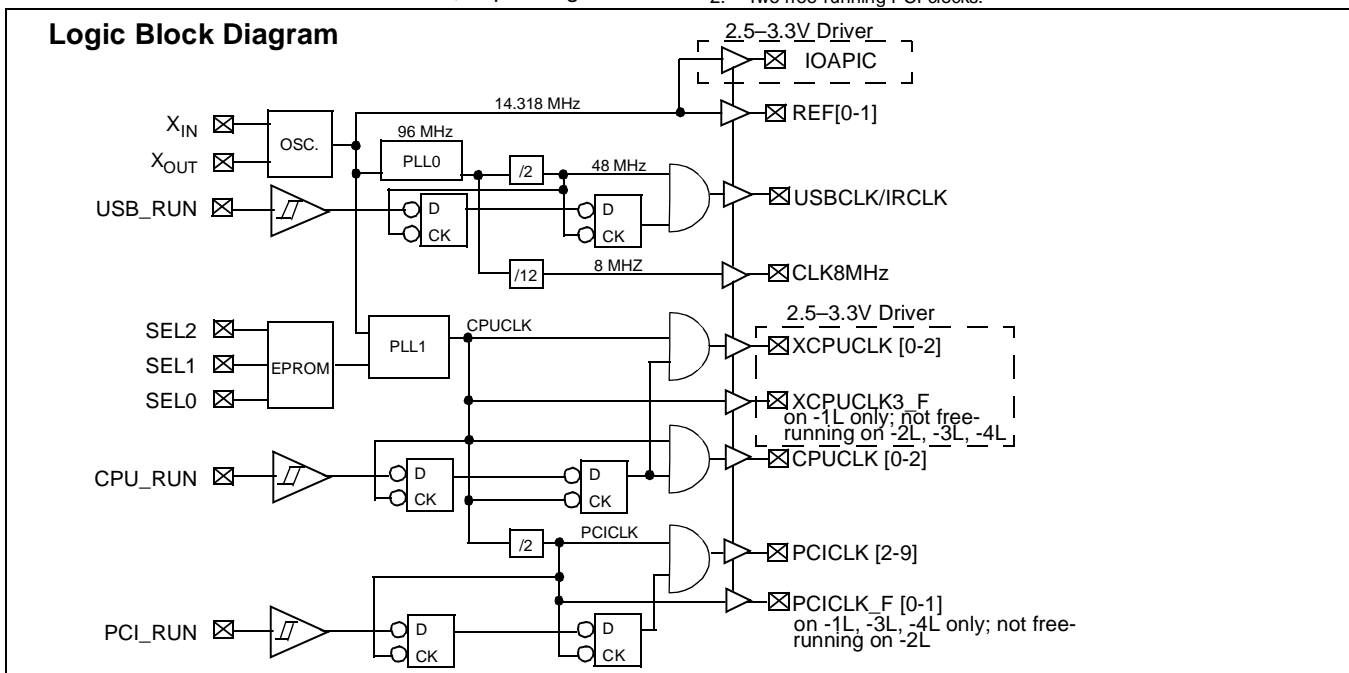
The CY2278A outputs are designed for low EMI emissions. Controlled rise and fall times, unique output driver circuits and factory-EPROM programmable output drive and slew-rate enable optimal configurations for EMI control.

## CY2278A Selector Guide

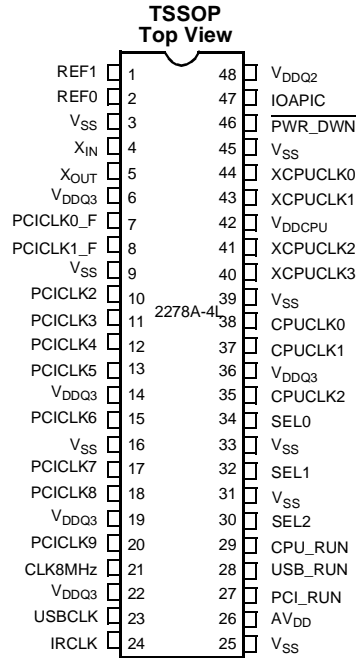
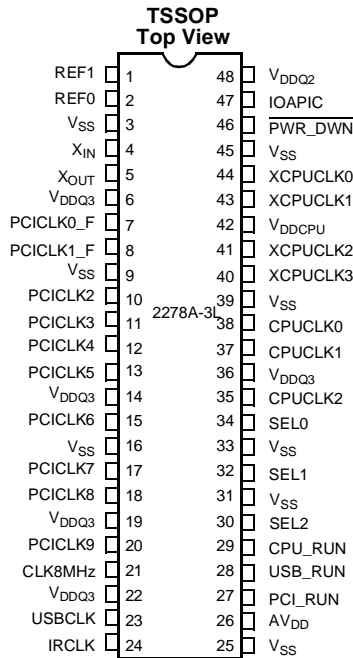
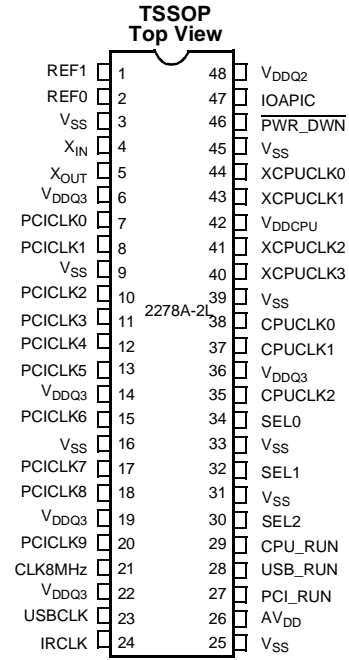
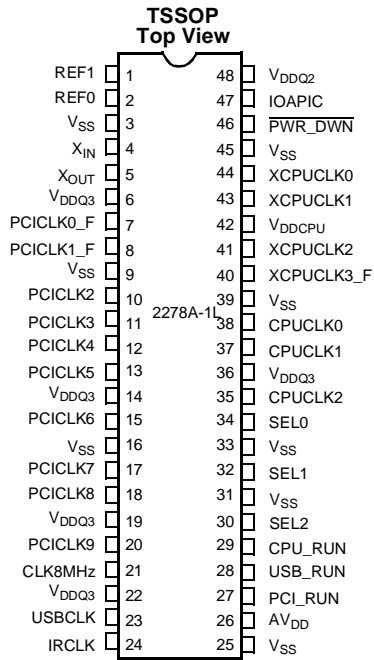
Clock Outputs	-1L	-2L	-3L	-4L
CPU@3.3V	3	3	3	3
CPU@2.5/3.3V	4 <sup>[1]</sup>	4	4	4
PCI (CPU/2MHz)	10 <sup>[2]</sup>	10	10 <sup>[2]</sup>	10 <sup>[2]</sup>
USB/IR (48MHz)	2	2	2	2
KB (8MHz)	1	1	1	1
IOAPIC (14.318 MHz)	2	2	2	2
Ref (14.318MHz)	2	2	2	2
CPU-PCI delay	0 ns	0 ns	1–5 ns	0 ns

### Notes:

1. One free-running CPU clock.
2. Two free-running PCI clocks.



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**Pin Configurations**


**Pin Summary**

Name	Pins	Description
V <sub>DDQ3</sub>	6, 14, 19, 22, 36	3.3V Digital voltage supply
V <sub>DDQ2</sub>	48	IOAPIC Digital voltage supply, 2.5V
V <sub>DDCPU</sub>	42	CPU Digital voltage supply, 2.5V or 3.3V
A <sub>V</sub> DD	26	Analog voltage supply, 3.3V
V <sub>SS</sub>	3, 9, 16, 25, 31, 33, 39, 45	Ground
XTALIN <sup>[3]</sup>	4	Reference crystal input
XTALOUT <sup>[3]</sup>	5	Reference crystal feedback
SEL2	30	CPU clock frequency select input, bit 2
SEL1	32	CPU clock frequency select input, bit 1
SEL0	34	CPU clock frequency select input, bit 0
PCI_RUN	27	Control input, stops all PCI clocks except PCICLK_F when driven LOW
USB_RUN	28	Control input, stops all USB/IR clocks when driven LOW
CPU_RUN	29	Control input, stops all CPU clocks except XCPUCLK_F when driven LOW
PWR_DWN	46	Power down input, shuts down device when driven LOW
XCPUCLK[0:2]	44, 43, 41	2.5V or 3.3V CPU clock outputs
XCPUCLK3_F	40	2.5V or 3.3V CPU clock output, free-running on CY2278A-1L only. This output is not free-running on the -2L, -3L, -4L configurations.
CPUCLK[0:2]	38, 37, 35	3.3V CPU clock output
PCICLK[2:9]	10, 11, 12, 13, 15, 17, 18, 20	PCI clock outputs
PCICLK_F[0:1]	7, 8	PCI clock outputs, free-running on CY2278A-1L, -3L, -4L only. This output is not free-running on the -2L configuration
CLK8MHZ	21	8-MHz Keyboard clock output
IOAPIC	47	IOAPIC clock output
REF[0:1]	2, 1	Reference clock outputs, 14.318 MHz. REF0 has high drive
USBCLK/IRCLK	23, 24	USB or IR clock outputs, 48 MHz

**Note:**

- For best accuracy, use a parallel-resonant crystal, C<sub>LOAD</sub> = 18 pF.

**Function Table**

SEL2	SEL1	SEL0	XTALIN	CPUCLK	PCICLK	REF IOAPIC	USBCLK IRCLK	CLK8MHZ
0	0	0	14.318 MHz	75.0 MHz	37.5 MHz	14.318 MHz	48.0 MHz	8.0 MHz
0	0	1	14.318 MHz	20.0 MHz	10.0 MHz	14.318 MHz	48.0 MHz	8.0 MHz
0	1	0	14.318 MHz	25 MHz	12.5 MHz	14.318 MHz	48.0 MHz	8.0 MHz
0	1	1	14.318 MHz	33.33 MHz	16.67 MHz	14.318 MHz	48.0 MHz	8.0 MHz
1	0	0	14.318 MHz	50.0 MHz	25.0 MHz	14.318 MHz	48.0 MHz	8.0 MHz
1	0	1	14.318 MHz	60.0 MHz	30.0 MHz	14.318 MHz	48.0 MHz	8.0 MHz
1	1	0	14.318 MHz	66.67 MHz	33.33 MHz	14.318 MHz	48.0 MHz	8.0 MHz
1	1	1	14.318 MHz	40.0 MHz	20.0 MHz	14.318 MHz	48.0 MHz	8.0 MHz

**Actual Clock Frequency Values**

Clock Output	Target Frequency (MHz)	Actual Frequency (MHz)	PPM
CPUCLK(0,0,0)	75.0 MHz	75.0	0
CPUCLK(0,0,1)	20.0 MHz	19.979	-1057
CPUCLK(0,1,0)	25 MHz	24.974	-1057
CPUCLK(0,1,1)	33.33 MHz	33.298	-1107
CPUCLK(1,0,0)	50.0 MHz	49.947	-1057
CPUCLK(1,0,1)	60.0 MHz	60.0	0
CPUCLK(1,1,0)	66.67 MHz	66.654	-171
CPUCLK(1,1,1)	40.0 MHz	39.992	-196
USBCLK <sup>[4]</sup>	48.0	48.008	167
CLK8MHz	8.0	8.001	167

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage ..... -0.5 to +7.0V

Input Voltage ..... -0.5V to  $V_{DD}+0.5$

Storage Temperature (Non-Condensing) ... -65°C to +150°C

Max. Soldering Temperature (10 sec) ..... +260°C

Junction Temperature ..... +150°C

Package Power Dissipation ..... 1W

Static Discharge Voltage ..... >2000V  
(per MIL-STD-883, Method 3015, like  $V_{DD}$  pins tied together)

**Operating Conditions<sup>[5]</sup>**

Parameter	Description	Min.	Max.	Unit
$AV_{DD}, V_{DDQ3}$	Analog and Digital Supply Voltage	3.135	3.465	V
$V_{DDCPU}, V_{DDQ2}$	CPU and IOAPIC Supply Voltage	2.375	2.625	V
$T_A$	Operating Temperature, Ambient	0	70	°C
$C_L$	Max. Capacitive Load on XCPUCLK, CPUCLK, USBCLK/IRCLK, CLK8MHZ, REF1, IOAPIC PCICLK REF0		20 20 30 45	pF
$f_{(REF)}$	Reference Frequency, Oscillator Nominal Value	14.318	14.318	MHz

**Notes:**

4. Meets Intel USB clock requirements.
5. Electrical parameters are guaranteed with these operating conditions.

**Electrical Characteristics**

Parameter	Description	Test Conditions		Min.	Max.	Unit
$V_{IH}$	High-level Input Voltage	Except Crystal Inputs <sup>[6]</sup>		2.0		V
$V_{IL}$	Low-level Input Voltage	Except Crystal Inputs <sup>[6]</sup>			0.8	V
$V_{OH}$	High-level Output Voltage	$V_{DDCPU}, V_{DDQ2} = 2.375V$	$I_{OH} = 9\text{ mA}$ XCPUCLK	2.0		V
			$I_{OH} = 13\text{ mA}$ IOAPIC			
$V_{OL}$	Low-level Output Voltage	$V_{DDCPU}, V_{DDQ2} = 2.375V$	$I_{OL} = 13\text{ mA}$ XCPUCLK		0.4	V
			$I_{OL} = 18\text{ mA}$ IOAPIC			

**Electrical Characteristics**

Parameter	Description	Test Conditions		Min.	Max.	Unit	
V <sub>OH</sub>	High-level Output Voltage	V <sub>DDQ3</sub> , AV <sub>DD</sub> , V <sub>DDCPU</sub> = 3.135V	I <sub>OH</sub> = 23 mA	XCPUCLK	2.4		V
			I <sub>OH</sub> = 23 mA	CPUCLK			
			I <sub>OH</sub> = 23 mA	PCICLK			
			I <sub>OH</sub> = 23 mA	USBCLK			
			I <sub>OH</sub> = 23 mA	CLK8MHZ			
			I <sub>OH</sub> = 23 mA	REF0			
			I <sub>OH</sub> = 23 mA	REF1			
V <sub>OL</sub>	Low-level Output Voltage	V <sub>DDQ3</sub> , AV <sub>DD</sub> , V <sub>DDCPU</sub> = 3.135V	I <sub>OL</sub> = 17 mA	XCPUCLK		0.4	V
			I <sub>OL</sub> = 17 mA	CPUCLK			
			I <sub>OL</sub> = 17 mA	PCICLK			
			I <sub>OL</sub> = 17 mA	USBCLK			
			I <sub>OL</sub> = 17 mA	CLK8MHZ			
			I <sub>OL</sub> = 17 mA	REF0			
			I <sub>OL</sub> = 17 mA	REF1			
I <sub>IH</sub>	Input High Current	V <sub>IH</sub> = V <sub>DD</sub>		-10	+10	μA	
I <sub>IL</sub>	Input Low Current	V <sub>IL</sub> = 0V			10	μA	
I <sub>DD</sub>	Power Supply Current <sup>[7]</sup>	V <sub>DDQ3</sub> = 3.465V, V <sub>IN</sub> = 0 or V <sub>DD</sub> , Loaded Outputs, CPU clocks = 66.67 MHz			200	mA	
I <sub>DD</sub>	Power Supply Current <sup>[7]</sup>	V <sub>DDQ3</sub> = 3.465V, V <sub>IN</sub> = 0 or V <sub>DD</sub> , Unloaded Outputs			100	mA	
I <sub>DDS</sub>	Power-down Current	Current draw in power-down state			150	μA	

**Notes:**

6. Crystal inputs have CMOS thresholds.
7. Power supply current will vary with number of outputs which are running. Therefore, power supply current can be calculated with the following formula: to be determined.

**Switching Characteristics<sup>[8]</sup>**

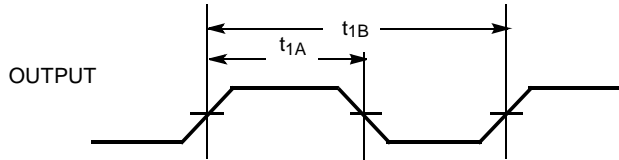
Parameter	Output	Description	Test Conditions	Min.	Typ.	Max.	Unit
t <sub>1</sub>	All	Output Duty Cycle <sup>[9]</sup>	t <sub>1</sub> = t <sub>1A</sub> ÷ t <sub>1B</sub>	45	50	55	%
t <sub>2</sub>	XCPUCLK	XCPU Clock Rising and Falling Edge Rate	Between 0.4V and 2.0V for 2.5V clocks	0.6		4.0	V/ns
t <sub>2</sub>	CPUCLK, IOAPIC	CPU and IOAPIC Clock Rising and Falling Edge Rate	Between 0.4V and 2.0V for 2.5V clocks Between 0.4V and 2.4V for 3.3V clocks	0.8		4.0	V/ns
t <sub>2</sub>	PCICLK	PCI Clock Rising and Falling Edge Rate	Between 0.4V and 2.4V	0.75		4.0	V/ns
t <sub>2</sub>	USBCLK, CLK8MHZ	USB, CLK8MHZ Clock Rising and Falling Edge Rate	Between 0.4V and 2.4V	0.8		4.0	V/ns
t <sub>2</sub>	REF0	REF0 Clock Rising and Falling Edge Rate	Between 0.4V and 2.4V	0.6		4.0	V/ns
t <sub>2</sub>	REF1	REF1 Rising and Falling Edge Rate	Between 0.4V and 2.4V	0.5		2.0	V/ns
t <sub>3</sub>	XCPUCLK	XCPU Clock Rise Time	Between 0.4V and 2.0V	0.4		2.67	ns
t <sub>3</sub>	CPUCLK IOAPIC	CPU and IOAPIC Clock Rise Time	Between 0.4V and 2.4V for 3.3V clocks Between 0.4V and 2.0V for 2.5V clocks	0.5 0.4		2.5 2.0	ns
t <sub>3</sub>	PCICLK	PCI Clock Rise Time	Between 0.4V and 2.4V	0.5		2.67	ns
t <sub>3</sub>	USBCLK, CLK8MHZ	USB Clock and CLK8MHZ Rise Time	Between 0.4V and 2.4V			2.5	ns
t <sub>4</sub>	XCPUCLK	XCPU Clock Fall Time	Between 2.0V and 0.4V	0.4		2.67	ns
t <sub>4</sub>	CPUCLK, IOAPIC	CPU and IOAPIC Clock Fall Time	Between 2.4V and 0.4V for 3.3V clocks Between 2.0V and 0.4V for 2.5V clocks	0.5 0.4		2.5 2.0	ns
t <sub>4</sub>	PCICLK	PCI Clock Fall Time	Between 2.4V and 0.4V	0.5		2.67	ns
t <sub>4</sub>	USBCLK, CLK8MHZ	USB Clock and I/O Clock Fall Time	Between 2.4V and 0.4V			2.5	ns
t <sub>5</sub>	XCPUCLK, CPUCLK	XCPU-XCPU Clock Skew CPU-CPU Clock Skew	Measured at 1.25V for 2.5V clocks Measured at 1.5V for 3.3V clocks		100	300 250	ps
t <sub>5</sub>	PCICLK	PCI-PCI Clock Skew	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks			500	ps
t <sub>6</sub>	XCPUCLK, PCICLK	XCPU-PCI Clock Skew	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks (-1L, -2L, -4L configurations)			500	ps
t <sub>6</sub>	XCPUCLK, PCICLK	XCPU-PCI Clock Skew	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks (-3L configuration)	1	3	5	ns
t <sub>7</sub>	XCPUCLK, CPUCLK	CPU-XCPU Clock Skew	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks			750	ps
t <sub>8</sub>	XCPUCLK, CPUCLK	Cycle-Cycle Clock Jitter <sup>[10]</sup>	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks			400	ps
t <sub>8</sub>	USBCLK, PCICLK	Cycle-Cycle Clock Jitter	Measured at 1.5V			500	ps
t <sub>8</sub>	CLK8MHZ	Cycle-Cycle Clock Jitter	Measured at 1.5V			650	ps
t <sub>9</sub>	XCPUCLK, PCICLK, CPUCLK	Power-up Time	CPU, PCI clock stabilization from power-up			3	ms

**Notes:**

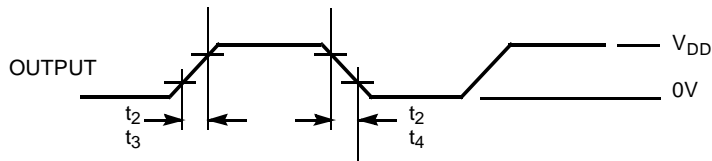
8. All parameters specified with loaded outputs;SEL[2:0]=110.
9. Duty cycle is measured at 1.5V when V<sub>DD</sub> = 3.3V. When V<sub>DDCPU</sub> = 2.5V, CPUCLK duty cycle is measured at 1.25V.
10. Room Temperature.

## Switching Waveforms

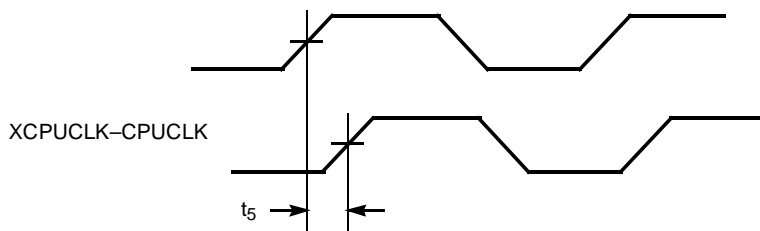
### Duty Cycle Timing



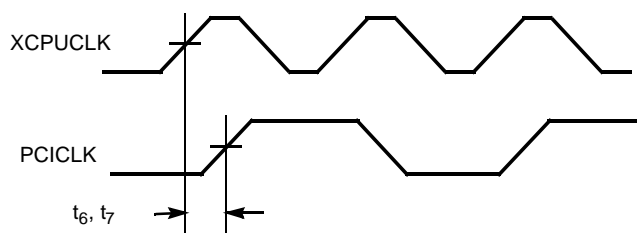
### All Outputs Rise/Fall Time

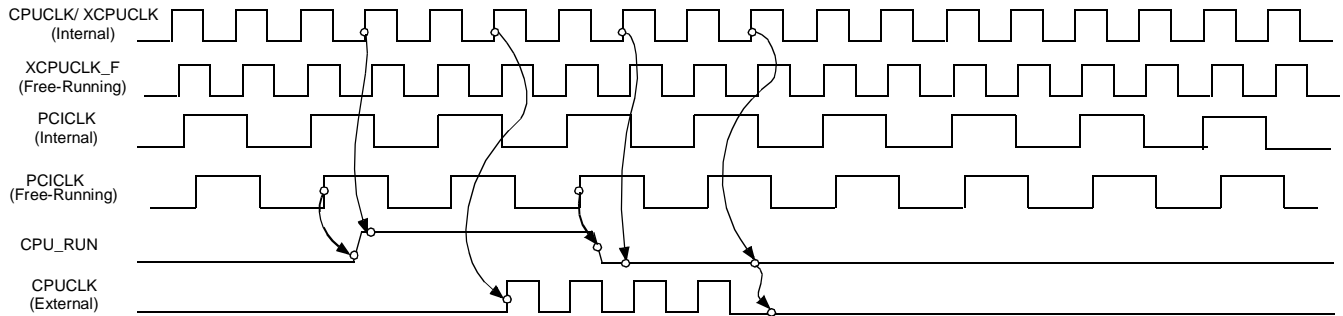
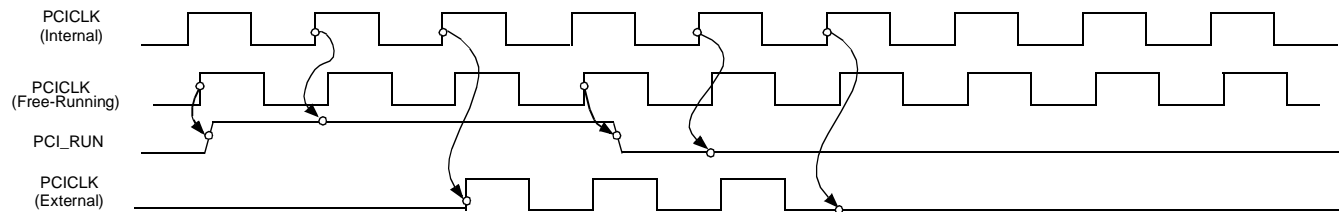
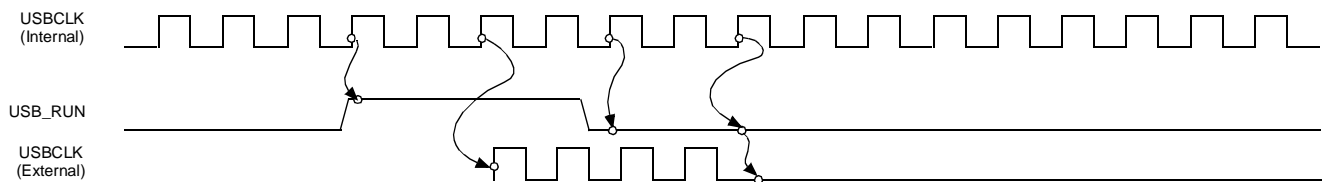
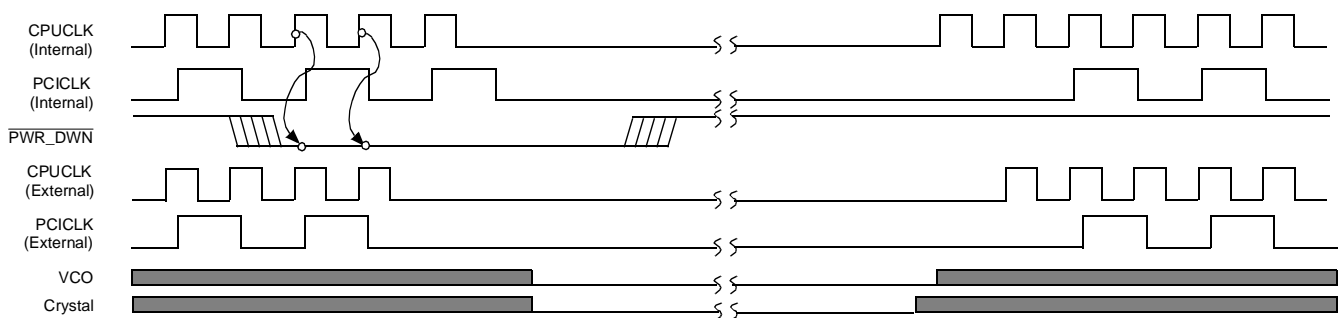


### XCPU-CPU Clock Skew



### XCPU-PCI Clock Skew



**Switching Waveforms (continued)**
**CPU\_RUN Timing<sup>[11, 12]</sup>**

**PCI\_RUN Timing<sup>[13, 14]</sup>**

**USB\_RUN Timing<sup>[15]</sup>**

**PWR\_DWN Timing**


Shaded section on the VCO and Crystal waveforms indicates that the VCO and crystal oscillator are active, and there is a valid clock.

**Notes:**

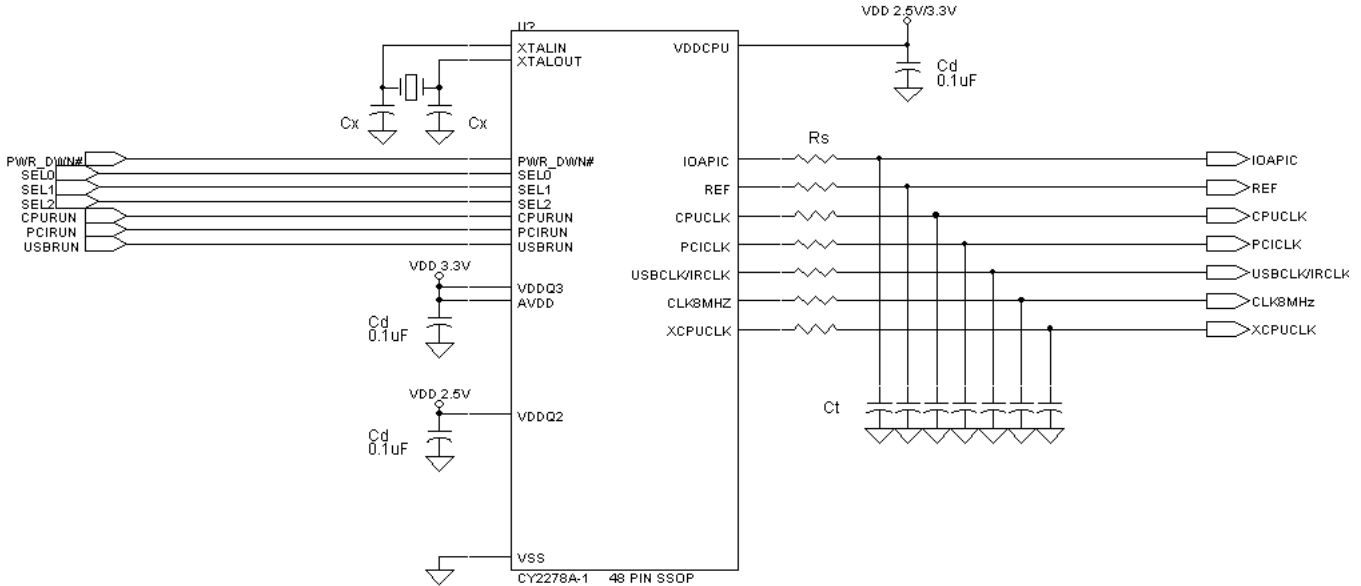
11. CPUCLK on and CPUCLK off latency is 2 or 3 external CPUCLK cycles.
12. CPU\_RUN may be applied asynchronously. It is synchronized internally.
13. PCICLK on and PCICLK off latency is 1 rising edge of the external PCICLK.
14. PCI\_RUN may be applied asynchronously. It is synchronized internally.
15. USBCLK on and USBCLK off latency is 2 USBCLK cycles.



## Application Information

Clock traces must be terminated with either series or parallel termination, as they are normally done.

## Application Circuit



Cd = DECOUPLING CAPACITORS

Ct = OPTIONAL EMI-REDUCING CAPACITORS

Cx = OPTIONAL LOAD MATCHING CAPACITOR

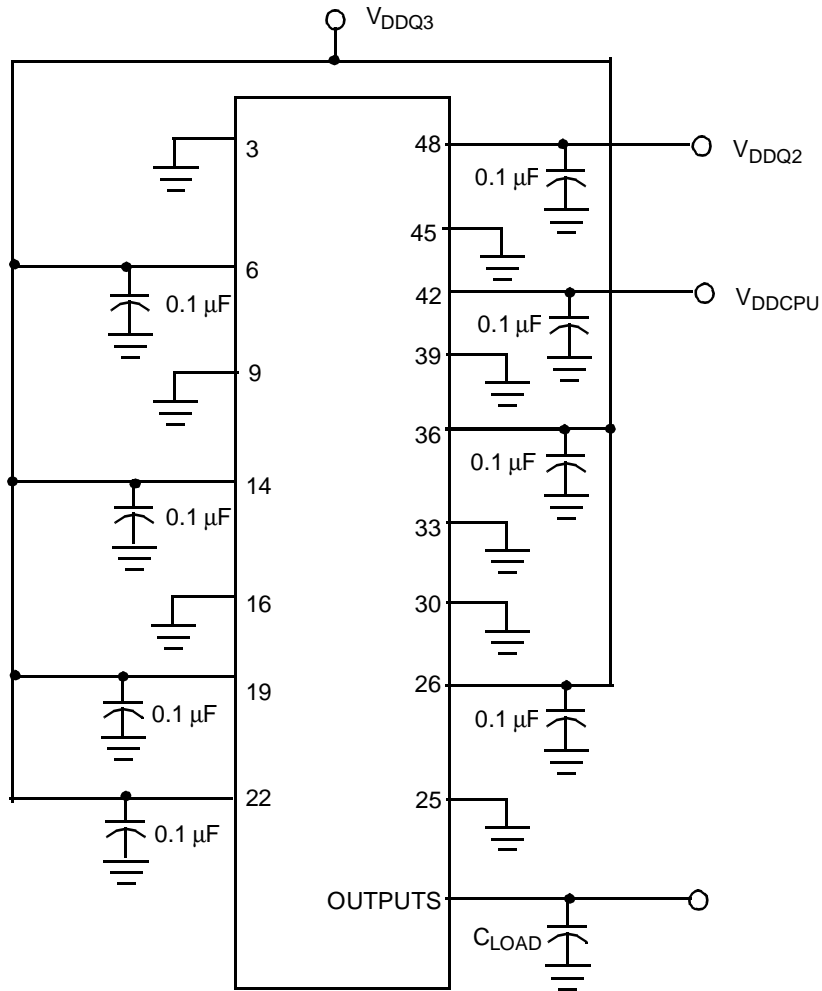
Rs = SERIES TERMINATING RESISTORS

## Summary

- A parallel-resonant crystal should be used as the reference to the clock generator. The operating frequency and  $C_{LOAD}$  of this crystal should be as specified in the data sheet. Optional trimming capacitors may be needed if a crystal with a different  $C_{LOAD}$  is used. Footprints must be laid out for flexibility.
- Surface mount, low-ESR, ceramic capacitors should be used for filtering. Typically, these capacitors have a value of 0.1  $\mu$ F. In some cases, smaller value capacitors may be required.
- The value of the series terminating resistor satisfies the following equation, where  $R_{trace}$  is the loaded characteristic impedance of the trace,  $R_{out}$  is the output impedance of the clock generator (specified in the data sheet), and  $R_{series}$  is the series terminating resistor.

$$R_{series} \geq R_{trace} - R_{out}$$

- Footprints must be laid out for optional EMI-reducing capacitors, which should be placed as close to the terminating resistor as is physically possible. Typical values of these capacitors range from 4.7 pF to 22 pF.
- A Ferrite Bead may be used to isolate the Board  $V_{DD}$  from the clock generator  $V_{DD}$  island. Ensure that the Ferrite Bead offers greater than 50 $\Omega$  impedance at the clock frequency, under loaded DC conditions. Please refer to the application note "Layout and Termination Techniques for Cypress Clock Generators" for more details.
- If a Ferrite Bead is used, a 10  $\mu$ F– 22  $\mu$ F tantalum bypass capacitor should be placed close to the Ferrite Bead. This capacitor prevents power supply droop during current surges.

**Test Circuit**


Note: All capacitors should be placed as close to each pin as possible.

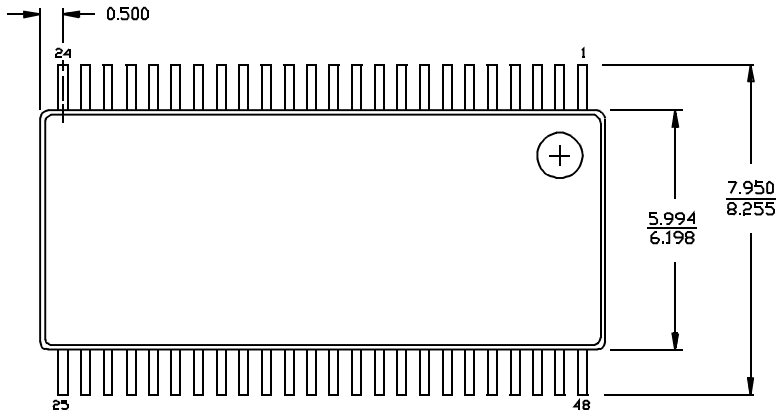
**Ordering Information**

Ordering Code	Package Name	Package Type	Operating Range
CY2278APAC-1L	Z48	48-Pin TSSOP	Commercial
CY2278APAC-2L	Z48	48-Pin TSSOP	Commercial
CY2278APAC-3L	Z48	48-Pin TSSOP	Commercial
CY2278APAC-4L	Z48	48-Pin TSSOP	Commercial

Document #: 38-00619-D

Package Diagram

48-Lead Thin Shrunken Small Outline Package Z48



DIMENSIONS IN MM MIN.  
MAX.

