AT83C5103 / AT87C5103
C51 LPC 8-Bit Microcontroller

ATMEL P/N : AT8xC5103xxx-IBRAL

PPAP Submission

Date: March 2003

Supplier: ATMEL-NANTES SA

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Revision history

Rev	Issue	Modification Notice	Applicable from
0	January 2003	Initial version	
1	March 2003	Update after product characterization completion (3V and 5V ranges)	

PPAP Checklist

Requirements	Included
Table of contents	yes
PPAP Checklist	yes
1. Design Records	yes
2. Engineering Change Documents	yes
3. Engineering Approval	yes
4. Design FMEA	Project Risk analysis
5. Process Flow Diagrams	yes
6. Process FMEA	yes
7. Dimensional Results	Not Applicable
8. Records of Material / Performance Test Results 8.1 Material Test Records 8.2 Performance Test Records	 Not applicable to IC yes
9. Initial Process Study	yes
10. Measurement System Analysis Study	yes
11. Qualified Laboratory Documentation	yes
12. Control Plan	yes
13. Part Submission Warrant (PSW)	yes
14. Appearance Approval Report	Not applicable to IC
15. Bulk Material Requirements Checklist	Not applicable to IC
16. Sample Production Parts	Separate order
17. Master Sample	Not attached
18. Checking Aids	Not Applicable
19. Customer Specific Requirements	Not defined

1 Design Records

1.1 Product Specification

Please see ATMEL's Data Sheet AT83C5103 / AT87C5103 Low-Pin-Count 8-Bit Microcontroller
http://www.atmel.com/

1.2 Package Outline

See attached file : SSOP16_outline.pdf

2 Engineering Change Documents

2.1 CDC Certificate of Design, Construction and Qualification

2.1.1 General Product Information

Product Name:	AT87C5103: 16k EPROM AT83C5103: 16k ROM
Function:	8 Bits Microcontroller, 16Kbytes memory
Wafer Process:	CMOS 0.5um
Package Type :	SSOP 16

Locations:

Process Development,	ATMEL Nantes , France
Product Development	ATMEL Nantes , France
Wafer Plant	ATMEL Nantes , France
QC Responsibility	ATMEL Nantes, France
Probe Test	ATMEL Nantes , France
Assembly	AMKOR Philippines
Final Test	TSTI Philippines
Lot Release	ATMEL Nantes, France
Shipment Control	Global Logistic Center, Philippines
Quality Assurance	ATMEL Nantes, France
Reliability Testing	ATMEL Nantes, France
Failure Analysis	ATMEL Nantes, France

2.1.2 Process Technology Information

Process Type (Name):	Z94 (SCMOS3 Non Volatile - EPROM) Z92 (SCMOS3 - ROM)
Base Material:	Epi (Z94) Bulk (Z92)
Wafer Thickness (final)	475µm
Wafer Diameter	150 mm
Number Of Masks	Z94: 22 Z92: 14
Gate Oxide (Logic transistors)	
Material	Silicon Dioxide
Thickness	110 A
Gate Oxide (EPROM cell)	
Material	Silicon Dioxide
Thickness	110 A
Polysilicon	
Number of Layers	Z94:2 Z92:1
Thickness Poly 1	2000A
Thickness Poly 2	3000A
Metal	
Number of Layers	3
Material:	AlCu
Layer 1 Thickness	5150A
Layer 2 Thickness	5150A
Layer 3 Thickness	7650A
Passivation	
Material	Z94: SiO2 / Oxynitride Z92: SiO2 / Nitride
Thickness	Z94: 3000A / 15000A Z92: 2600A / 6400A

2.2 Product Design

2.2.1 Product Design Information

Die Size	3500µm * 3090µm (10.82mm2)
Pad Size Opening	80µm * 80µm
Logic Effective Channel Length	0.5µm
Gate Poly Width (min.)	0.50µm
Gate Poly Spacing (min.)	0.60µm
Metal 1 Width	0.60µm
Metal 1 Spacing	0.70µm
Metal 2 Width	0.80µm
Metal 2 Spacing	0.70µm
Metal 3 Width	0.80µm
Metal 3 Spacing	0.70µm
Contact size	0.60µm
Via 1 size	0.60µm
Via 2 size	0.60µm

2.2.2 Package Technology Information

Package weight	0.14 g
Chip separation method	Sawing
Lead frame	
Material	Cu
Thickness	6 mils
Lead plating	Electroplated Sn/Pb 85/15
Die attach	
Material	Silver epoxy
Type	Ablestick 84-1 LMISR4
Wire bonding	
Material	Au
Diameter	1.0 mil
Method	Thermosonic
Molding	
Material	MP8000AN
Flammability rating	UL94V-0
Marking	
Method	Top : Printed ink Back : Laser

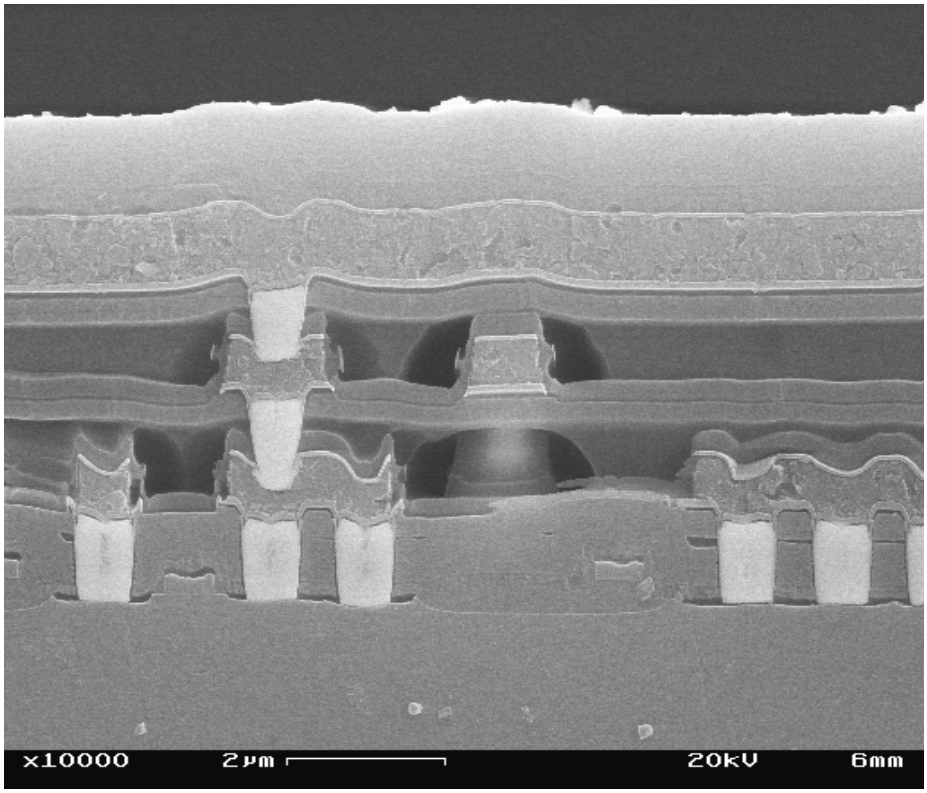
2.2.3 Packing Delivery Information

Dry packing	No
Tube packed	
Primary	Tube
Material	Antistatic PVC
Number per unit	77
Secondary	Box
Material	Cardboard
Number per unit	385
Labelling (minimum)	Device type, quantity, Date code, Production code
Bar coding	Code 39 to EIA-556-A
Reel packed	
Primary	Reel
Material	
Carrier tape	Conductive black polystyrene
Cover tape	Antistatic film
Number per unit	2000
Secondary	Box
Number per unit	1
Labelling (minimum)	Device type, quantity, Date code, Production code

2.2.4 Final Test Information

Probe equipment	Maverick GT or PT
Probe temperature	125° C
Test equipment	Maverick GT or PT
Test temperature	- 40° C + 125° C + 25° C

2.2.5 Device Cross Section



2.3 Qualification and Change Procedure

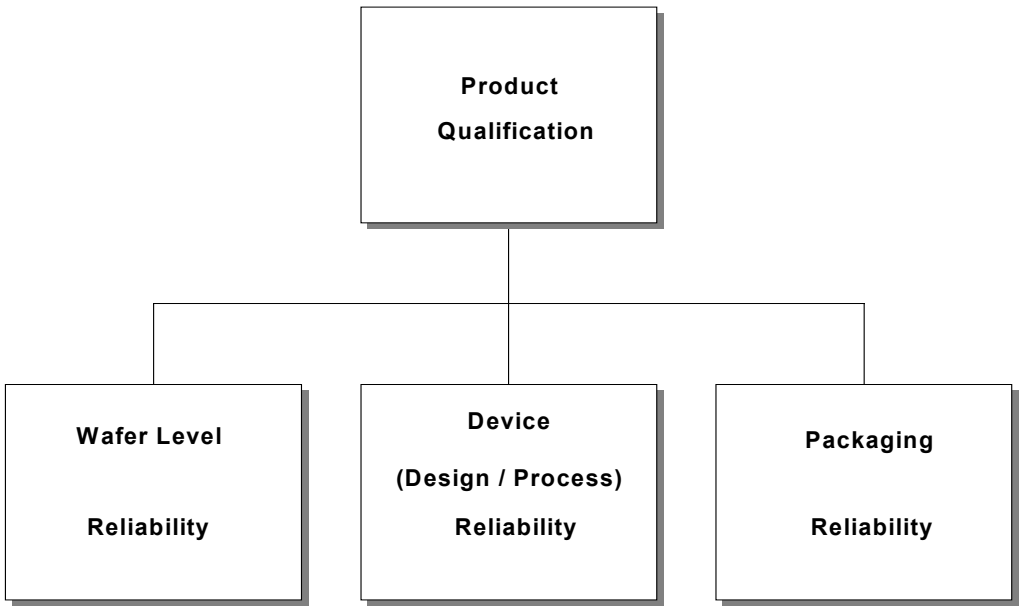
2.3.1 Qualification methodology

All product qualifications are split into three distinct steps as shown below. Before a product is released for use, successful qualification testing are required at wafer, device and package level.

- Wafer Level Reliability consists in testing individually basic process modules regarding their well known potential limitations (Electromigration, Hot Carriers Injection, Oxide Breakdown, NVM Data Retention). Each test is performed using wafer process specific structures.

- Device reliability is covering either dice design and processing aspects. The tests are performed on device under qualification, but generic data may also be considered for reliability calculation.

- For each package type proposed in the Datasheet, it is verified that qualification data are available. If not qualification tests are carried out for the new package types. In addition, one package type is selected to verify packaging reliability of the device under qualification.



2.3.2 Change Procedure

All changes are controlled by ECN (Engineering Change Notice). All major changes are notified to the customers using products that are affected by the change.

A major change is defined as a change which affects the electrical and/or mechanical specification as defined in the datasheet or which affects the following parameters as defined hereafter:

1	**General Major Changes**
1-1	Manufacturing line
1-2	Sequence of fabrication process cycle
1-3	Material type
1-4	Electrical parameter
1-5	External physical dimension
1-6	Die size

2	**Changes specific to wafer fabrication area**
2-1	Doping method
2-2	Gate oxide formation method
2-3	Equipment change
2-4	Layer Thickness
2-5	Module dimensions

3	**Changes specific to assembly process area**
3-1	Sawing method
3-2	Die attach
3-3	Wire interconnect tools
3-4	Molding process
3-5	Tinning method

4	**Changes specific to test area**
4-1	Specification limit
4-2	Test coverage reduction
4-2	Product identification
4-3	Final conditioning

2.3.3 Qualification test methods

General Requirements for Plastic packaged CMOS Ics.

Standard	Test Description	Acceptance
MIL-STD 883 Method 1005	**Electrical Life Test (Early Failure Rate)** 48 hours 140°C	0/300 - 48h
MIL-STD 883 Method 1005	**Electrical Life Test (Latent Failure Rate)** 1000 hours 140°C Dynamic or Static	0/100 - 500h
MIL-STD 883 Method 3015.7	**Electrostatic Discharge HBM** +/-2000v 1.5kOhm/100pF/3 pulses	0/3 per level
JEDEC 78	**Latch up** 50mW power injection, 50% overvoltage @125°C	0/5 per stress
AEC Q100 Method 005	**NVM Endurance** Program Erase Cycles 25°C	0/50 - 100kc
AEC Q100 Method 005	**NVM Data Retention** High Temperature Storage 165°C	0/50 - 500h
MIL-STD 883 Method 1010	**Temperature Cycling** 1000 cycles -65°C/150°C air/air	0/50 - 500c
Atmel PAQA0184	**HAST after Preconditioning** 144 hours 130°C/85%RH	0/50 - 72h
EIA JESD22-A101	**85/85 Humidity Test** 1000 hours 85°C/85%RH	0/50 - 500h
EIA JESD22-A110	**HAST** 336 hours 130°C/85%RH/5.5V	0/50 - 168h
EIA JEDEC 20-STD	**Preconditioning** Soldering Stress 220°C/235°c/3 times	0/11 per class
MIL-STD 883 Method 2003	**Solderability**	0/3
MIL-STD 883 Method 2015	**Marking Permanency**	0/5

3 Engineering Approval

AT8xC5103 is qualified since January 2003

Released to production is planned on February 2003

Release to Production loop approval is the following :

- Head of Technical Center
- Technical Project Leader
- Project Manager
- Product Engineering
- Operation Backend
- Operation Frontend
- Quality Management
- Marketing
- Business Planning
- Test Development

4 Design FMEA

For new products, a Project Risk Analysis is performed during Feasibility phase under the Project Leader responsibility, using expertise in many areas including Design.

This Project Risk Analysis and related Action Plan to reduce the risks are reviewed at each milestone of the project.

The Project Risk Analysis report is an ATMEL internal document .

5 Process Flow Diagrams

5.1 Frontend

1. Incoming inspection of silicon wafers.
2. PBL (Z94) or Locos (Z92) Isolation.
3. Non Volatile Well Implants (Z94).
4. MOS N-Well implants (Z94 & Z92) and N Well diffusion. (Z92)
5. EPROM floating Gate oxidation and Poly deposition (Z94).
6. EPROM ONO stack oxidation (Z94).
7. HVMOS gate oxidation (Z94)
8. MOS P-Well Implants (Z94 & Z92).
9. Depleted MOS Well Implants (Z94).
10. MOS definition (Z94).
11. MOS Gate oxidation (Z94 & Z92).
12. Polysilicon deposition and MOS gate definition(Z94 & Z92).
13. EPROM control gate definition (Z94) and EPROM Implants (Z94).

14. MOS / HVMOS Implants with Spacer definition. (Z94 & Z92)
15. Silicide Hard mask definition.(Z94 & Z92)
16. Salicide module. (Z94 & Z92)
17. ILD deposition and SOG planarization (Z94 & Z92)
18. Contact etching and Plug1 filling. (Z94 & Z92)
19. Metal 1 deposition and etching (Z94 & Z92)
20. IMD1 and REB planarization (Z94 & Z92)
21. Via1 etching and Plug2 filling (Z94 & Z92)
22. Metal 2 deposition and etching (Z94 & Z92)
23. IMD2 and REB planarization (Z94 & Z92)
24. Via2 etching and Plug3 filling (Z94 & Z92)
25. Metal 3 deposition and etching (Z94 & Z92)
26. Passivation deposition and etching (Z94 & Z92)
27. UV erasing (Z94)
28. Test site (Z94 & Z92)
29. Wafer sort1 (Z94 & Z92)
30. Bake (Z94)
31. Wafer sort2 (Z94)

5.2 Assembly

Referenced Process Flow Chart : Amkor Philippines P470-0501-0204

1. Wafer mount
2. Wafer saw
3. First optical
4. Die bonding
5. Wire bonding
6. Molding
7. Solder plating
8. Top marking
9. Trim and form
10. Final visual inspection

5.3 Test and Packing

1. Room temperature initial test
2. Burn-in
3. Room temperature test
4. Hot test
5. Cold test
6. Final quality checks
7. Packing

6 Process FMEA

Process FMEA for 0.5uM Z92 and Z94 are implemented and are only shown upon request during customer audits.

7 Dimentional Results

Only necessary for new packages and/or new assembly locations/lines
Not necessary for this PPAP, because parts are produced in standard SSOP16 package
Package dimensions were checked during Package Qualification (see chapter 8.1.2 for more details)

8 Performance Test Results

8.1 Qualification Results

8.1.1 Wafer Process Qualification

ATMEL 0.5µm SCMOS3 wafer process is qualified since 1997, september

ATMEL 0.5µm SCMOS3NV wafer process is qualified since 2000, february

8.1.2 Package Qualification

Performed on product G1001 at AMKOR Philippines : QTP 0329 (11/10/1996)

The following table summarizes the SSOP16 package qualification results

Test Description	Step	Result	Comment
Humidity 85°C/85RH	1000H	0/45	
Thermal Cycles – 65°C/100°C	1000C	0/45	
Lead Finish Adhesion		0/3	
Construction Analysis		0/5	AC96009
Marking Permanency		0/5	
IR Reflow mounting	168H	0/45	With preconditionning
Physical Dimentions		0/5	
IR Reflow mounting	168H	0/45	Without preconditionning

Conclusions : No failure was observed during the reliability tests. The qualification of SSOP16L at AMKOR Philippines is pronounced.

8.1.2.1 Product Qualification

8.1.2.2 Device Reliability

The test results are summarized in the table below:

Lot	Device Type	Test Description	Step	Result	Comment
Z42859B	AT83C5103	EFR Dynamic Life Test	12h	0/800	
		LFR Life Test	500h 1000h	0/77 0/77	
Z40807C	TSS463	EFR Dynamic Life Test	12h	1/776	overstress
		LFR Life Test	500h 1000h	0/77 0/77	
Z27921A	TS83C51RX2	EFR Dynamic Life Test	12h	0/297	
		LFR Life Test	500h 1000h	0/100 0/100	
Z27300A	TS83C51RC2	ESD HBM	4000v	0/3	Class 3 of MIL STD 883 Method 3015
		LATCH-UP Power Injection Over-voltage	 50mw 10v	 0/5 0/5	Latch-up free (up to 120mW)

8.1.2.3 Package Reliability

In this section are presented the packaging qualification measurements done on AT83C5103 in SSOP16 .

Lots	Device Type	Test Description	Step	Result	Comment
Z42859B	AT83C5103	85/85 Humidity	500h 1000h	0/77 0/77	After preconditioning level1
		Thermal Cycles	500c 1000c	0/77 0/5 0/5 0/72	After preconditioning level1 Ball shear cpk:1.22 (30 pads) Wire pull cpk:1.39 (30 wires)
		HAST after Soldering Stress	96h	0/77	
		High Temperature Storage 165°C	500h 1000h	0/77 0/77	
		Moisture sensitivity JESD20 – level1	Csam Elect	0/11 0/231	

8.1.2.4 Electrical Distribution in Operating Life-Test

Not available

8.1.2.5 Failure Mechanisms and Corrective Actions

Not applicable

8.1.2.6 ESD Results (HBM) - MIL-STD 883E method 3015.7

Product 87C5103 is classified in **class 1** of the MIL-STD
Product 83C5103 is classified in **class 3** of the MIL-STD

8.1.2.7 Latchup Results

Power Injection	50mw	0/5	Latch-up free (up to 120mW)
Over-voltage	10v	0/5	

8.2 Product Characterization

8.2.1 Characterization environment

Tester: Maverick 2 / ntomv23
Corner lot: Z42859
Process: Z92G - Bulk
ROM Code: 3ZAA
Assy package: 3Z (PDIL24.300)

8.2.2 Corner lot's splits

In order to characterize the product with realistic excursion of the process, corner run splits have been manufactured using :

- Variation onsLeffP and LeffN
- Variations on VTP and VTN

8.2.3 Results / Parameter capability

8.2.3.1 Input Voltages

Symbol	Parameter	Specification	Vcc	Temp	Average	Cpk	Conditions
VIH	Input High Level exept RST & XTAL1	1.89V max	2 .7V	-40°C	1.22V	4.2	
				130°C	1.09V	5.7	
		2.31V max	3 .3V	-40°C	1.42V	4.5	
				130°C	1.29V	5.6	
		2.52V max	3.6V	-40°C	1.5V	5.0	
				130°C	1.39	5.7	
		3.15V max	4.5V	-40°C	1.77V	6.8	
				130°C	1.68V	6.2	
		3.85V max	5.5V	-40°C	2.04V	7.2	
				130°C	2.03V	7.1	
VIH1	Input High Level RST	1.89V max	2.7V	-40°C	0.99V	6.1	
				130°C	0.86V	4.7	
		2.31V max	3.3V	-40°C	1.13V	8.0	
				130°C	0.96V	8.4	
		2.52V max	3.6V	-40°C	1.2V	9.5	
				130°C	1.02V	11 .1	
		3.15V max	4.5V	-40°C	1.41V	11.4	
				130°C	1.22V	12.8	
		3.85V max	5.5V	-40°C	1.64V	13.5	
				130°C	1.44V	19.5	
VIH1	Input High Level XTAL1	1.89V max	2.7V	-40°C	1.41V	8.0	
				130°C	1.45V	6.5	
		2.31V max	3.3V	-40°C	1.75V	7.0	
				130°C	1.79V	6.8	
		2.52V max	3.6V	-40°C	1.93V	6.8	
				130°C	1.97V	6.7	
		3.15V max	4.5V	-40°C	2.45V	6.4	
				130°C	2.5V	6.5	
		3.85V max	5.5V	-40°C	3.06V	6.2	
				130°C	3.1V	6.0	
VIL	Input Low Level	0.44V min	2.7V	-40°C	1.19V	3.2	
				130°C	1.06V	3.7	
		0.56V min	3.3V	-40°C	1.39V	3.0	
				130°C	1.25V	3.1	
		0.62V min	3.6V	-40°C	1.48V	3.1	
				130°C	1.35V	2.9	
		0.8V min	4.5V	-40°C	1.75V	2.9	
				130°C	1.62V	2.3	
		1.0V min	5.5V	-40°C	2.03V	2.1	
				130°C	1.92V	1.8	

8.2.3.2 Output Voltages

Symbol	Parameter	Specification	Vcc	Temp	Average	Cpk	Conditions
VOH_PP	Output High Level in Push-Pull Mode Ports 1 & 4	2.2V min	2.7V	-40°C	2.7V	163	IOH = 0.1 mA
				130°C	2.7V	112	
		4.0V min	4.5V	-40°C	4.5V	138	
				130°C	4.5V	106	
		1.7V min	2.7V	-40°C	2.35V	9.3	IOH = 1mA
				130°C	2.06V	2.5	
		3.5V min	4.5V	-40°C	4.27V	29	
				130°C	4.13V	15	
VOH	Output High Level in Pseudo Bidirectional Mode Ports 1 & 4	4.2V min	4.5V	-40°C	4.41V	14.1	IOH = 10µA
				130°C	4.35V	9.9	
		3.8V min		-40°C	4.25V	15	IOH = 30µA
				130°C	4.08V	7.3	
		3.0V min		-40°C	4.0V	15.6	IOH = 60µA
				130°C	3.6V	5.9	
		2.4V min	2.7V	-40°C	2.57V	9.2	IOH = 10µA
				130°C	2.48V	3	
VOL	Output Low Level Ports 1 & 4	0.3V max	4.5V	-40°C	0.05V	11.4	IOH = 0.1mA
				130°C	0.08V	5.8	
		0.45V max		-40°C	0.35V	2.2	IOH = 1.6mA
				130°C	0.35V	1.9	
		1.0V max		-40°C	0.72V	3.3	IOH = 3.5mA
				130°C	0.70V	3.8	
		0.3V max	2.7V	-40°C	0.05V	11.4	IOH = 0.1mA
				130°C	0.08V	5.7	
		1.0V max		-40°C	0.37V	13.5	IOH = 1.6mA
				130°C	0.39V	10.8	

8.2.3.3 Input currents

Symbol	Parameter	Specification	Vcc	Temp	Average	Cpk	Conditions
IIL	Input Low current in Pseudo Bidirectional Mode	-50µA	3.3V	-40°C	-7µA	26.2	Vin = 0.45V
				130°C	-4µA	56.4	
			3.6V	-40°C	-8.3µA	22.2	
				130°C	-4.9µA	48	
			5.5V	-40°C	-19.7µA	8.8	
				130°C	-11.8µA	21.6	
ITL	Input Transition current in Pseudo Bidirectional Mode	-650µA	3.3V	-40°C	-94.1µA	32.8	VIN = 2V
				130°C	-56.1µA	67.9	
			3.6V	-40°C	-119.4µA	25.2	
				130°C	-71.6µA	52.6	
			5.5V	-40°C	-301.5µA	7.6	
				130°C	-189.8µA	17.8	
ILI_Z	Input Leakage current in Input Mode	10µA	3.3V	-40°C	0.7nA	188.5	VIN = 0V
				130°C	2.7nA	120.9	
			3.6V	-40°C	1.6nA	184.7	
				130°C	3.5nA	118.6	
			5.5V	-40°C	1.1nA	186.3	
				130°C	4.1nA	123	
			3.3V	-40°C	56nA	107.5	VIN = VCC
				130°C	78.4nA	52.6	
			3.6V	-40°C	61.6nA	106.6	
				130°C	68.6nA	48.2	
			5.5V	-40°C	92nA	75.4	
				130°C	48.2nA	27.5	
ILI_OD	Input Leakage current in Open Drain Mode	10µA	3.3V	-40°C	0.1nA	181.9	VIN = 0V
				130°C	3nA	121.7	
			3.6V	-40°C	1.1nA	180.8	
				130°C	3nA	119.4	
			5.5V	-40°C	0.8nA	182.7	
				130°C	2.9nA	125.2	
			3.3V	-40°C	55.8nA	106.9	VIN = VCC
				130°C	81nA	50.3	
			3.6V	-40°C	63nA	101	
				130°C	88.2nA	47.5	
			5.5V	-40°C	92.2nA	71.5	
				130°C	150.6nA	27.4	

8.2.3.4 Pull-Down Resistor on Reset Pin

Symbol	Parameter	Specification	Vcc	Temp	Average	Cpk	Conditions
RPDRST	Pull-Down Reset Resistor	Min = 30Kohms Max = 150Kohms (Rom version only)	2.7V	-40°C	39.4K	4.8	
				130°C	67.7K	7.1	
			3.3V	-40°C	39.7K	4.8	
				130°C	68.1K	7	
			3.6V	-40°C	39.8K	5	
				130°C	68.3K	6.9	
			4.5V	-40°C	40.2K	5.1	
				130°C	68.9K	6.7	
			5.5V	-40°C	40.7K	5.2	
				130°C	69.5K	6.5	

8.2.3.5 Consumptions

Symbol	Parameter	Specification	Vcc	Temp	Average	Cpk	Conditions
IPD	Power-Down current	50µA max	3.3V	130°C	8µA	2.7	See datasheet
			3.6V		9µA	1.8	
		100µA max	5.5V		16µA	2.2	
ICCOP	Operating consumption	14.2mA max	3.3V	-40°C	7.9mA	7.5	16.7Mhz CPU running
				130°C	6.8mA	6.9	
			3.6V	-40°C	8.9mA	6.3	
				130°C	7.7mA	5.7	
		21.5mA max	5.5V	-40°C	15.2mA	5.8	
				130°C	13.9mA	5.1	
ICCIDL	Idle Mode consumption	10.8mA max	3.3V	-40°C	5.5mA	5.9	16.7Mhz Cpu inactive
				130°C	4.8mA	7.7	
			3.6V	-40°C	6.2mA	4.6	
				130°C	5.4mA	6.2	
		18.2mA max	5.5V	-40°C	11.4mA	4.8	
				130°C	9.9mA	6.0	

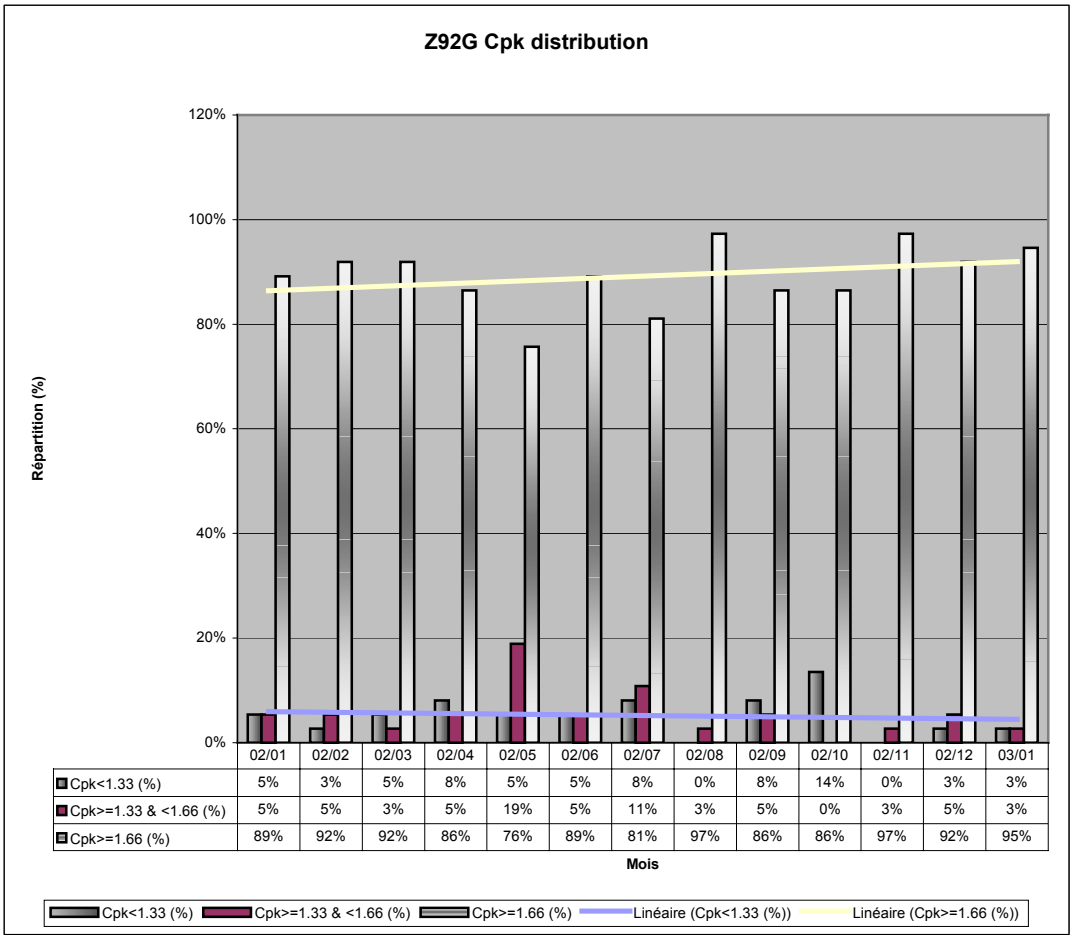
9 Initial Process Study

9.1 SCMOS3 process (Z92G)

Parameters controlled during Electrical Test :

NMOS/PMOS :junction Breakdown Voltage, Threshold voltage, electrical width & length, Thin oxide Breakdown Voltage, Sub-threshold current.
Sheet Resistance : N+, P+, WELL, PolyN, PolyP, Unsalicided Poly
Metal continuity / isolation: metal1, metal2, metal3
Contacts/ Vias1 & Vias2 resistance
Contacts Breakdown Voltage
Salicide isolation

Cpk history (Last update 23/01/2003)



	02/01	02/02	02/03	02/04	02/05	02/06	02/07	02/08	02/09	02/10	02/11	02/12	03/01
Cpk<1.33 (%)	5%	3%	5%	8%	5%	5%	8%	0%	8%	14%	0%	3%	3%
Cpk>=1.33 & <1.66 (%)	5%	5%	3%	5%	19%	5%	11%	3%	5%	0%	3%	5%	3%
Cpk>=1.66 (%)	89%	92%	92%	86%	76%	89%	81%	97%	86%	86%	97%	92%	95%

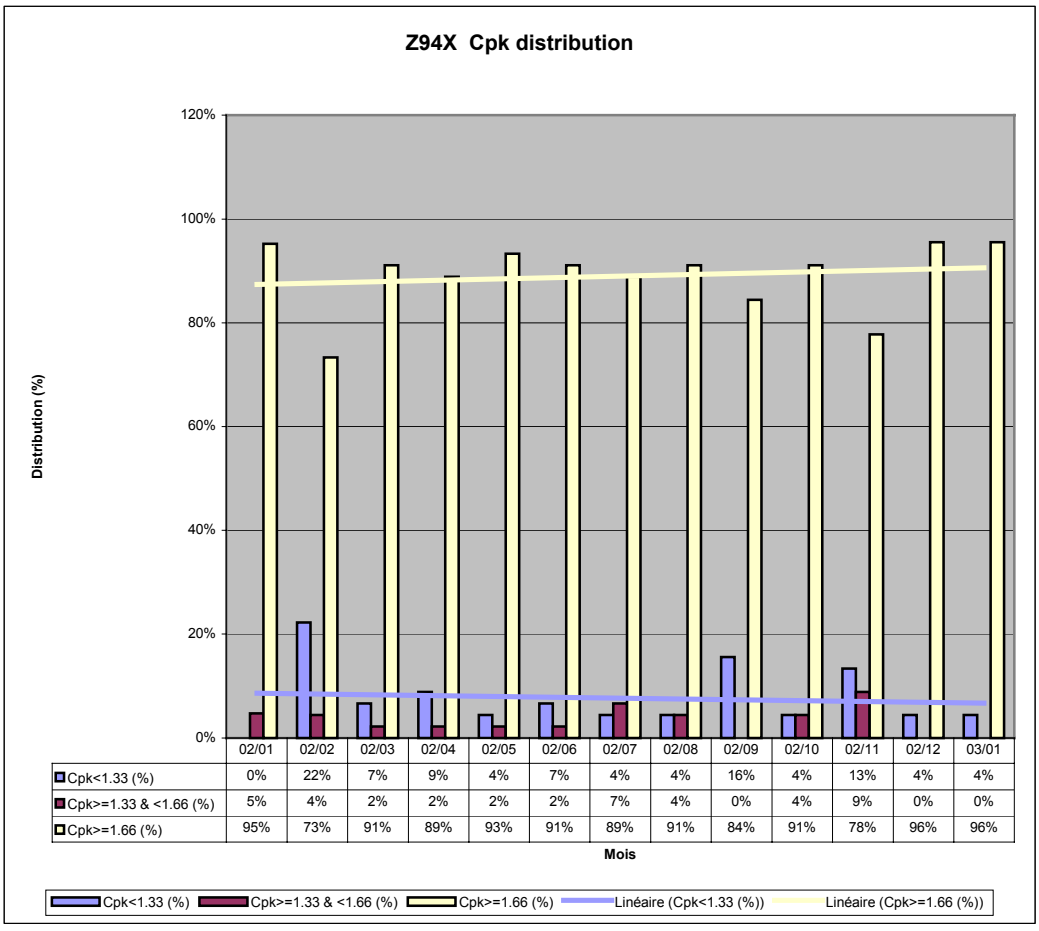
9.2 SCMOS3NV process (Z94X)

Parameters controlled during Electrical Test :

Same as Z92G with

EPROM junction Breakdown voltage, Programmed threshold voltage, ONO breakdown voltage
High Voltage MOS: oxide breakdown voltage, High voltage threshold voltage, High voltage junction breakdown
Depleted MOS: threshold voltage.

Cpk history (Last update 23/01/2003)



	02/01	02/02	02/03	02/04	02/05	02/06	02/07	02/08	02/09	02/10	02/11	02/12	03/01
Cpk<1.33 (%)	0%	22%	7%	9%	4%	7%	4%	4%	16%	4%	13%	4%	4%
Cpk>=1.33 & <1.66 (%)	5%	4%	2%	2%	2%	2%	7%	4%	0%	4%	9%	0%	0%
Cpk>=1.66 (%)	95%	73%	91%	89%	93%	91%	89%	91%	84%	91%	78%	96%	96%

10 Measurement System Analysis Study

Repeatability and Reproductability tests are performed on all the manufacturing equipments.
Critical parameters are followed by Cpk but equipment performance is followed by GRR and maintenance follow-up.

11 Qualified Laboratory Documentation

Internal Lab – COMPLIANT QS-9000 3rd edition

	Scope
Application Lab	Check the functionality of products to customer applications
Calibration Lab	Standard Gage Calibration
Characterization Lab	Product and process characterization before completing industrialization
Chemical Lab	Incoming inspection on chemical products and process monitoring on DI water , gases
Environmental Lab	Reliability Tests
Technology Analysis Lab	Failure Analysis and Yield enhancement

12 Control Plan

See attached file : Control Plan for Z92G process

13 Part Submission Warrant

Part Name **AT8XC5103** Part Number _____

Safety and/or Government Regulation ☐ Yes ☐ No Engineering Drawing Change Level _____ Dated _____

Additional Engineering Changes _____ Dated _____

Shown on Drawing No. _____ Purchase Order No. _____ Weight _____ kg

Checking Aid No. _____ Engineering Change Level _____ Dated _____

SUPPLIER MANUFACTURING INFORMATION

ATMEL Nantes SA
Supplier Name Supplier Code

La Chantrerie Route de Gachet BP 70602
Street Address

44306 Nantes Cedex 3 FRANCE
City/State/Postal Code

SUBMISSION INFORMATION

☐ Dimensional ☐ Materials/Functional ☐ Appearance

Customer Name/Division _____

Buyer/Buyer Code _____

Application _____

REASON FOR SUBMISSION

☒ Initial Submission
☐ Engineering Change(s)
☐ Tooling: Transfer, Replacement, Refurbishment, or additional
☐ Correction of Discrepancy
☐ Change to Optional Construction or Material
☐ Sub-Supplier or Material Source Change
☐ Change in Part Processing
☐ Parts Produced at Additional Location

☐ Other - please specify _____

REQUESTED SUBMISSION LEVEL (Check one)

☐ Level 1 - Warrant, Appearance Approval Report (for designated appearance items only).

☐ Level 2 - Warrant, Parts, Drawings, Inspection Results, Laboratory and Functional Results, Appearance Approval Report.

☒ Level 3 - At Customer Location - Warrant, Parts, Drawings, Inspection Results, Laboratory and Functional Results, Appearance Approval Report, Process Capability Results, Capability Study, Process Control Plan, Gage Study, FMEA.

☐ Level 4 - Per Level 3, but without parts.

☐ Level 5 - At Supplier Location - Warrant, Parts, Drawings, Inspection Results, Laboratory and Functional Results, Appearance Approval Report, Process Capability Results, Capability Study, Process Control Plan, Gage Study, FMEA.

SUBMISSION RESULTS

The results for ☒ dimensional measurements ☒ material and functional tests and ☒ appearance criteria and ☒ statistical process package meet all drawing and specification requirements: ☒ Yes ☐ No (If "No" - Explanation Required)

DECLARATION

I affirm that the samples represented by this warrant are representative of our parts and have been made to the applicable customer drawings and specifications and in the case of production samples, are made from specified materials on regular production tooling with no operations other than the regular production process. I have noted any deviations from this declaration below:

EXPLANATION/COMMENTS:

Print Name **René BORDIEC** Title **Design Assurance Quality Engineer** Phone No. **(33) 2 40 18 18 47**

Supplier Authorized Signature _____ Date _____

FOR CUSTOMER USE ONLY

Part Disposition ☐ Approved ☐ Rejected ☐ Other _____

Customer Name _____ Customer Signature _____ Date _____

14 Appearance Approval Report

Not Applicable for IC

15 Bulk Material Requirements

Not Applicable for IC

16 Sample Production Parts

Not attached, delivered previously

17 Master Sample

Not attached.

18 Checking Aids

Not applicable

19 Customer-Specific Requirements

Not specified.