AP4809

Stereo Headphone Amplifier With Shutdown Mode

■ Features

- Operate from 3V to 7V Single Supply Voltage
- High Signal-to-Noise ratio
- High Slew Rate
- Large Output Voltage Swing
- Low Distortion
- Low Power Consumption
- Switch On/Off Click suppression
- Excellent Power Supply Ripple Rejection
- SOP-8, PDIP-8 and MSOP-8 **Pb-Free** Packages

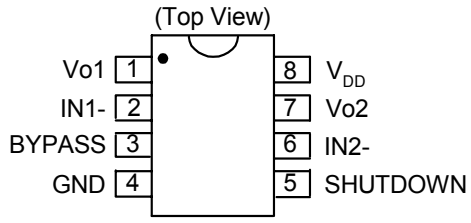
■ Applications

- CD-ROM, DVD-ROM
- MP3 Player
- Battery Powered Devices
- Personal Computers

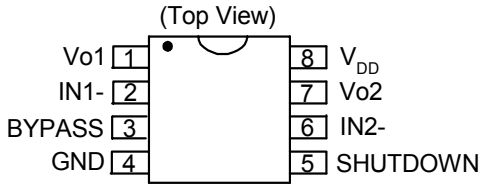
■ General Description

The AP4809 is a stereo power amplifier in an 8-pin SOP package capable of delivering 70mW continuous average power per channel into 32Ω loads with less than 0.1% (THD+N) from a 5V power supply. Amplifier gain is externally configured by means of two resistors per input channel. It was designed specially to provide high quality output power with a minimal amount of external components and is therefore optimally suited for low-power portable systems.

■ Pin Assignments



SOP-8L/PDIP-8L

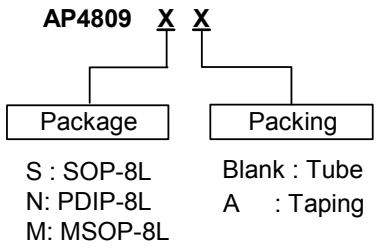


MSOP-8L

■ Pin Descriptions

Pin No.	Pin Name	Description
1	Vo1	Output 1
2	IN1-	Inverting input 1
3	BYPASS	Tap to voltage divider for internal mid-rail bias supply.
4	GND	Ground
5	SHUTDOWN	Logic low to put chip in shutdown mode.
6	IN2-	Inverting input 2
7	Vo2	Output 2
8	V_{DD}	Positive power supply

■ Ordering Information



■ Absolute Maximum Ratings (T_A=25°C)

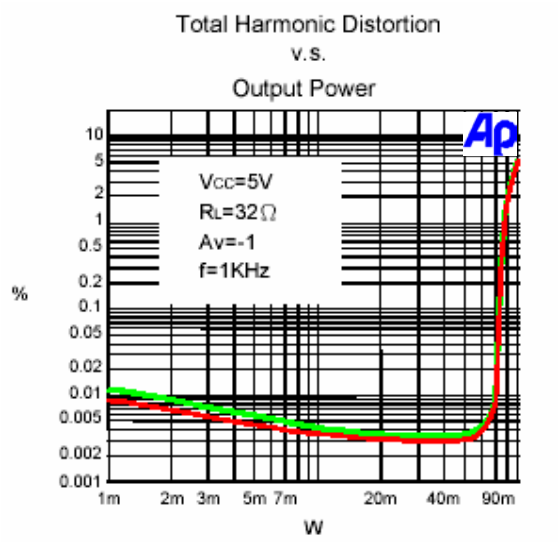
Symbol	Parameter	Max.	Unit
V_{DD}	Supply Voltage	7	V
T_J	Junction Temperature	150	°C
T_S	Soldering Temperature, 10 Seconds	250	°C
T_A	Operating Ambient Temperature Range	-40 to 85	°C
T_{STG}	Storage Temperature Range	-65 to 150	°C
V_{ESD}	ESD Susceptibility (Note 1)	2000	V
P_D	Package Power Dissipation	500	mW

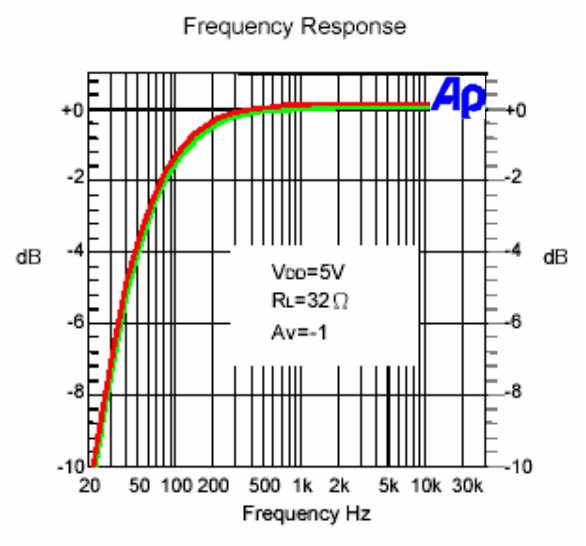
Note 1: Human Body Model, C=100pF, R=1500Ω, 3 positive pulses and 3 Negative Pulses.

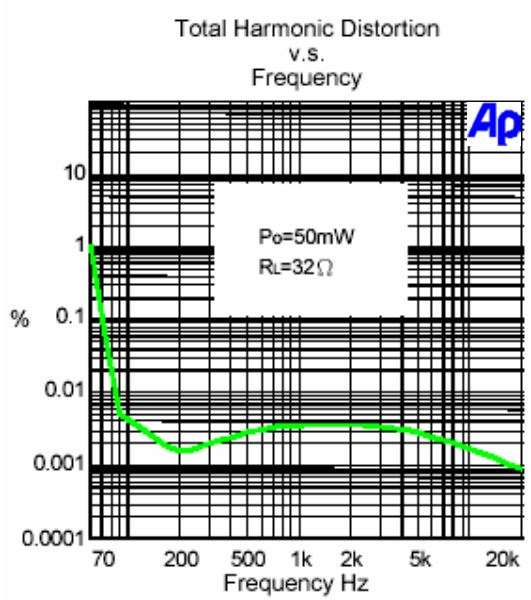
■ Electrical Characteristics (T_A=25°C, V_{DD}=5V, f_i=1KHz, R_L=32Ω)

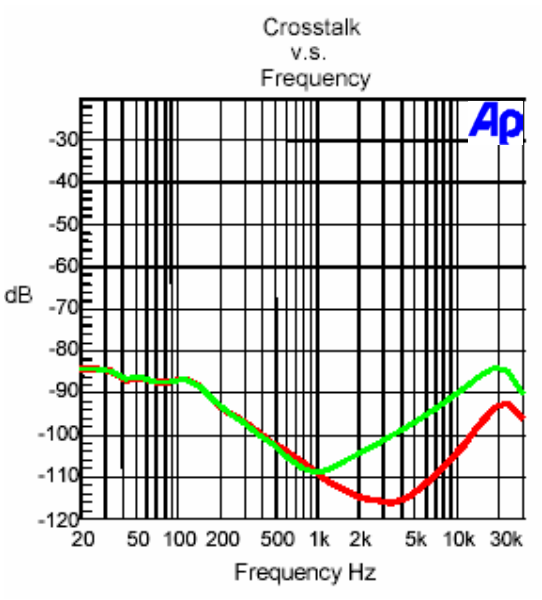
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		2.5	-	5.5	V
I_{DD}	Supply Current	V_{IN}=0V, I_O=0A	-	3	5	mA
P_{TOT}	Total Power Dissipation	V_{IN}=0V, I_O=0A	-	10	20	mW
$V_{I(OS)}$	Input Offset Voltage	V_{IN}=0V	-	5	-	mV
I_{BIAS}	Input Bias Current		-	10	-	pA
V_{CM}	Common Mode Voltage		0	-	3.5	V
G_V	Open-Loop Voltage Gain	R_L=5KΩ	-	80	-	dB
I_O	Max. Output Current	THD+N < 0.1%	-	80	-	mA
V_{SHUT}	Shutdown Enabled	Shutdown Pin Voltage	-	-	0.7	V
V_{SHUT}	Shutdown Disabled	Shutdown Pin Voltage	0.9	-	-	V
R_O	Output Resistance		-	0.3	-	Ω
V_O	Output Voltage Swing	R_L=16Ω, THD+N=0.1%	0.24	-	4.43	V
		R_L=32Ω, THD+N=0.1%	0.12	-	4.69	V
PSRR	Power Supply Ripple Rejection		-	75	-	dB
α_S	Channel Separation	R_L=32Ω	-	80	-	dB
THD+N	Total Harmonic Distortion + Noise	R_L=32Ω V_O=3.2V_{P-P} (at 0 dB)	-	0.02	-	%
SNR	Signal-TO-Noise Ratio	V_O=3.2V_{P-P} (at 0 dB)	-	105	-	dB
f_G	Unity Gain Frequency	Open Loop, R_L=5KΩ	-	6	-	MHz
P_O	Output Power	R_L=32Ω, THD+N=0.1%	-	75	-	mW
SR	Slew Rate	Unity Gain Inverting	-	6	-	V/μs

■ Typical Performance Characteristics

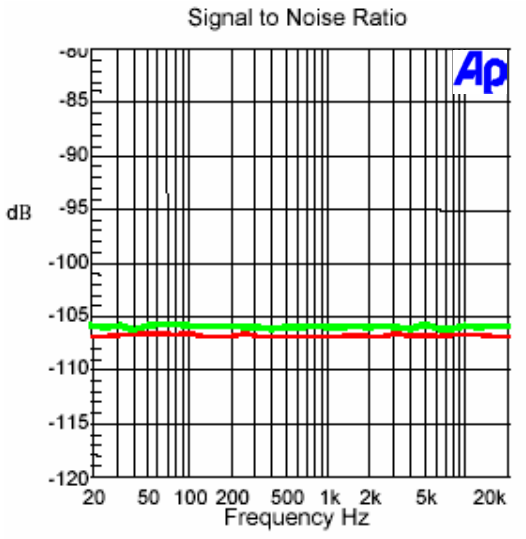


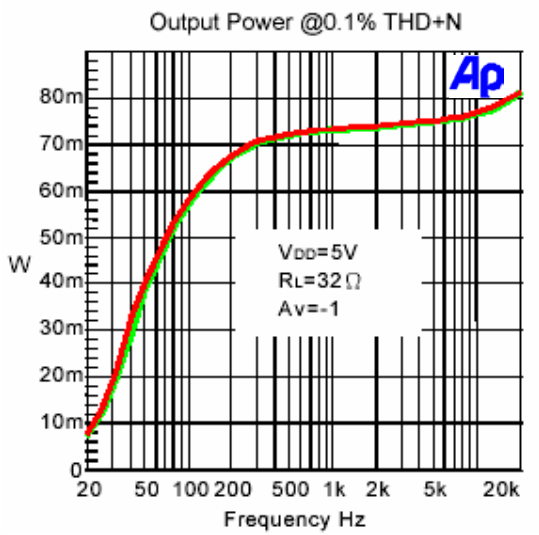




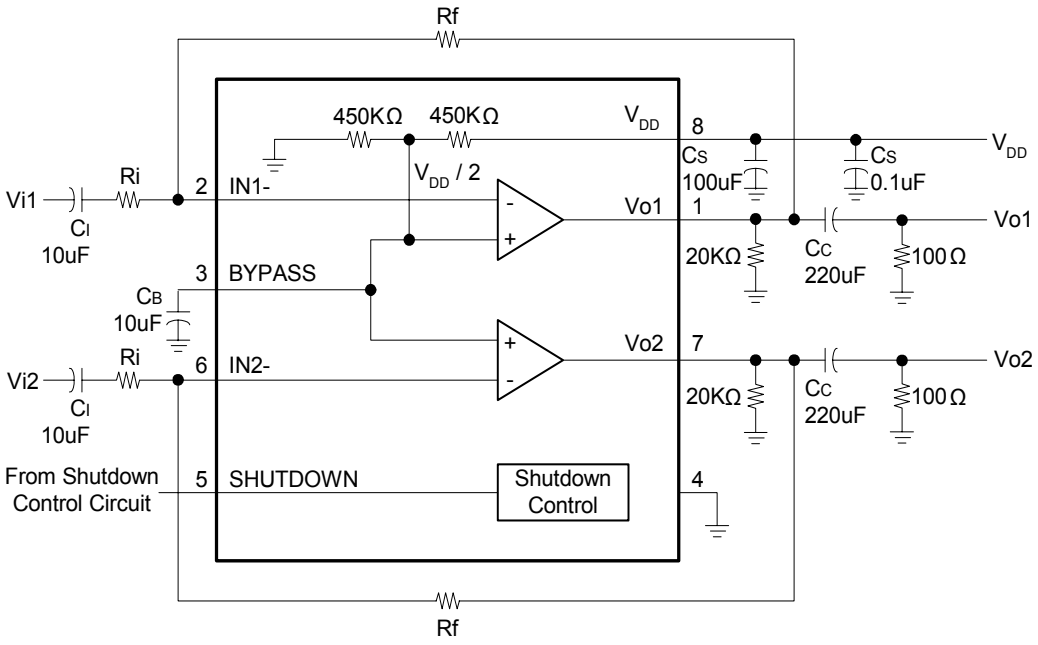


■ Typical Performance Characteristics





■ Test Circuit



■ Application Information

1. Input Capacitor, C_I

In the typical application, an input capacitor, C_i, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_i and R_i form a high-pass filter with the corner frequency determined in following equation (1).

$$f_{co(highpass)} = \frac{1}{2\pi R_i C_i} \quad (1)$$

The value of C_i is important to consider, as it directly affects the low frequency performance of the circuit. Consider the example where R_i is 15kΩ and the specification calls for a flat bass response down to 20Hz. Equation (1) is reconfigured as below:

$$C_i = \frac{1}{2\pi R_i f_{co(highpass)}} \quad (2)$$

In this example, C_i is 0.5 μF, so one would likely choose a value in the range of 1μF to 2.2μF. A further consideration for this capacitor is the leakage path from the input source through the input network (R_i, C_i) and the feedback resistor (R_f) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high-gain applications (>10). For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications, as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. It is important to confirm the capacitor polarity in the application.

2. Power Supply Decoupling, C_S

The AP4809 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1μF, placed as close as possible to the device V_{DD} lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10μF or greater placed near the power amplifier is recommended.

3. Mid-rail Bypass Capacitor, C_B

In the consideration of reducing the start-up pop, the mid-rail voltage should rise at a sub-sonic rate; that is, less than the rise time of 20Hz waveform and slower than the charging rate of both C_i & C_C. The relationship shown in equation (3) should be maintained to keep the noise as low as possible. Where C_B is the value of bypass capacitor and R_{SOURCE} is the equivalent source impedance of the voltage divider (the parallel combination of the two resistors)

$$\frac{1}{C_B \times R_{SOURCE}} \leq \frac{1}{C_i R_i} << \frac{1}{R_L R_C} \quad (3)$$

The bypass capacitor, C_B, serves several important functions. During start-up, C_B determines the rate at which the amplifier starts up. This helps to push the start-up pop noise into the sub-audible range (so slow it can not be heard). The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the mid-rail generation circuit internal to the amplifier. The capacitor is fed from the resistor divider with equivalent resistance of R_{SOURCE}. On selection of bypass capacitor, C_B, ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

4. Output Coupling Capacitor, C_C

In the typical single-supply single-ended (SE) configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier, thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation (4).

$$f_{(out\ high)} = \frac{1}{2\pi R_L C_C} \quad (4)$$

The main disadvantage, from a performance standpoint, is that the typically small load impedances drive the low-frequency corner higher. Large values of C_C are required to pass low frequencies into the load.

The output coupling capacitor required in single-supply SE mode also places additional constraints on the selection of other components in the amplifier circuit. With the rules described earlier still valid, add the following relationship:

■ Application Information (Continued)

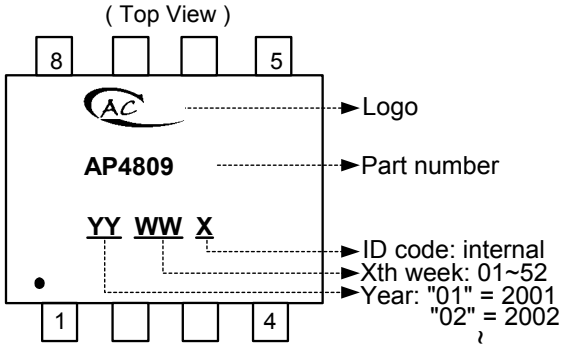
4.1 Output Pull-Down Resistor, R_C + R_O

Placing a 100Ω resistor, R_C, from the output side of the coupling capacitor to ground insures the coupling capacitor, C_C, is charged before a plug is inserted into the jack. Without this resistor, the coupling capacitor would charge rapidly upon insertion of a plug, leading to an audible pop in the headphones. Placing a 20kΩ resistor, R_O, from the output of the IC to ground insures that the coupling capacitor fully discharges at power down. If the supply is rapidly cycled without this capacitor, a small pop may be audible in 10kΩ loads.

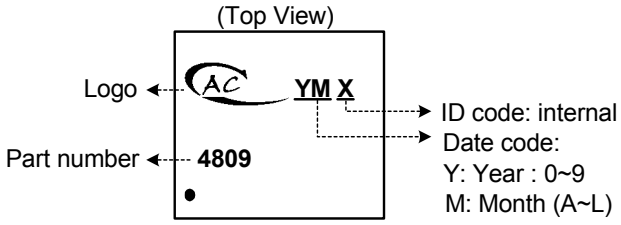
4.2 Using Low-ESR Capacitors

Low-ESR capacitors are recommended throughout this application. A real capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

■ Marking Information



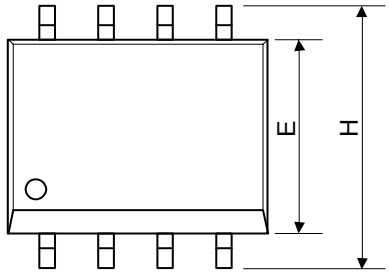
SOP-8L/PDIP-8L

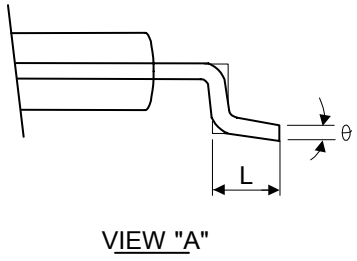


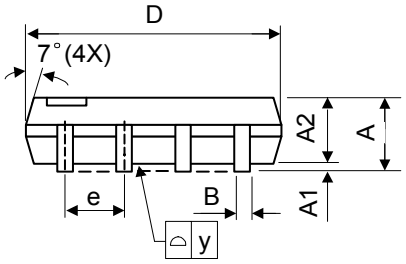
MSOP-8L

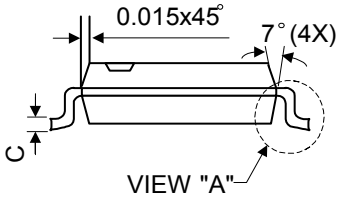
■ Package Information

(1) Package Type: SOP-8L





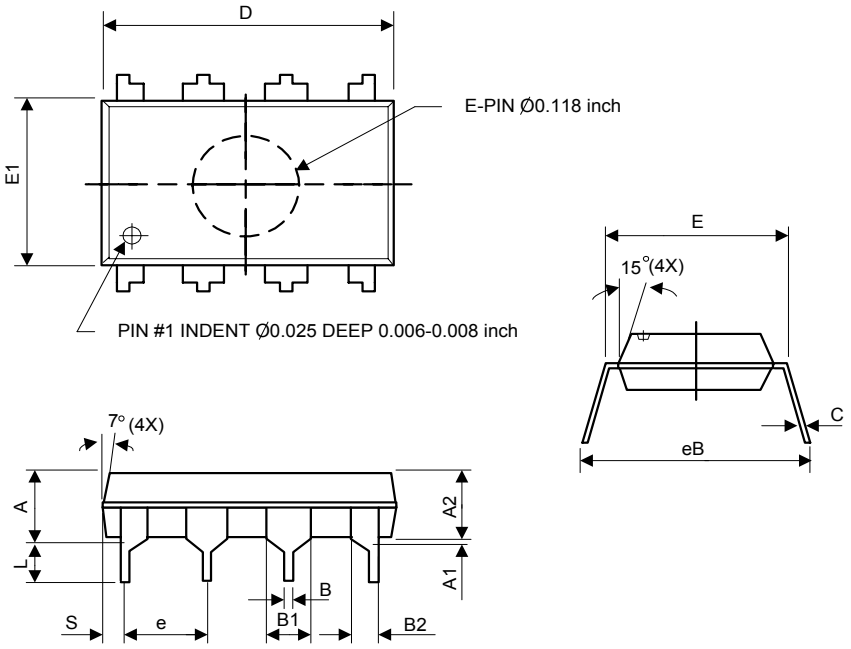




Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.40	1.60	1.75	0.055	0.063	0.069
A1	0.10	-	0.25	0.040	-	0.100
A2	1.30	1.45	1.50	0.051	0.057	0.059
B	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.010
D	4.80	5.05	5.30	0.189	0.199	0.209
E	3.70	3.90	4.10	0.146	0.154	0.161
e	-	1.27	-	-	0.050	-
H	5.79	5.99	6.20	0.228	0.236	0.244
L	0.38	0.71	1.27	0.015	0.028	0.050
y	-	-	0.10	-	-	0.004
θ	0^{O}	-	8^{O}	0^{O}	-	8^{O}

■ Package Information(Continued)

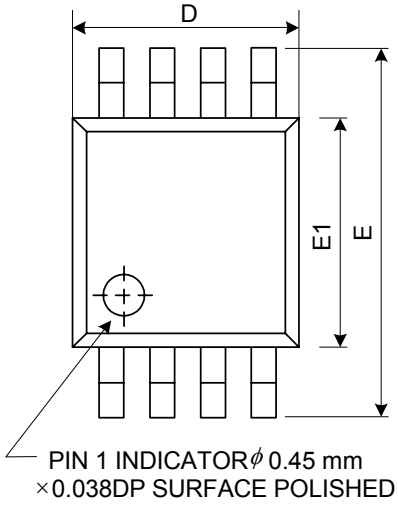
(2) Package Type: PDIP-8L

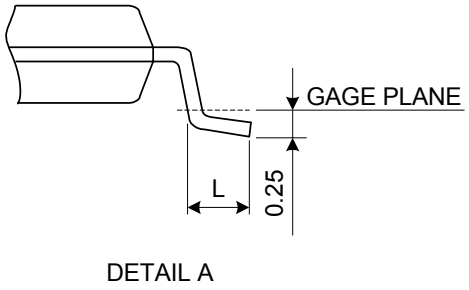


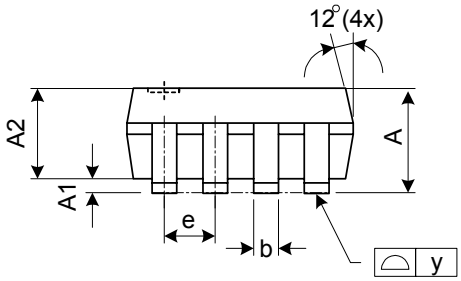
Symbol	Dimensions in millimeters			Dimensions in inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	5.33	-	-	0.210
A1	0.38	-	-	0.015	-	-
A2	3.1	3.30	3.5	0.122	0.130	0.138
B	0.36	0.46	0.56	0.014	0.018	0.022
B1	1.4	1.52	1.65	0.055	0.060	0.065
B2	0.81	0.99	1.14	0.032	0.039	0.045
C	0.20	0.25	0.36	0.008	0.010	0.014
D	9.02	9.27	9.53	0.355	0.365	0.375
E	7.62	7.94	8.26	0.300	0.313	0.325
E1	6.15	6.35	6.55	0.242	0.250	0.258
e	-	2.54	-	-	0.100	-
L	2.92	3.3	3.81	0.115	0.130	0.150
eB	8.38	8.89	9.40	0.330	0.350	0.370
S	0.71	0.84	0.97	0.028	0.033	0.038

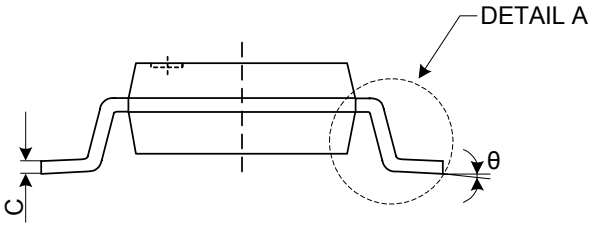
■ Package Information (Continued)

(3) Package Type: MSOP-8L









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	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.81	1.02	1.22	0.032	0.040	0.048
A1	0.05	-	0.15	0.002	-	0.006
A2	0.76	0.86	0.97	0.030	0.034	0.038
b	0.28	0.30	0.38	0.011	0.012	0.015
C	0.13	0.15	0.23	0.005	0.006	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.80	4.90	5.00	0.189	0.193	0.197
E1	2.90	3.00	3.10	0.114	0.118	0.122
e	-	0.65	-	-	0.0256	-
L	0.40	0.53	0.66	0.016	0.021	0.026
y	-	-	0.076	-	-	0.003
θ	0°	3°	6°	0°	3°	6°