Wideband/Differential Output Transimpedance Amplifier

AD8015

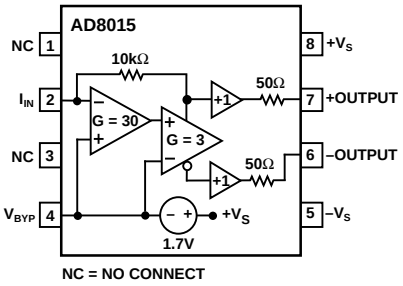
FEATURES

Low Cost, Wide Bandwidth, Low Noise
Bandwidth: 240 MHz
Pulse Width Modulation: 500 ps
Rise Time/Fall Time: 1.5 ns
Input Current Noise: 3.0 pA/$\sqrt{Hz}$ @ 100 MHz
Total Input RMS Noise: 26.5 nA to 100 MHz
Wide Dynamic Range
Optical Sensitivity: –36 dBm @ 155.52 Mbps
Peak Input Current: ±350 μA
Differential Outputs
Low Power: 5 V @ 25 mA
Wide Operating Temperature Range: –40°C to +85°C

APPLICATIONS

Fiber Optic Receivers: SONET/SDH, FDDI, Fibre Channel
Stable Operation with High Capacitance Detectors
Low Noise Preamplifiers
Single-Ended to Differential Conversion
I-to-V Converters

FUNCTIONAL BLOCK DIAGRAM



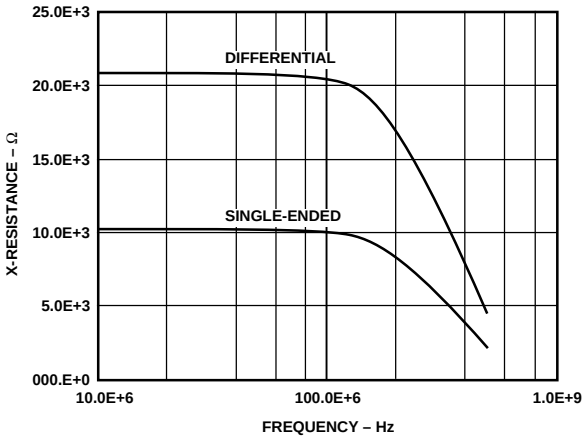


Figure 1. Differential/Single-Ended Transimpedance vs. Frequency

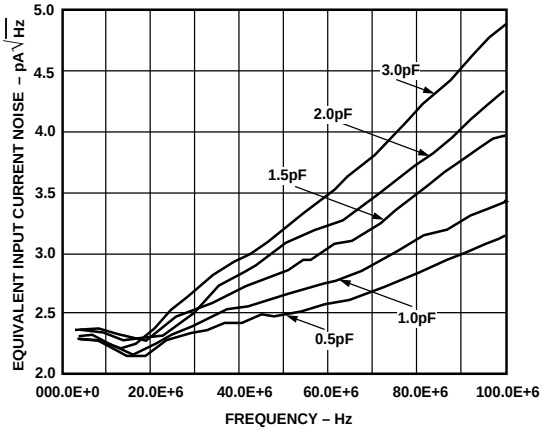


Figure 2. Noise vs. Frequency (SO-8 Package with Added Capacitance)

PRODUCT DESCRIPTION

The AD8015 is a wide bandwidth, single supply transimpedance amplifier optimized for use in a fiber optic receiver circuit. It is a complete, single chip solution for converting photodiode current into a differential voltage output. The 240 MHz bandwidth enables AD8015 application in FDDI receivers and SONET/SDH receivers with data rates up to 155 Mbps. This high bandwidth supports data rates beyond 300 Mbps. The differential outputs drive ECL directly, or can drive a comparator/ fiber optic post amplifier.

In addition to fiber optic applications, this low cost, silicon alternative to GaAs-based transimpedance amplifiers is ideal for systems requiring a wide dynamic range preamplifier or single-ended to differential conversion. The IC can be used with a standard ECL power supply (–5.2 V) or a PECL (+5 V) power supply; the common mode at the output is ECL compatible. The AD8015 is available in die form, or in an 8-pin SOIC package.

REV. A

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AD8015–SPECIFICATIONS (SO Package @ T_A = +25°C and V_S = +5 V, unless otherwise noted)

Parameter	Conditions	AD8015AR Min	Typ	Max	Units
DYNAMIC PERFORMANCE					
Bandwidth	3 dB	180	240		MHz
Pulse Width Modulation	10 µA to 200 µA Peak		500		ps
Rise and Fall Time	10% to 90%		1.5		ns
Settling Time[1]	to 3%, 0.5 V Diff Output Step		3		ns
INPUT					
Linear Input Current Range	±2.5%, Nonlinearity	±25	±30		µA
Max Input Current Range	Saturation	±200	±350		µA
Optical Sensitivity	155 Mbps, Avg Power		–36		dBm
Input Stray Capacitance	Die, by Design		0.2		pF
	SOIC, by Design		0.4		pF
Input Bias Voltage	$+V_S$ to I_{IN} and V_{BYP}	1.6	1.8	2.0	V
NOISE	Die, Single Ended at P_{OUT}, or Differential (P_{OUT}–N_{OUT}), C_{STRAY} = 0.3 pF				
Input Current Noise	f = 100 MHz		3.0		pA/√Hz
Total Input RMS Noise	DC to 100 MHz		26.5		nA
TRANSFER CHARACTERISTICS					
Transresistance	Single Ended	8	10	12	kΩ
	Differential	16	20	24	kΩ
Power Supply	Single Ended		37.0		dB
Rejection Ratio	Differential		40		dB
OUTPUT					
Differential Offset			6	20	mV
Output Common-Mode Voltage	From Positive Supply	–1.5	–1.3	–1.1	V
Voltage Swing (Differential)	Positive Input Current, R_L = ∞		1.0		V p-p
	Positive Input Current, R_L = 50 Ω		600		mV p-p
Output Impedance		40	50	60	Ω
POWER SUPPLY	T_{MIN} to T_{MAX}				
Operating Range	Single Supply	+4.5	+5	+11	V
	Dual Supply	±2.25		±5.5	V
Current			25	26	mA

NOTES
[1]Settling Time is defined as the time elapsed from the application of a perfect step input to the time when the output has entered and remained within a specified error band symmetrical about the final value. This parameter includes propagation delay, slew time, overload recovery, and linear settling times.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ($+V_S$ to $–V_S$) . . . . . 12 V
Internal Power Dissipation[2]
  Small Outline . . . . . 0.9 Watts
  Output Short Circuit Duration . . . . . Indefinite
Maximum Input Current . . . . . 10 mA
Storage Temperature Range . . . . . –65°C to +125°C
Operating Temperature Range (T_{MIN} to T_{MAX})
  AD8015ACHIP/AR . . . . . –40°C to +85°C
Maximum Junction Temperature . . . . . +165°C
Lead Temperature Range (Soldering 10 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for device in free air: 8-pin SOIC package: θ_{JA} = 155°C/W.

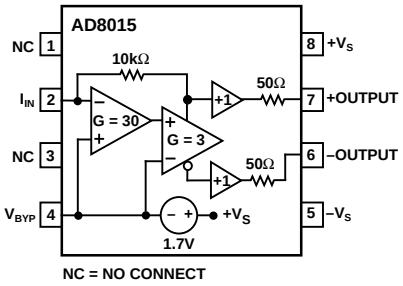
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8015AR	–40°C to +85°C	8-Pin Plastic SOIC	SO-8
AD8015ACHIPS	–40°C to +85°C	Die Form	

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8015 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

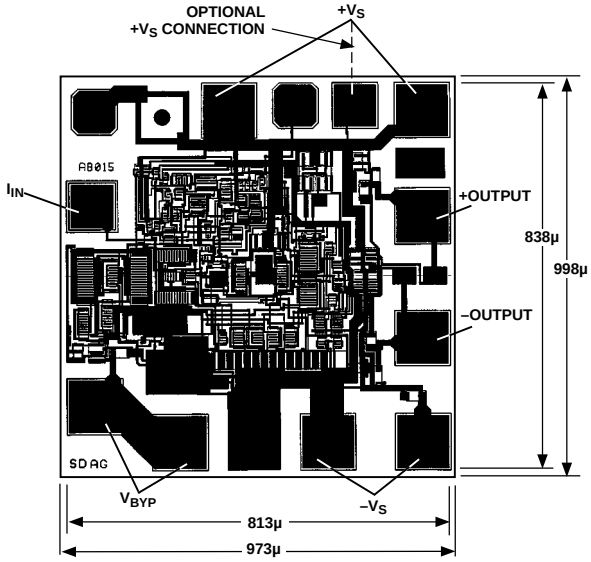
PIN CONFIGURATION



NC = NO CONNECT

METALIZATION PHOTOGRAPH

Dimensions shown in microns. Not to scale.



NOTE:
FOR BEST PERFORMANCE ATTACH PACKAGE SUBSTRATE TO $+V_S$.
MATERIAL AT BACK OF DIE IS SILICON. USE OF $+V_S$ OR $–V_S$ FOR DIE ATTACH IS ACCEPTABLE.

FIBER OPTIC RECEIVER APPLICATIONS

In a fiber optic receiver, the photodiode can be placed from the I_{IN} pin to either the positive or negative supply. The AD8015 converts the current from the photodiode to a differential voltage in these applications. The voltage at the V_{BYP} pin is ≈1.8 V below the positive supply. This node must be bypassed with a capacitor (C1 in Figures 3 and 4 below) to the signal ground. If large levels of power supply noise exist, then connecting C1 to $+V_S$ is recommended for improved noise immunity. For optimum performance, choose C1 such that $C1 > 1/(2\pi \times 1000 \times f_{MIN})$; where f_{MIN} is the minimum useful frequency in Hz.

PHOTODIODE REFERRED TO POSITIVE SUPPLY

Figure 3 shows the AD8015 used in a circuit where the photodiode is referred to the positive supply. The back bias voltage on the photodiode is ≈1.8 V. This method of referring the photodiode provides greater power supply noise immunity (PSRR) than referring the photodiode to the negative supply. The signal path is referred to the positive rail, and the photodiode capacitance is not modulated by high frequency noise that may exist on the negative rail.

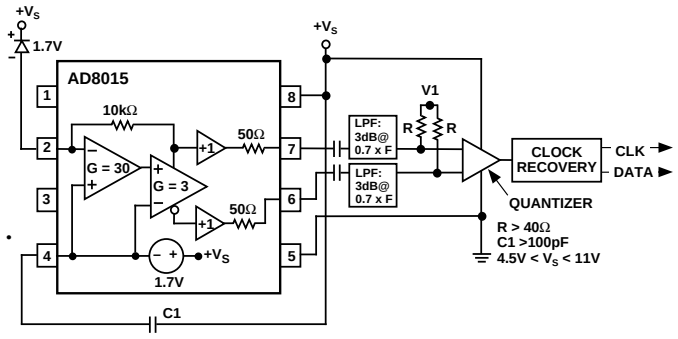


Figure 3. Fiber Optic Receiver Application: Photodiode Referred to Positive Supply

PHOTODIODE REFERRED TO NEGATIVE SUPPLY

Figure 4 shows the AD8015 used in a circuit where the photodiode is referred to the negative supply. This results in a larger back bias voltage than when referring the photodiode to the positive supply. The larger back bias voltage on the photodiode decreases the photodiode's capacitance thereby increasing its bandwidth. The R2, C2 network shown in Figure 4 is added to decouple the photodiode to the positive supply. This improves PSRR.

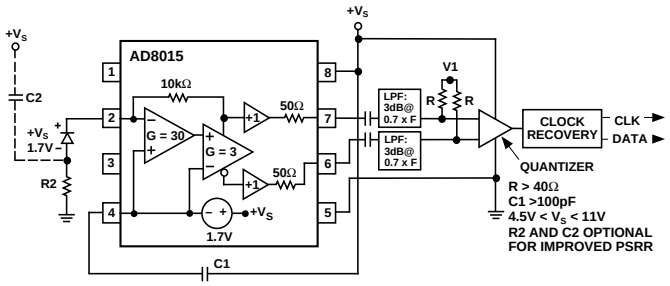


Figure 4. Fiber Optic Receiver Application: Photodiode Referred to Negative Supply

FIBER OPTIC SYSTEM NOISE PERFORMANCE

The AD8015 maintains 26.5 nA referred to input (RTI) to 100 MHz. Calculations below translate this specification into minimum power level and bit error rate specifications for SONET and FDDI systems. The dominant sources of noise are: 10 kΩ feedback resistor current noise, input bipolar transistor base current noise, and input voltage noise.

The AD8015 has dielectrically isolated devices and bond pads that minimize stray capacitance at the I_{IN} pin. Input voltage noise is negligible at lower frequencies, but can become the dominant noise source at high frequencies due to I_{IN} pin stray capacitance. Minimizing the stray capacitance at the I_{IN} pin is critical to maintaining low noise levels at high frequencies. The pins surrounding the I_{IN} pin (Pins 1 and 3) have no internal connection and should be left unconnected in an application. This minimizes I_{IN} pin package capacitance. It is best to have no ground plane or metal runs near Pins 1, 2, and 3 and to minimize capacitance at the I_{IN} pin.

The AD8015AR (8-pin SOIC) I_{IN} pin total stray capacitance is 0.4 pF without the photodiode. Photodiodes used for SONET or FDDI systems typically add 0.3 pF, resulting in roughly 0.7 pF total stray capacitance.

SONET OC-3 SENSITIVITY ANALYSIS

OC-3 Minimum Bandwidth = $0.7 \times 155\ MHz \approx 110\ MHz$

Total Current Noise = $(\pi/2) \times 26.5\ nA$

= 42 *nA* (*assuming single pole response*)

To maintain a BER < 1×10^{-10} (1 error per 10 billion bits):

Minimum current level needs to be > $13 \times$ *Total Current Noise*

= 541 *nA* (*peak*)

Assume a typical photodiode current/power conversion ratio

= 0.85 *A/W*

Sensitivity (minimum power level) = 541/0.85 *nW*

= 637 *nW (peak)*

= –32.0 *dBm (peak)*

= –35.0 *dBm (average)*

The SONET OC-3 specification allows for a minimum power level of –31 dBm peak, or –34 dBm average. Using the AD8015 provides 1 dB margin.

FDDI SENSITIVITY ANALYSIS

FDDI Minimum Bandwidth = $0.7 \times 125\ MHz \approx 88\ MHz$

$$Total\ Current\ Noise = (\pi/2) \times \frac{\sqrt{88\ MHz}}{\sqrt{100\ MHz}} \times 26.5\ nA$$

= 39 *nA* (*assuming single pole response*)

To maintain a BER < 2.5×10^{-10} (1 error per 4 billion bits):

Minimum current level needs to be > $12.6 \times$ *Total Current Noise*

= 492 *nA* (*peak*)

Assume a typical photodiode current/power conversion ratio

= 0.85 *A/W*

Sensitivity (minimum power level) = 492/0.85 *nW*

= 579 *nW (peak)*

= –32.4 *dBm (peak)*

= –35.4 *dBm (average)*

The FDDI specification allows for a minimum power level of –28 dBm peak, or –31 dBm average. Using the AD8015 provides 4.4 dB margin.

THEORY OF OPERATION

The simplified schematic is shown in Figure 5. Q1 and Q3 make up the input stage, with Q3 running at 300 µA and Q1 running at 2.7 mA. Q3 runs essentially as a grounded emitter. A large capacitor (0.01 µF) placed from V_{BYP} to the positive supply shorts out the noise of R17, R21, and Q16. The first stage of the amplifier (Q3, R2, Q4, and C1) functions as an integrator, integrating current into the I_{IN} pin. The integrator drives a differential stage (Q5, Q6, R5, R3, and R4) with gains of +3 and –3. The differential stage then drives emitter followers (Q41, Q42, Q60 and Q61). The positive output of the differential stage provides the feedback by driving R_{FB}. The differential outputs are buffered using Q7 and Q8.

The bandwidth of the AD8015 is set to within ±20% of the nominal value, 240 MHz, by factory trimming R5 to 60 Ω. The following formula describes the AD8015 bandwidth:

$$Bandwidth = 1/(2\pi \times C1 \times R_{FB} \times (R5 + 2\ re)/R4)$$

where *re* (of Q5 and Q6) = 9 Ω each, constant over temperature, and $R_{FB}/R4$ = 43.5, constant over temperature.

The bandwidth equation simplifies, and the bandwidth depends only on the value of C1:

$$Bandwidth = 1/(2\pi \times 3393 \times C1).$$

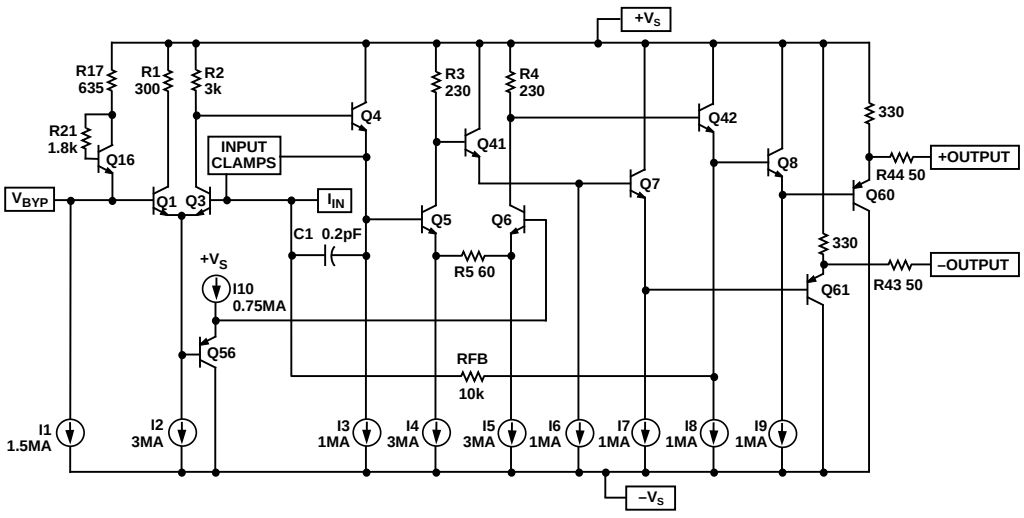


Figure 5. AD8015 Simplified Schematiic

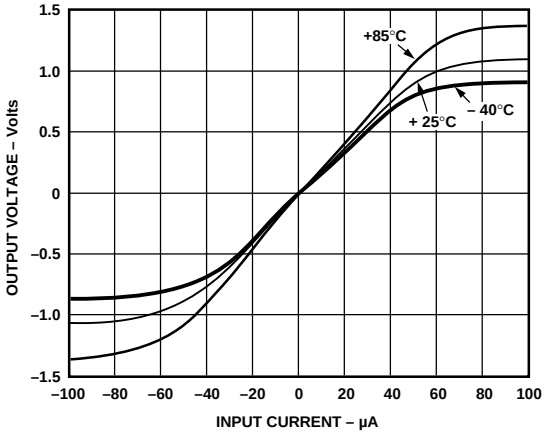


Figure 6. Differential Output vs. Input Current

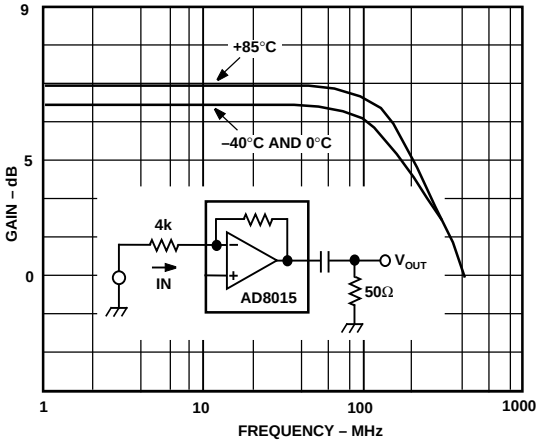


Figure 9. Gain vs. Frequency

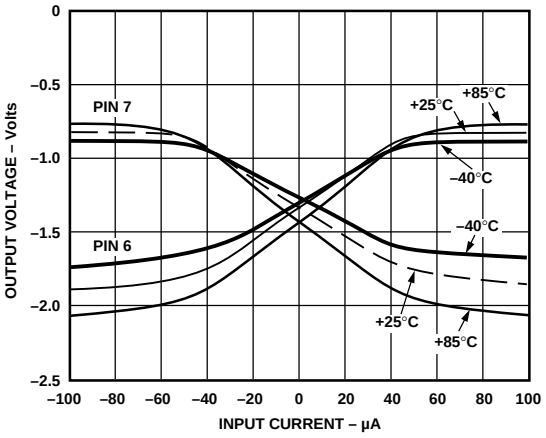


Figure 7. Single-Ended Output vs. Input Current

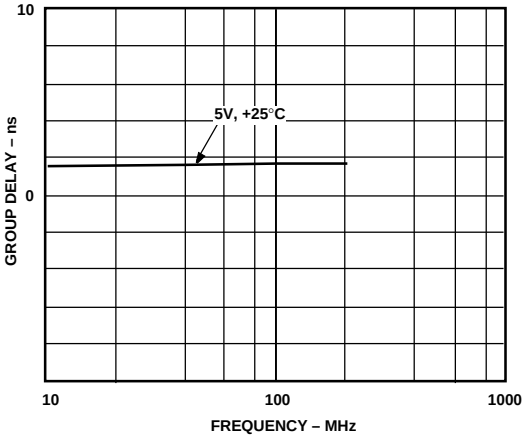


Figure 10. Group Delay vs. Frequency

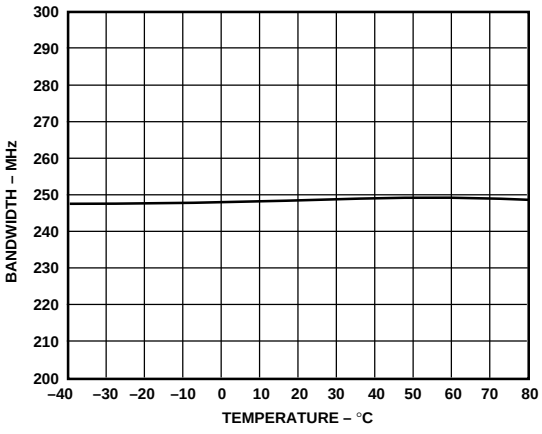


Figure 8. Bandwidth vs. Temperature

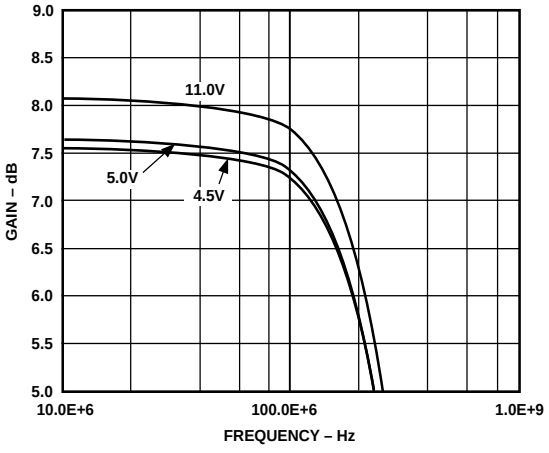


Figure 11. Differential Gain vs. Supply

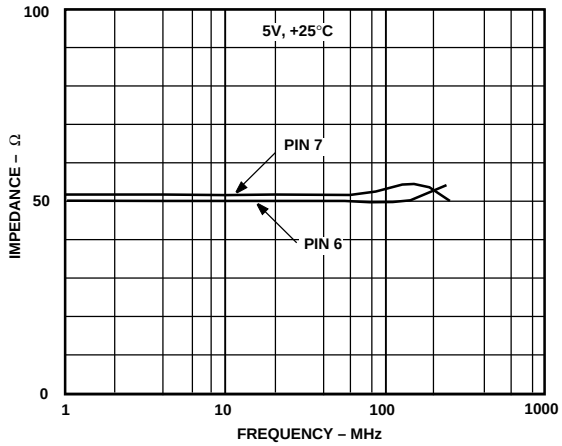


Figure 12. Output Impedance vs. Frequency

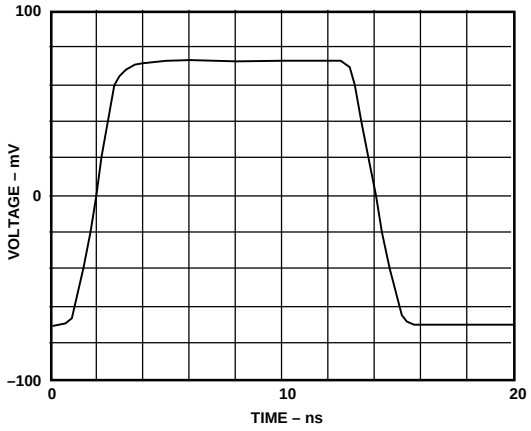


Figure 13. Small Signal Pulse Response

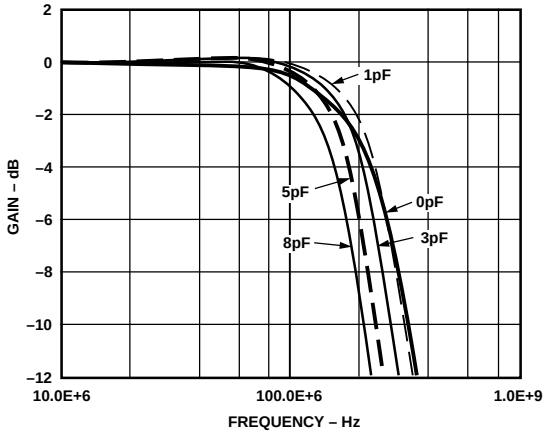


Figure 14. Differential Gain vs. Input Capacitance

APPLICATION

155 Mbps Fiber Optic Receiver

The AD8015 and AD807 can be used together for a complete 155 Mbps Fiber Optic Receiver (Transimpedance Amplifier, Post Amplifier with Signal Detect Output, and Clock Recovery and Data Retiming) as shown in Figure 16.

The PIN diode front end is connected to a single mode, 1300 nm laser source. The PIN diode has 3.3 V reverse bias, 0.8 A/W responsivity, 0.7 pF capacitance, and 2.5 GHz bandwidth.

The AD8015 outputs (P_{OUT} and N_{OUT}) drive a differential, constant impedance (50 Ω) low-pass π filter with a 3 dB cutoff of 100 MHz. The outputs of the low-pass filter are ac coupled to the AD807 inputs (PIN and NIN). The AD807 PLL damping factor is set at 10 using a 0.22 µF capacitor.

The entire circuit was enclosed in a shielded box. Table I summarizes results of tests performed using a 2^{23}–1 PRN sequence, and varying the average power at the PIN diode.

The circuit acquires and maintains lock with an average input power as low as –39.25 dBm.

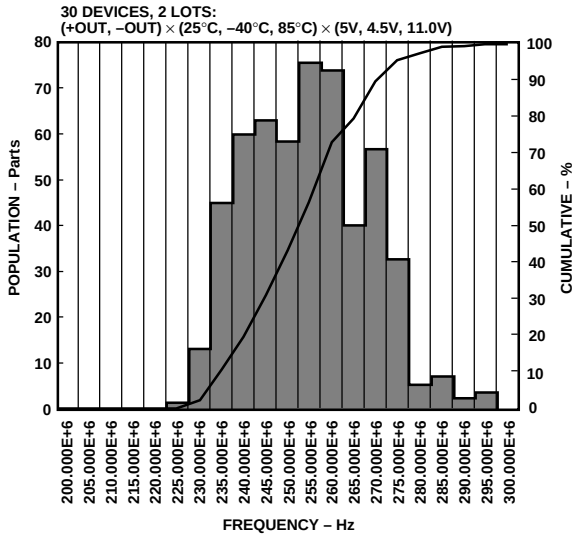


Figure 15. Bandwidth Distribution Matrix

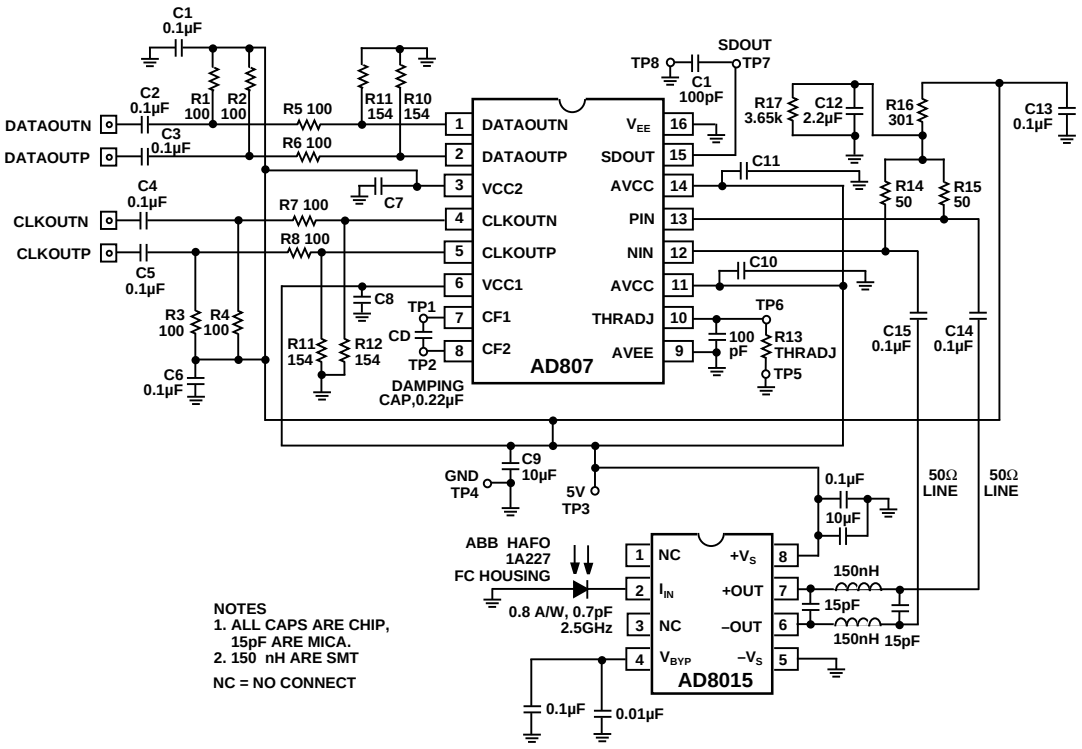


Figure 16. 155 Mbps Fiber Optic Receiver Schematic

Table I. AD8015, AD807 Fiber Optic Receiver Circuit: Output Bit Error Rate & Output Jitter vs. Average Input Power

Average Optical Input Power (dBm)	Output Bit Error Rate	Output Jitter (ps rms)
–6.4	Loses Lock	
–6.45	1.2×10^{-2}	
–6.50	7.5×10^{-3}	
–6.60	9.4×10^{-4}	
–6.70	1×10^{-14}	
–7.0 to –35.50	1×10^{-14}	< 40
–36.00	3.0×10^{-12}	< 40
–36.50	4.8×10^{-10}	
–37.00	2.8×10^{-8}	
–37.50	8.2×10^{-7}	
–38.00	1.3×10^{-5}	
–38.50	1.1×10^{-4}	
–39.00	1.0×10^{-3}	
–39.1	1.3×10^{-3}	
–39.20	1.9×10^{-3}	
–39.25	2.2×10^{-3}	
–39.30	Loses Lock	

AC COUPLED PHOTODIODE APPLICATION FOR IMPROVED DYNAMIC RANGE

AC coupling the photodiode current input to the AD8015 (Figure 17) extends fiber optic receiver overload by 3 dB while sacrificing only 1 dB of sensitivity (increasing receiver dynamic range by 2 dB). This application results in typical overload of –4 dBm, and typical sensitivity of –35 dBm. AC coupling the input also results in improved pulse width modulation performance.

Careful attention to minimize parasitic capacitance at the AD8015 input (from the photodetector input), R_{AC} and C_{AC} are critical for sensitivity performance in this application. Note that C_{AC} of 0.01 μF was chosen for a low frequency cutoff equal to 2.2 kHz.

C1973–6–1/96

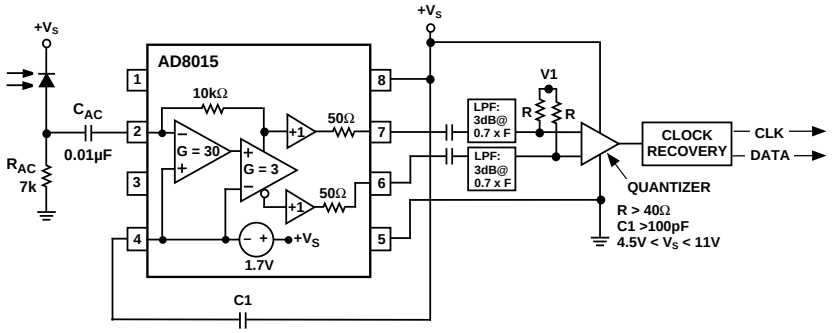
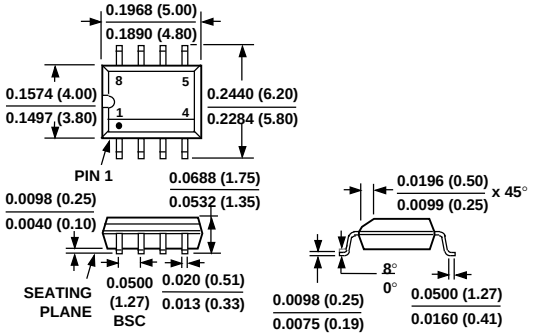


Figure 17. AC Coupled Photodiode Application for Improved Dynamic Range

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead Small Outline IC Package (SO-8)



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