TC40H166P/F

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC40H166 8-BIT SHIFT REGISTER (P/S-IN, S-O)

The TC40H166 is an 8-bit PARALLEL-IN and SERIAL-OUT shift register, permitting SERIAL-IN and SERIAL-out operations.

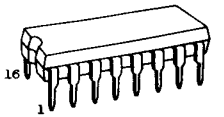
In PARALLEL operation, PARALLEL-IN DATA are shifted at the rising edge of CLOCK in sequence and outputted from the final stage of F/F.

In SERIAL operation, each F/F is triggered at the rising edge of CLOCK.

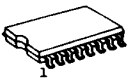
Switching of PARALLEL operation and SERIAL operation is made by SHIFT/LOAD input

When SHIFT/LOAD input is at "H" level, SERIAL operation is performed, and when SERIAL operation is at "L" level, PARALLEL operation is performed.

The function and pin assignment of the TC40H166 are the same as those of the 74LS166.

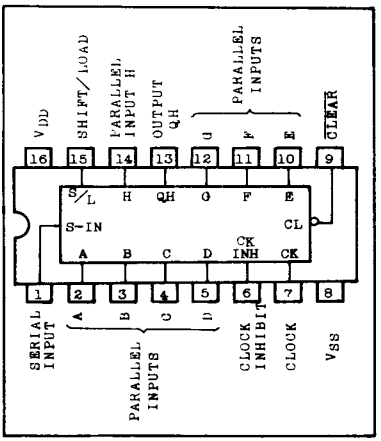


DIP16(3D16A-P)



MFP16(F16GC-P)

PIN CONNECTION



MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5 ∿ V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5 ∿ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ∿ V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Storage Temperature	Tstg	-65 ∿ 150	°C
Lead Temp./Time	Tsol	260°C • 10 sec	

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0.0V)

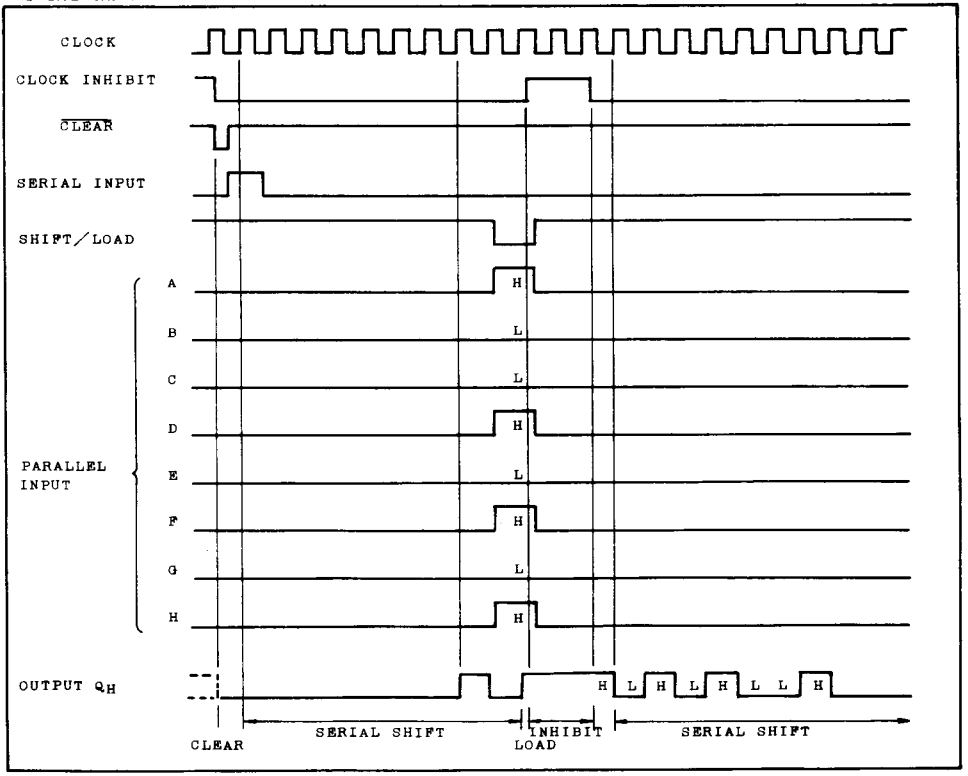
CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	-	2.0	-	8.0	V
Input Voltage	V_{IN}	-	0	-	V_{DD}	V
Operating Temperature	Topr	-	-40	-	85	°C

TRUTH TABLE

INPUTS							OUTPUTS			FUNCTION MODE
$\overline{CLEAR}$	SHIFT/LOAD	CLOCK INHIBIT	CLOCK	SERIAL INPUT	PARALLEL INPUT A	PARALLEL INPUT H	INTERNAL Q_A	INTERNAL Q_B	Q_H	
L	*	*	*	*	*	*	L	L	L	Clear
H	H	L	↑	L	*	*	L	Q_{An}	Q_{Gn}	Shift
H	H	L	↑	H	*	*	H	Q_{An}	Q_{Gn}	
H	L	L	↑	*	L	L	L	P_{INB}	L	Parallel Load
H	L	L	↑	*	L	H	L	P_{INB}	H	
H	L	L	↑	*	H	L	H	P_{INB}	L	
H	L	L	↑	*	H	H	H	P_{INB}	H	
H	*	H	*	*	*	*	Q_{AO}	Q_{BO}	Q_{HO}	Hold
H	*	*	↓	*	*	*	Q_{AO}	Q_{BO}	Q_{HO}	No change

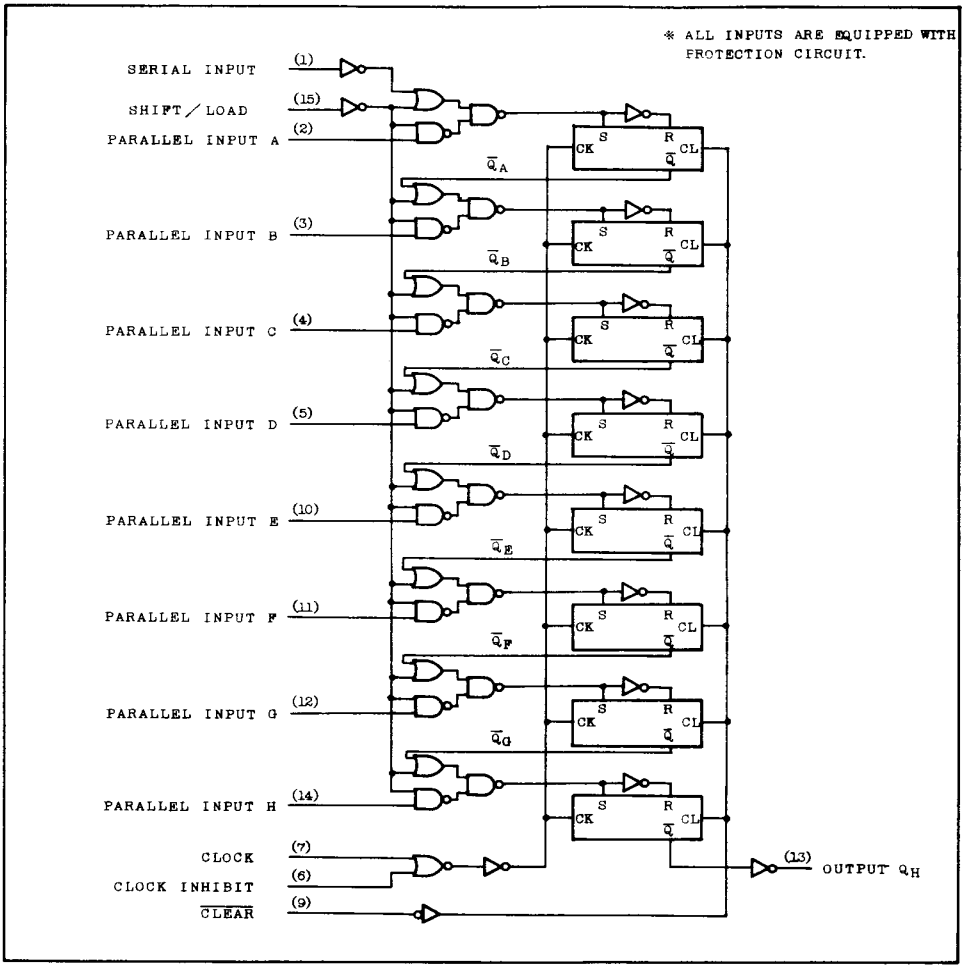
*= Don't care Q_{no}= Data one clock before

TIMING CHART



TC40H166P/F

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (V_{SS}=0.0V)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage		V_{OH}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage		V_{OL}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.0	0.05	-	0.05	V
High Level Output Current		I_{OH}	V_{OH}=4.6V $V_{IN}=V_{SS},V_{DD}$	5	-0.52	-	-0.44	-	-	-0.36	-	mA
Low Level Output Current		I_{OL}	V_{OL}=0.4V $V_{IN}=V_{SS},V_{DD}$	5	1.4	-	1.1	-	-	0.8	-	mA
Input Voltage	"H" Level	V_{IH}	$\|I_{OUT}\|<1\mu A$ V_{OUT}=0.5V V_{OUT}=4.5V	5	4.0	-	4.0	-	-	4.0	-	V
	"L" Level	V_{IL}		5	-	1.0	-	-	1.0	-	1.0	V
Input Current	"H" Level	I_{IH}	V_{IH}=8.0V	8	-	0.3	-	10^{-5}	0.3	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0.0V	8	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	μA
Quiescent Supply Current		I_{DD}	*$V_{IN}=V_{SS},V_{DD}$	5	-	12.5	-	10^{-3}	12.5	-	75	μA

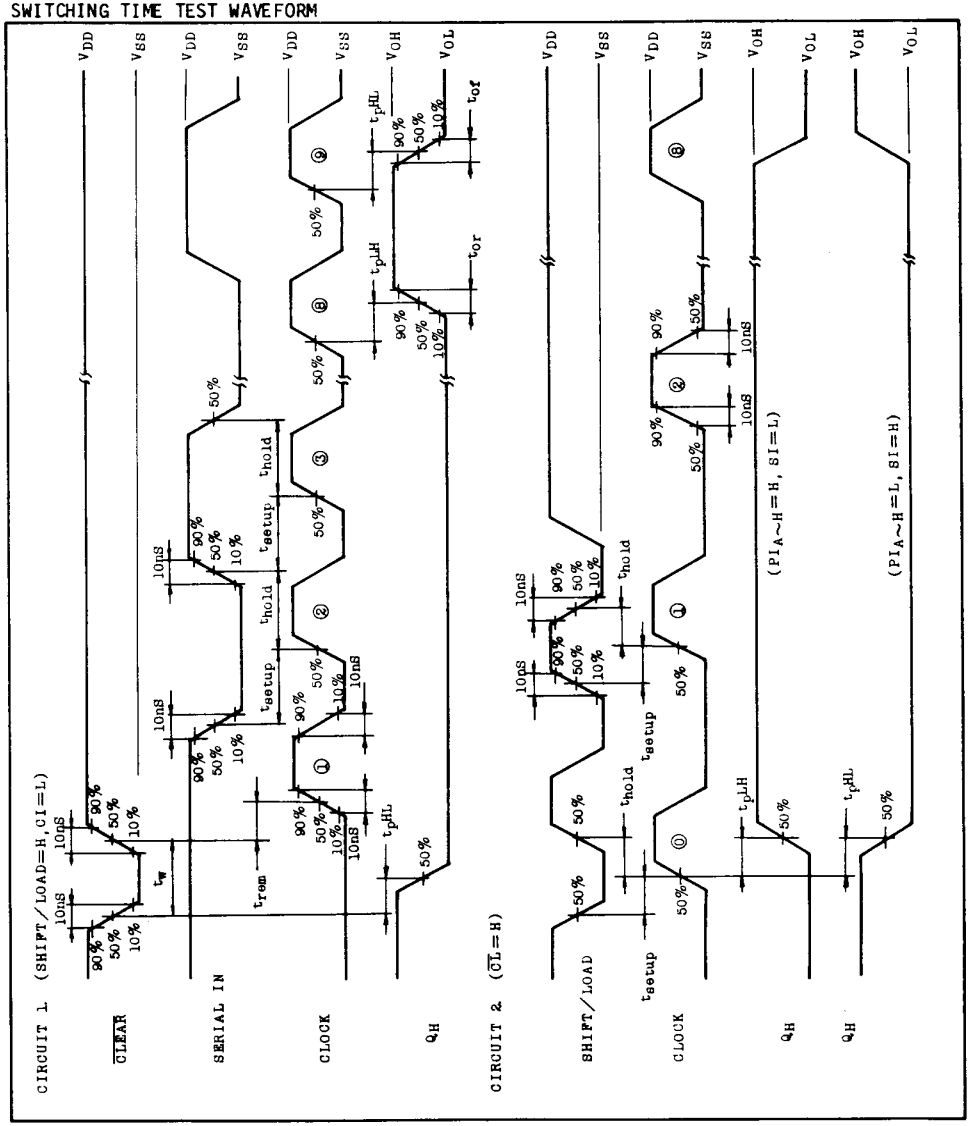
*All valid input combinations.

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, V_{DD}=5V, C_L=15pF)

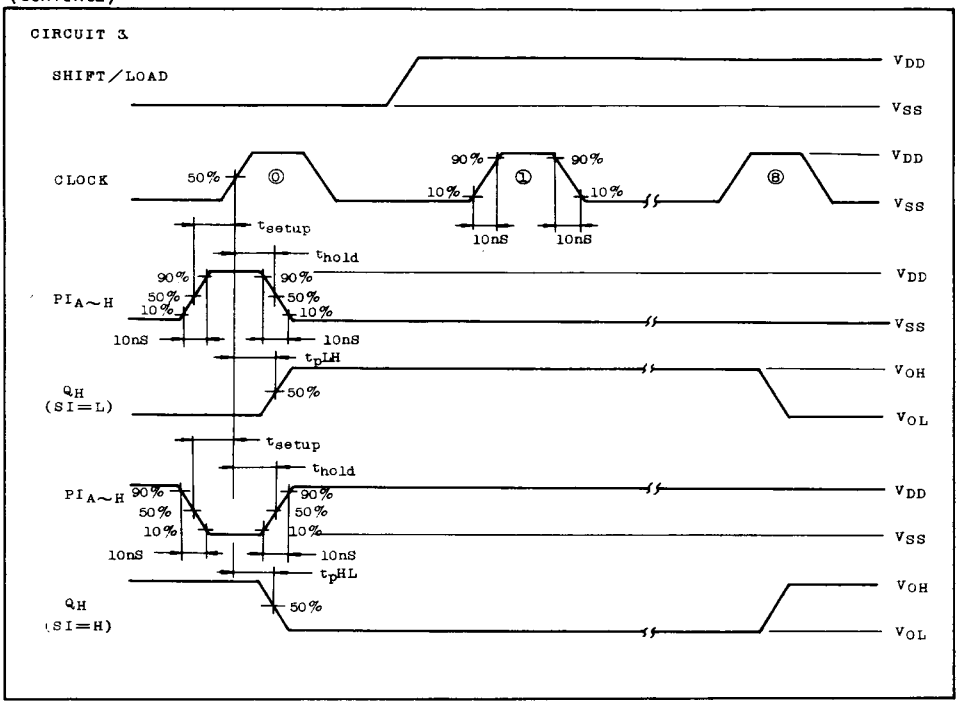
CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Rise Time		t_{or}	Fig. 1	-	17	35	ns
Output Fall Time		t_{of}		-	14	30	ns
Propargation Delay Time	(Low-High)	t_{pLH}	CLOCK - Q_H Figs.1,2,3	-	29	44	ns
	(High-Low)	t_{pHL}		-	36	54	ns
Propergation Deley Time (High-Low)		t_{pHL}	$\overline{CLEAR}$ - Q_H Fig. 1	-	38	57	ns
Maximum Clock Frequency		$f_{max\phi}$		15	25	-	MHz
Max Clock Rise Time Fall Time		$t_{r\phi}$, $t_{f\phi}$			20	-	μs
Min. Clear Width of Pulse		t_W	Fig. 1	-	15	27	ns
Min. Clear Remobal Time		t_{rem}	Fig. 2	-	12	25	ns
Min. Data Setup Time		t_{set-up}	PI, SI Fig. 1, 3	-	-	25	ns
Min. Data Setup Time		t_{set-up}	SIFT/LOAD Fig. 2	-	-	35	ns
Min. Data Hold Time		t_{hold}	PI, SI Fig. 1, 3	-	-	0	ns
Min. Data Hold Time		t_{hold}	SHIFT/LOAD Fig. 2	-	-	0	ns
Input Capacitance		C_{IN}		-	5	-	pF

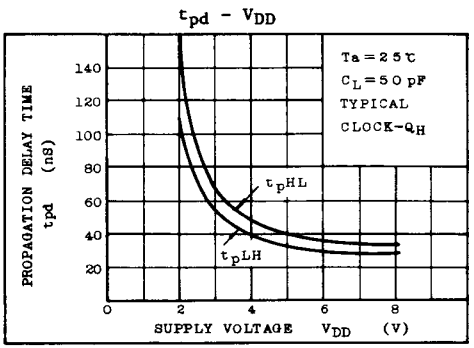
TC40H166P/F

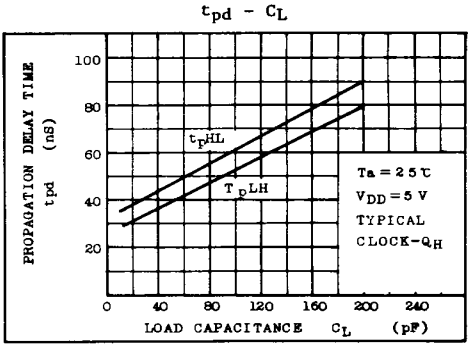
SWITCHING TIME TEST WAVEFORM



(CONTINUE)

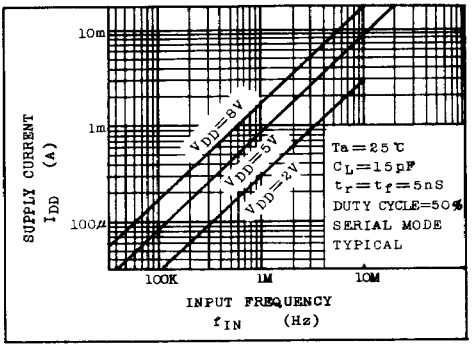




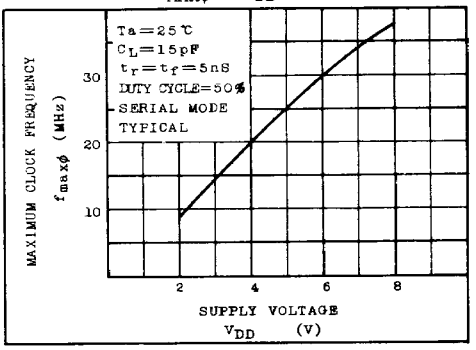


TC40H166P/F

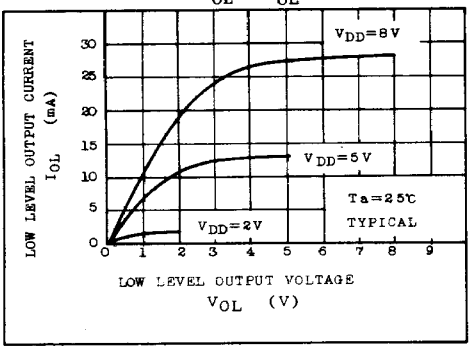
I_{DD} - f_{IN}



$f_{MAX\phi}$ - V_{DD}



I_{OL} - V_{OL}



I_{OH} - (V_{DD} - V_{OH})