TOSHIBA MPEG-4 Video Decoder LSI

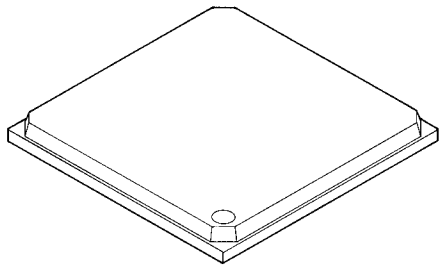
TC35274

Tentative Technical Data Sheet

MPEG-4 Video Decoder LSI

Features

- A single-chip MPEG-4 video decoder LSI performs 15frames/sec of MPEG-4 video decoding with QCIF (176x144 pixels) at 30MHz clock frequency.
- A 4-Mbit embedded DRAM is integrated to reduce power consumption without performance degradation.
- An MPEG-4 video core consists of a 16-bit RISC processor and dedicated hardware accelerators so as to bring programmability, high performance, and low power consumption.



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- Firmware program for the RISC is downloaded into the embedded DRAM before starting operation. Other applications, such as H.263, are performed by using appropriate firmware.
- General host interface is adopted in order to support various host CPU.

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1. Functional Specifications

1.1 MPEG-4 Video Decoder

ISO MPEG-4 IS SP@L1 decoding is executed with QCIF (176x144 pixels) at 15 frames/sec.

YCbCr 4:2:2 8bit digital image data output to a LCD via an external LCD controller.

Size conversion and de-blocking filter operatation.

16-bit parallel host interface.

1.2 System Configurations

Fig. 1 illustrates a block diagram of TC35274.

- Before starting operation, an external host CPU downloads a firmware into an embedded DRAM via a host interface.
- Encoded video bitstream are transferred from a host CPU via a host interface, and stored into the embedded DRAM. Then, an MPEG-4 video core decodes the bitstream.
- The decoded pictures output to an external LCD controller via an LCD I/F.

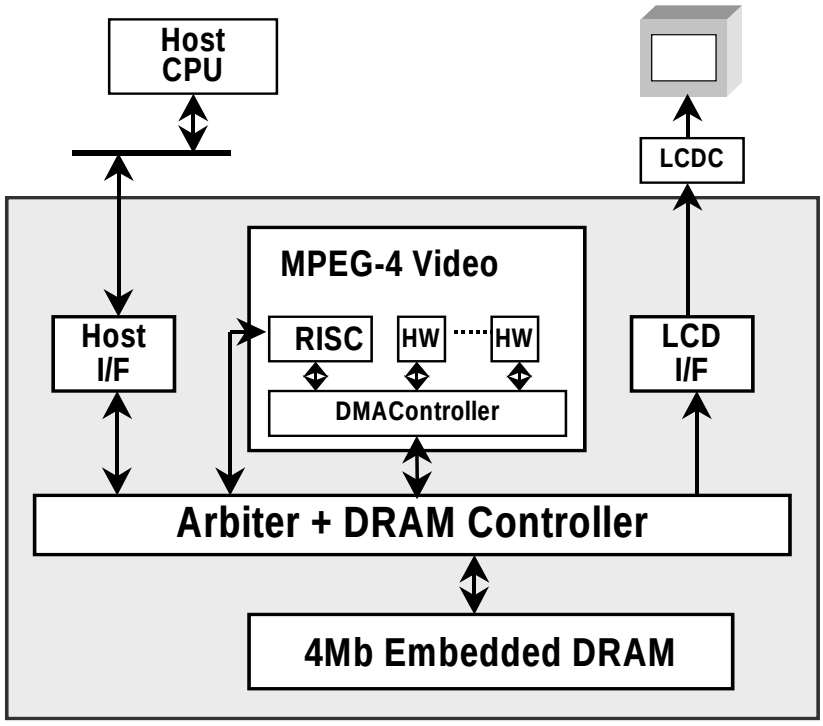

Fig. 1 Block diagram of TC35274

* In order to run this LSI as an MEPG-4 video decoder LSI, Specified firmware programs have to be obtained in advance.

2. Terminals

2.1 Pin Assignment

TBD

2.2 Pin Allocation

TBD

2.3 I/O Pins

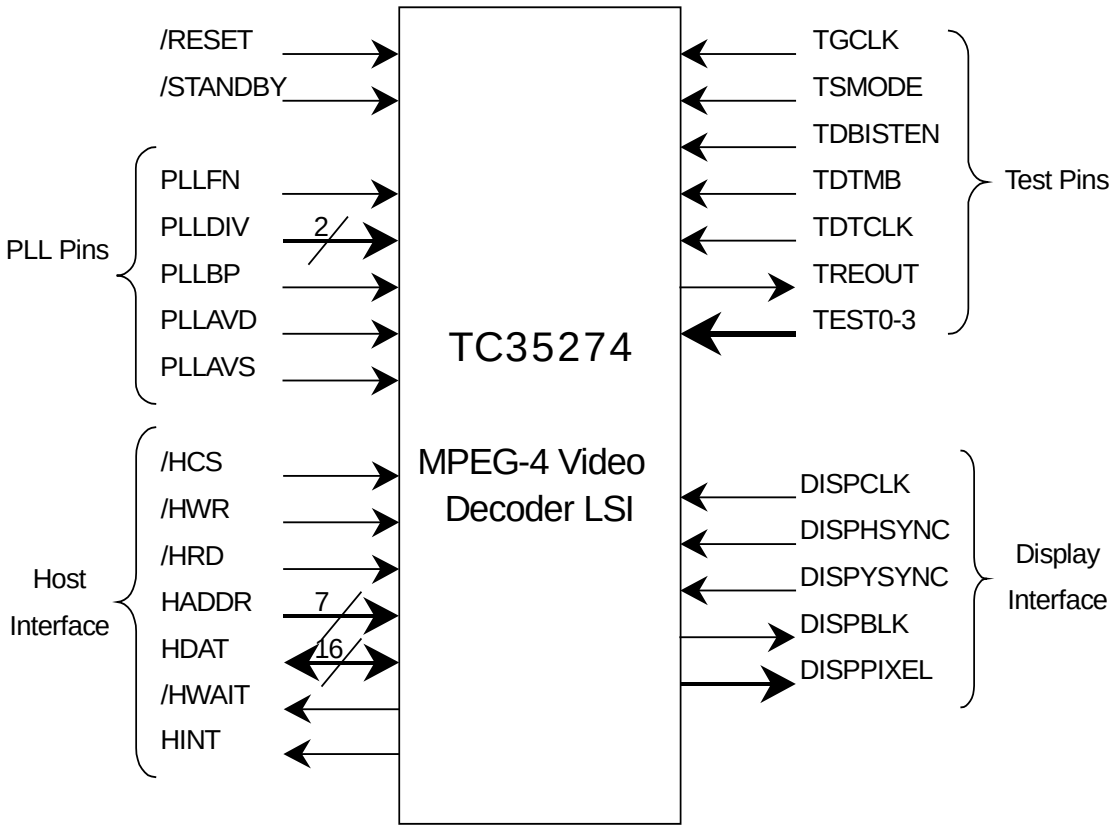

Fig. 2 Pin Map

Table 1. System Control Signals

Signal Name	In/Out	Bit Width	Description
/RESET	In	1	System Reset Input (Low Active). When the LSI is reset, this terminal has to be low for more than 16 clock cycles. When power on, the LSI has to be reset after PLL locked. It takes approximately 100us until the PLL locked.
STANDBY	In	1	System Standby Input (High Active). Stop clock distribution to the LSI. After standby, system reset is required. "0" : Active. "1" : Standby.

Table 2. PLL Control Signals

Signal Name	In/Out	Bit Width	Description
PLLFN	In	1	Reference Clock Input. It has to be 13.00MHz to 20MHz with +/- 10% duty.
PLLDIV[2:0]	In	3	System clock frequency select. System Clock = PLLFN * N. "00" : N=1.0. "01" : N=1.5. "10" : N=2.0 "11" : N=2.5.
PLLAVD	In	1	Analog PLL Power(VDD).
PLLAVS	In	1	Analog PLL Ground(VSS).

Table 3. Host Interface

Signal Name	In/Out	Bit Width	Description
/HCS	In	1	Chip enable input (low active). "0" : Chip select. "1" : Non operation.
/HWR	In	1	Write strobe (low active). "0" : Write operation. "1" : Non operation.
/HRD	In	1	Read Strobe (low active). "0" : Read operation. "1" : Non operation.
HADDR[6:0]	In	7	Address signal.
HDAT[15:0]	In/Out	16	Data signal.
HWAIT	Out	1	Bus wait signal (low active). "0" : Wait. "1" : Non wait.
HINT	Out	1	Interrupt signal (high active). "0" : Non operation. "1" : Interrupt Operation.

Table 4 Video Display Interface

Signal Name	In/Out	Bit Width	Description
DISPCLK	In	1	Clock signal from display.
/DISPHSYNC	In	1	HSYNC signal from display.
/DISPVSYNC	In	1	VSYNC signal form display.
/DISPBLK	Out	1	Blanking signal to display.
DISPPIXEL	Out	8	Luminance (Y) and chrominance (Cb,Cr) signal output.

Table 5 Test Control Signal

Signal Name	In/Out	Bit Width	Description
TGCLK	In	1	Test terminal. Please connect to Vss.
TSMODE	In	1	Test terminal. Please connect to Vss.
TDBISTEN	In	1	Test terminal. Please connect to Vss.
TREOUT	Out	1	Test terminal. Please connect to open.
TDTMB	In	1	Test terminal. Please connect to Vss.
TDTCLK	In	1	Test terminal. Please connect to Vss.
TEST[2:0]	In	3	Test terminal. Please connect to Vss.

Table 6 Power Supply and GND

Signal Name	In/Out	Bit Width	Description
Vss			GND
Vdds			3.3V Vdd
Vdd2			2.5V Vdd

3. Interface Specifications

3.1 Host Interface

An external host CPU can access to TC35274 via a host interface. The access timing of a read, a write, and an interrupt operation are explained below. The host interface has two access modes; handshake access mode and synchronized access mode.

3.1.1 Handshake access mode

In this mode, the host CPU has to finish an access operation after a waiting signal (/HWAIT) becomes high.

Fig.3 shows the timing diagram of a read operation. A read access starts by asserting both a chip select signal (/HCS) and a read signal (/RD) (timing (a)). At this timing, /HWAIT becomes low. When the read data are ready, /HWAIT becomes high (timing (b)). The host CPU gets the read data and finishes the read operation by negating both /HCS and /HRD (timing (c)).

Fig.4 shows the timing diagram of a write operation. A write access starts by asserting both /HCS and a write signal (/WR) (timing (a)). At this timing, /HWAIT becomes low. When TC35274 gets the write data, /HWAIT becomes high (timing (b)). After that, the host CPU finishes the write operation by negating both /HCS and /HWR (timing (c)).

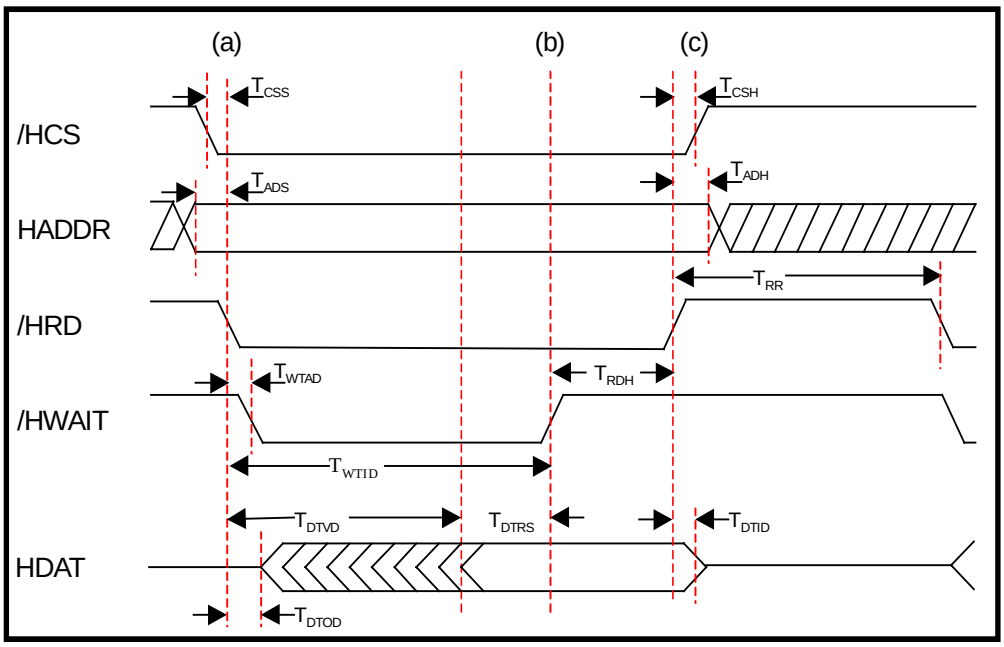

Fig. 3 Read Operation in handshake mode

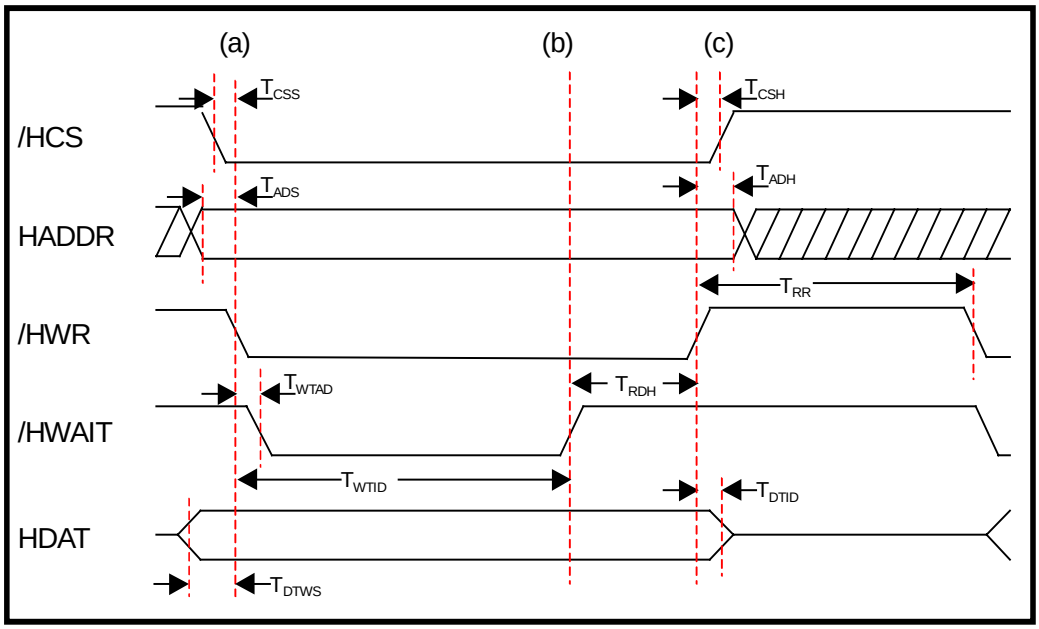

Fig. 4 Write Operation in handshake mode

3.1.2 Synchronized access mode

In this mode, a host CPU accomplishs an access to TC35274 in the specified period without a handshake. However, if the host CPU accesses to the embedded DRAM in TC35274, it has to check whether the next access is available or not by checking a status register at every 8 accesses.

Fig.5 shows the timing diagram of a read operation. A read access starts by asserting both a chip select signal (/HCS) and a read signal (/RD) (timing (a)). After the specified cycles indicated as Tacs, the host CPU gets the read data and finishes the read operation by negating both /HCS and /HRD (timing (b)).

Fig.6 shows the timing diagram of a write operation. A write access starts by asserting both /HCS and a write signal (/WR) (timing (a)). After the specified cycles, the host CPU finishes the write operation by negating both /HCS and /HWR (timing (b)).

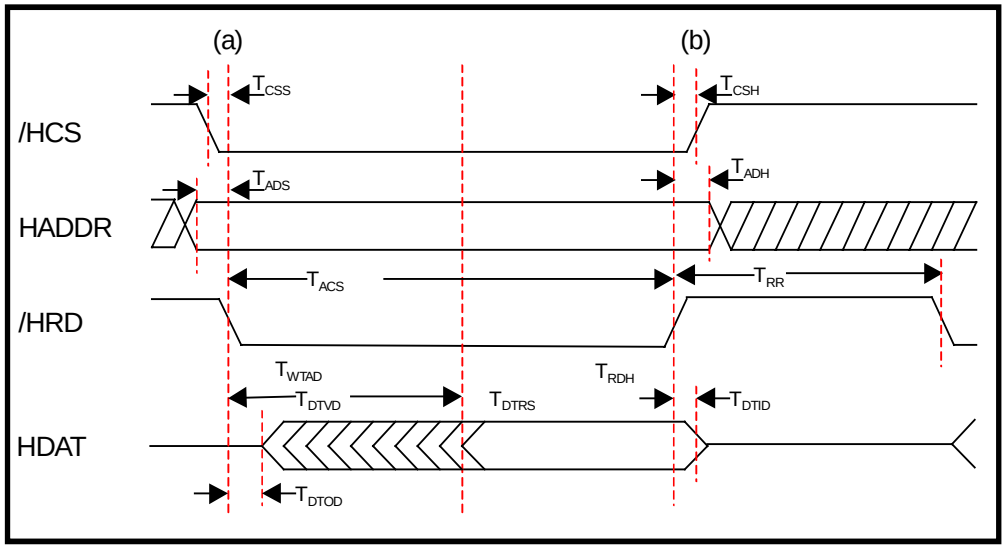

Fig.5 Read Operation in Synchronization mode

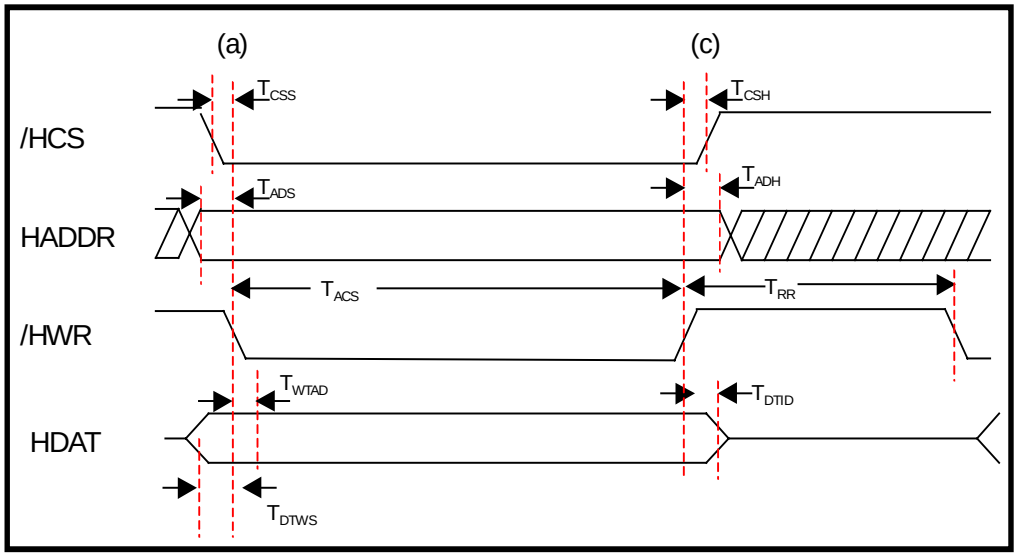

Fig.6 Write Operation in Synchronization Mode

3.1.3 Interrupt

An interrupt to the external host CPU is performed as follows.

(a) HINT Active

When an interrupt is requested by TC35274, HINT becomes high (timing (a)).

(b) Clear HINT

The host CPU detects the interrupt request by HINT. The CPU also detects the interrupt causes by reading an interrupt status register in the host interface of TC35274. When the CPU reads the register at the timing (b), The CPU detects the interrupt causes occurring during the timing (a) and (b). HINT is cleared when the CPU reads the interrupt status register.

(c) Multiple Interrupt

Even if another interrupt is requested during the timing (b) and (c), The assertion of HINT is suspended to the timing (c).

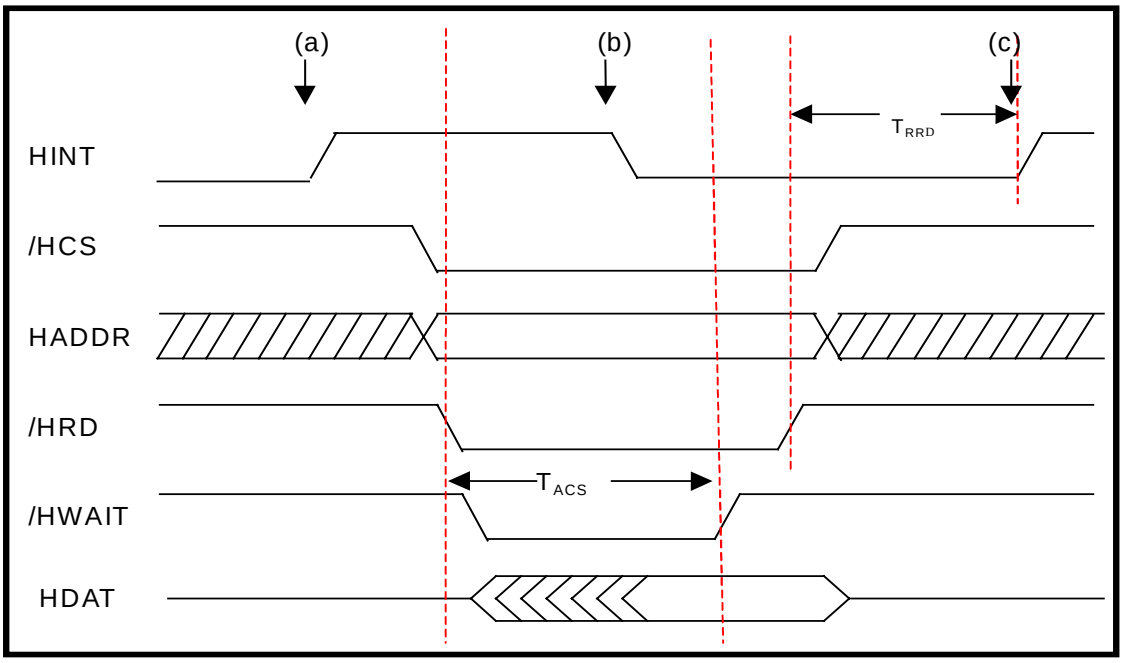

Fig. 7 Interrupt Operation

Table 7 Host Interface Timing

Parameters	Description	Min	Max	Unit
T_{CSS}	Setup time of HCS.	0.0		ns
T_{CSH}	Hold time of HCS.	0.0		ns
T_{ADS}	Setup time of Address.	0.0		ns
T_{ADH}	Hold time of Address.	0.0		ns
T_{WTAD}	Delay time of /HWAIT for /HRD or /HWR.		15.0	ns
T_{WTID}	Access time in handshake access mode.*	T_{SYSCLK}*3	T_{SYSCLK}*100	ns
T_{ACS}	Access time in synchronized access mode.	T_{SYSCLK}*3		ns
T_{ACID}	Delay time of HACK		15.0	ns
T_{DTOD}	Delay time of Data.		15.0	ns
T_{DTVD}	Data hold time.	T_{SYSCLK}*2	T_{SYSCLK}*99	ns
T_{DTRS}	Read data setup time.	T_{SYSCLK}*1		ns
T_{DTwS}	Write data setup time.	0.0		ns
t_{DTID}	Data hold time.		15.0	ns
T_{RDH}	Hold time of /HRD.	0.0		ns
T_{RR}	Recovery time of /HRD or /HWR	T_{SYSCLK}*3		ns

* T_{SYSCLK} means the cycle time of TC35274 internal system clock.

* Access to internal DRAM requires Tsysclk*100 (ns) in a worst case. As for the others accesses, it takes 3 cycles of the internal system clock.

3.4 Video Display Interface

The video display interface outputs image data with YCbCr 4:2:2 8-bit digital format. An external LCD controller is required to connect LCD.

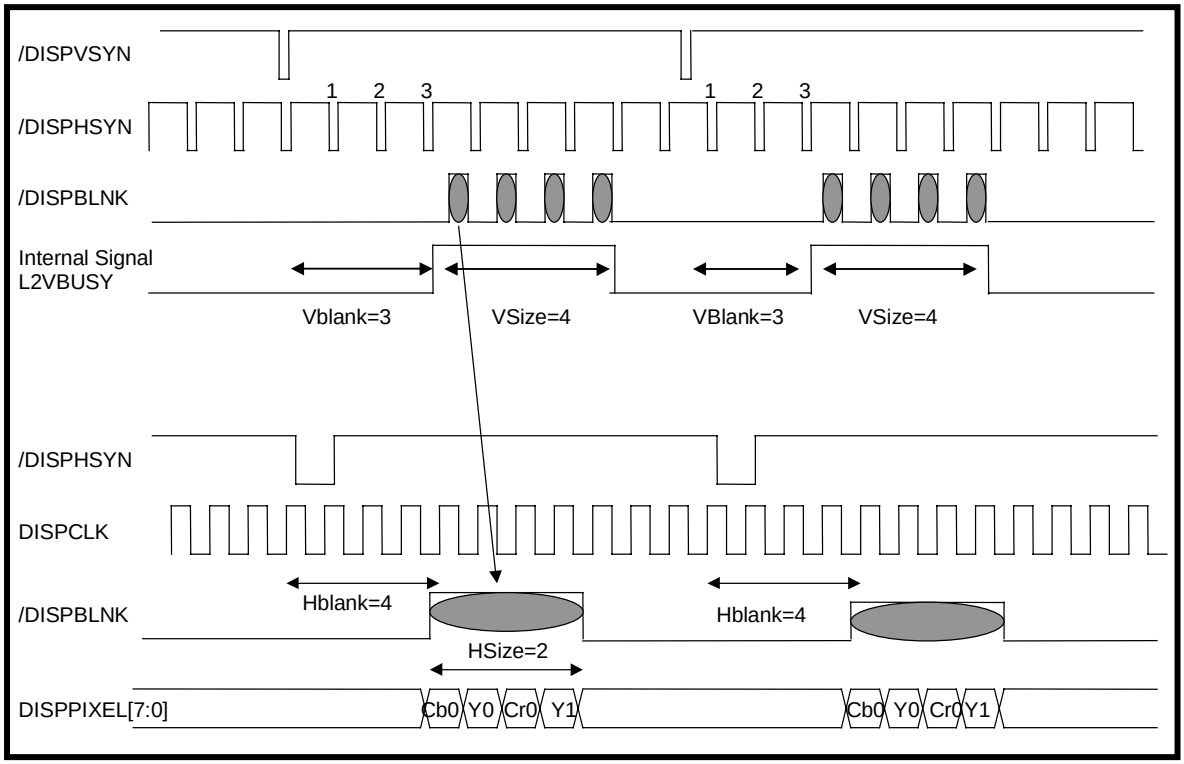

Fig. 8 Timing Diagram of Display Interface.

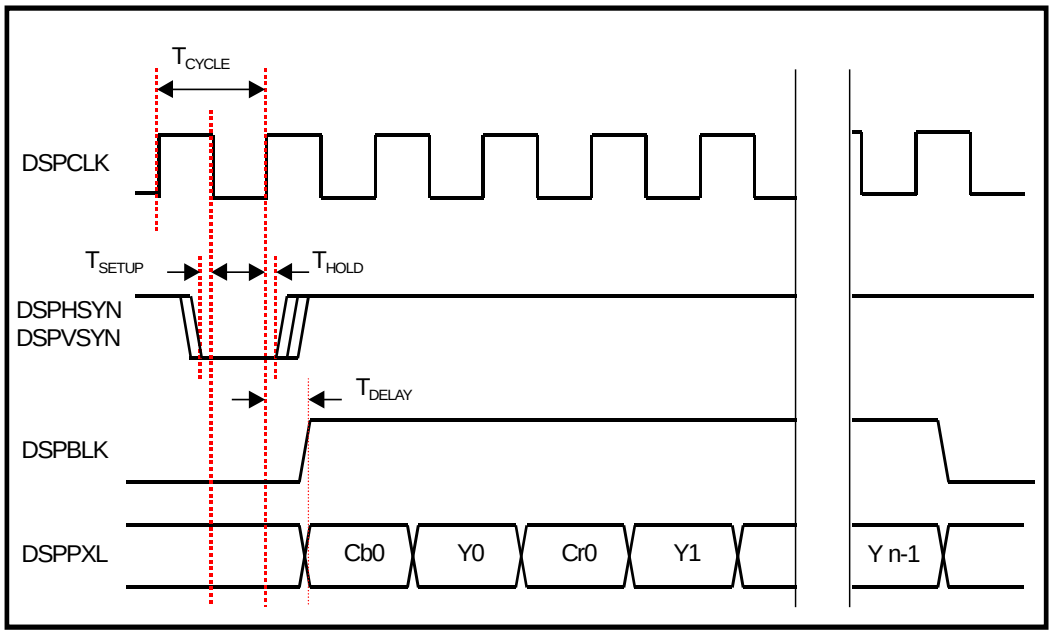

Fig. 9 Detail Timing Diagram of Display Interface.

Table 8 Display Interface Timing

Parameter	Description	Min	Max	Unit
T_{CYCLE}	Cycle time of DISPCLK	100		ns
T_{SETUP}	Setup time of DISPHSYN and DISPVSYN	2		ns
T_{HOLD}	Hold time DISPHSYN and DISPVSYN	2		ns
T_{DELAY}	Delay time of DISPBLK and DISPPXL		(T_{SYSCLK}*3)+15	ns

* When system clock is 40MHz, DSPCLK has to be less than 10MHz.

4. Electric Specifications

4.1 TBD.