MX275

MX·COM, INC.

DATA BULLETIN

February 1994

Low Voltage *Pvt* SQUELCH™ CTCSS Encoder/Decoder

Features

- MX•COM MiXed SIGNAL CMOS
- PRIVATE/CLEAR CAPABILITY
- ON-CHIP TX AUDIO PRE-/DE-EMPHASIS
- ALTERNATIVE TO CTCSS "PARTY LINE"
- LOW VOLTAGE
- EXCEEDS TIA/EIA-603 LAND MOBILE RADIO STANDARD

SIX SIGMA BASED

Applications

- MOBILE RADIOS
- COMMUNITY REPEATERS
- TELEPHONE/RADIO INTERCONNECT SYSTEMS
- SPORT RADIOS
- SERVES 2- and 3-CELL APPLICATIONS

MX275LH
24-lead PLCC

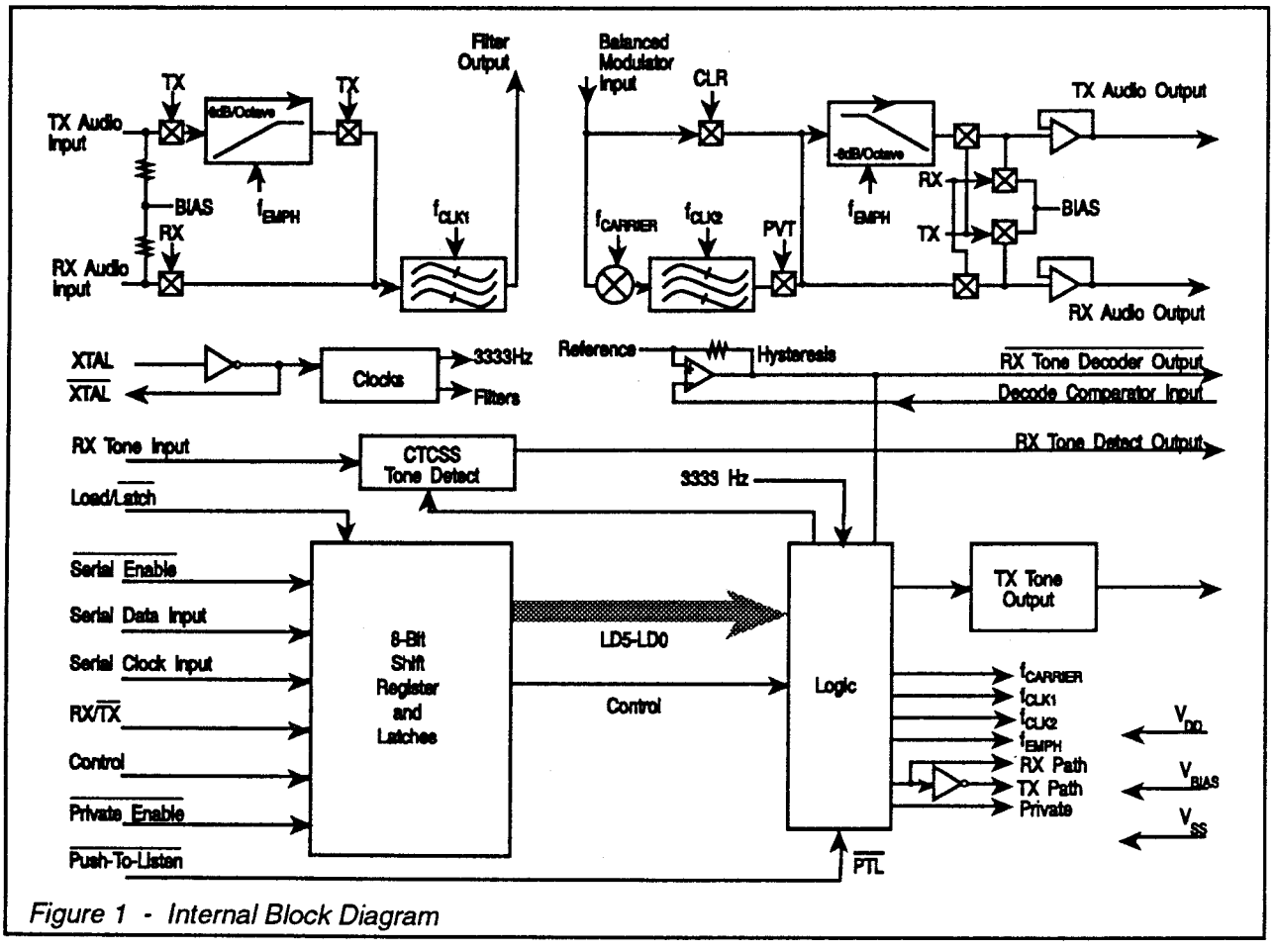


Figure 1 - Internal Block Diagram

Description

The MX275 is a CMOS LSI combination of a CTCSS encoder/decoder and a simple (frequency inversion) speech scrambler. CTCSS (Continuous Tone-Controlled Squelch System) multiplexes a sub-audible tone (1 of 38) with speech. This is performed continuously in 2-Way Radio systems -- as a means of segregating the traffic of co-channel talk groups. The MX275 integrated circuit carries this process an extra step called *Pvt* SQUELCH™. This uses the detection of the CTCSS tone to enable the clear recovery of scrambled speech. As talk groups are assigned unique CTCSS tones, their voice traffic is rendered intelligible only among its own members. The audio monitored by co-channel users with different talk group tones is unintelligible.

The MX275 Features

1) Serial control, but with parallel PTT, PTL and PVT/CLR options.
2) Squelch Tail Elimination facilitated by 180° reverse burst option.
3) On-chip speech filters aid FDM (CTCSS+audio) multiplexing.
4) *Pvt* SQUELCH™ operation.
5) Grants to the 2-Way Radio protection under the ECPA*.

Why not Busy Channel Lock Out? (sometimes called Privacy Lock Out)

While BCLO also affords co-channel users privacy, its implementation is at the discretion of the receiver, not the sender. BCLO prevents inadvertant PTT keying and impolite disruptions by co-channel users who fail to monitor before transmitting. But BCLO provides no protection against scanners nor under the ECPA. BCLO assures politeness, *Pvt* SQUELCH™ privacy.

Application Notes

Pre- and de-emphasis (6dB/octave) filters are included on-chip in the transmit path, so that the use of this device will produce natural sounding audio (clear or private modes) when installed in modern radio communication transceivers, with or without existing audio processing circuitry. The recommended layout is shown in block form below.

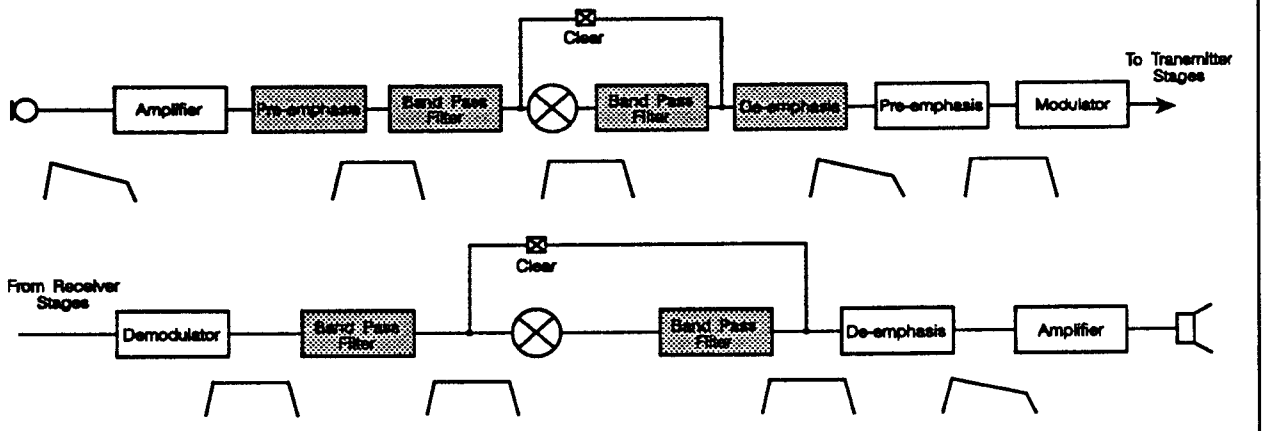


Figure 2 - The MX275's Transmit and Receive Paths

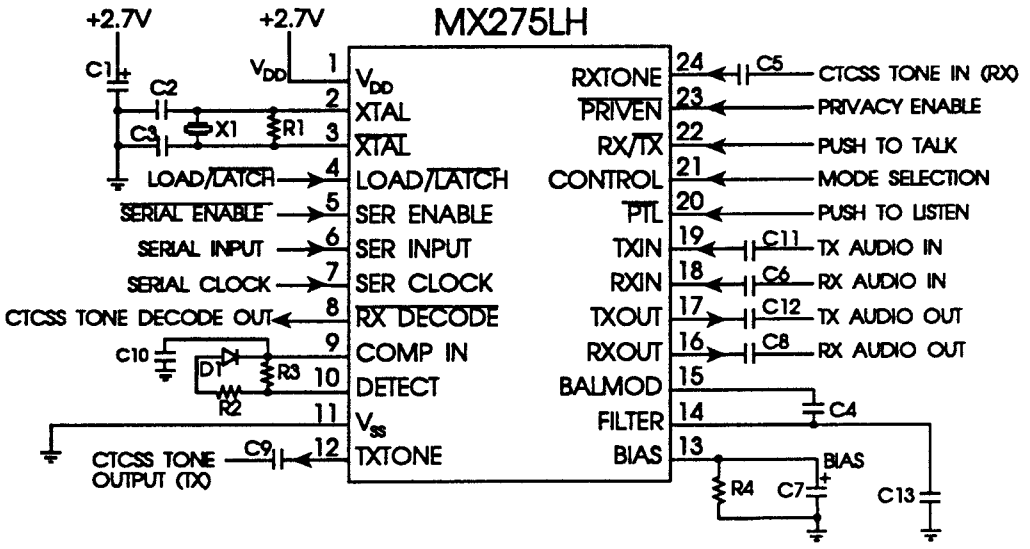
** Electronic Communications Privacy Act of 1986.*

Pin Function Chart

Pin	Function
1	V_{DD}: The positive 2.7V supply pin.
2	**XTAL/CLOCK**: This is the input to the clock oscillator inverter. An external 4 MHz xtal or clock input should be applied to this pin.
3	**$\overline{\text{XTAL}}$**: This is the 4 MHz output of the clock oscillator inverter.
4	**LOAD/$\overline{\text{LATCH}}$**: This input controls the eight input latches: RX/$\overline{\text{TX}}$, $\overline{\text{Private Enable}}$, and D0-D5, as detailed in Table 2(a). Alternatively, the RX/$\overline{\text{TX}}$ and $\overline{\text{Private Enable}}$ inputs can be addressed separately by setting the Load/Latch and Control inputs as shown in Table 2(b). 1 MΩ pullup. An external pull-up or active CMOS drive is recommended.
5-7	**Programming Inputs**: These are the RX/$\overline{\text{TX}}$ tone programming and function inputs which enable the serial programming mode. With Load/Latch at logic "0" data is loaded in the following sequence: D5, D4, D3, D2, D1, D0, RX/$\overline{\text{TX}}$, $\overline{\text{Private Enable}}$. When these 8 bits have been clocked in on the rising clock edge, data is latched by strobing the Load/Latch input "0 - 1 - 0" (See Figure 4). Pin 5 = $\overline{\text{Serial Enable}}$ Pin 6 = Serial Data Input Pin 7 = Serial Clock Input
8	**$\overline{\text{RX TONE DECODE}}$**: The gated output of the decode comparator. In RX, a logic "0" indicates a valid CTCSS tone decode condition, or the presence of NOTONE programming. A logic "0" enables the RX audio path. In TX this output is held at logic "1."
9	**DECODE COMPARATOR**: The voltage level at this pin is compared internally with a switched $^1/_3$-$^2/_3$ V_{DD} reference that provides hysteresis. An input level exceeding the reference results in a logic "0" at the RX Tone Decode output. This input should be externally connected to the RX Tone Detect output via external integration components C_7, R_2, R_3, and D_1 (see Figure 3).
10	**RX TONE DETECT**: In RX, this pin outputs a logical "1" when a valid programmed CTCSS tone is received at the RX TONE INPUT. This input should be externally connected to the Decode Comparator input via external integration components C_{10}, R_2, R_3, and D_1 (see Figure 3).
11	V_{SS}: The negative supply pin (ground).
12	**TX TONE OUTPUT**: The buffered CTCSS sinewave tone output appears on this pin. In TX mode, the tone frequency is selected by program code (see Table 1); if NOTONE is programmed, the output is at V_{BIAS}-0.7V. In RX mode, the output goes open circuit. This is an emitter follower output with an internal 10 kΩ load.
13	**BIAS**: This pin is set internally to approximately $V_{DD}/2$. It must be externally connected to V_{SS} using capacitor C_7 and resistor R_4. See Figure 3.
14	**FILTER OUTPUT**: This is the output of the Input Audio Bandpass Filter. It must be A.C. coupled to the Balanced Modulator Input via capacitor C_4. See Figure 3.
15	**BALANCED MODULATOR INPUT**: This is the input to the balanced modulator. It must be A.C. coupled to the Filter Output via capacitor C_4. See Figure 3.

Pin Function Chart

Pin	Function
16	**RX AUDIO OUTPUT:** Outputs the received audio from a buffered output stage and is held at V_{BIAS} when in TX. Capacitive loads exceeding 15pF should be avoided.
17	**TX AUDIO OUTPUT:** Outputs the transmitted audio in TX. In RX, this pin is held at V_{BIAS}. Capacitive loads exceeding 15pF should be avoided.
18	**RX AUDIO INPUT**: The audio input for the RX mode. Input signals should be AC coupled via external capacitor C_6. See Figure 3.
19	**TX AUDIO INPUT:** This is the TX Audio voice input. Signals should be AC coupled via external capacitor C_{11}. See Figure 3.
20	**$\overline{\text{PTL}}$**: The "press to listen" function input. In RX mode, a logic "0" enables the RX Audio Output directly, overriding tone squelch but not intercepting a private conversation; in TX mode, a logic "0" reverses the phase of the TX Tone Output for "squelch tail" reduction (see Table 2).
21	**CONTROL:** This input, together with Load/$\overline{\text{Latch}}$, selects the operational mode of the RX/$\overline{\text{TX}}$ and $\overline{\text{Private Enable}}$ functions. See Table 2(b).
22	**RX/$\overline{\text{TX}}$**: This input selects the RX or TX mode (RX = 1, TX = 0). See Table 2.
23	**$\overline{\text{PRIVATE ENABLE}}$**: This input selects either Private or Clear mode (Clear = 1, Private = 0), and is loaded as described in Table 2. This input has an internal 1 MΩ pullup resistor.
24	**RX TONE INPUT**: This is the received audio input to the on-chip CTCSS tone decoder. It should be A.C. coupled via capacitor C_5.



COMPONENT VALUES

R1 = 1MΩ	C1 = 1µF	C6 = 0.1µF	C11 = 0.1µF
R2 = 560kΩ	C2 = 33pF	C7 = 1µF	C12 = 0.1µF
R3 = 820kΩ	C3 = 33pF	C8 = 0.1µF	C13 = 0.001µF
R4 = 560kΩ	C4 = 0.1µF	C9 = 0.1µF	D1 = small signal
X1 = 4MHz	C5 = 0.1µF	C10 = 0.1µF	

Tolerances: Resistors: ±5% Capacitors: ±10%

XTAL: At cut, fundamental, parallel resonant 20pF load capacitance, tolerance 100 PPM.

Figure 3 - External Component Connections

CTCSS PROGRAMMING TABLE

TIA/EIA-603 Nominal Frequency(Hz)	Frequency (Hz)	Δf_o (%)	Programming Inputs D5	D4	D3	D2	D1	D0	HEX
67.0	67.05	+0.07	1	1	1	1	1	1	3F
71.9	71.9	0	0	1	1	1	1	1	1F
74.4	74.35	-0.07	1	1	1	1	1	0	3E
77.0	76.96	-0.5	0	0	1	1	1	1	0F
79.7	79.77	+0.09	1	1	1	1	0	1	3D
82.5	82.59	+0.1	0	1	1	1	1	0	1E
85.4	85.38	-0.2	1	1	1	1	0	0	3C
88.5	88.61	+0.13	0	0	1	1	1	0	0E
91.5	91.58	+0.09	1	1	1	0	1	1	3B
94.8	94.76	-0.04	0	1	1	1	0	1	1D
97.4	97.29	-0.11	1	1	1	0	1	0	3A
100.0	99.96	-0.04	0	0	1	1	0	1	0D
103.5	103.43	-0.07	0	1	1	1	0	0	1C
107.2	107.15	-0.05	0	0	1	1	0	0	0C
110.9	110.77	-0.12	0	1	1	0	1	1	1B
114.8	114.64	-0.14	0	0	1	0	1	1	0B
118.8	118.8	0	0	1	1	0	1	0	1A
123.0	122.8	-0.17	0	0	1	0	1	0	0A
127.3	127.08	-0.17	0	1	1	0	0	1	19
131.8	131.67	-0.10	0	0	1	0	0	1	09
136.5	136.61	+0.08	0	1	1	0	0	0	18
141.3	141.32	+0.02	0	0	1	0	0	0	08
146.2	146.37	+0.12	0	1	0	1	1	1	17
151.4	151.09	-0.2	0	0	0	1	1	1	07
156.7	156.88	+0.11	0	1	0	1	1	0	16
162.2	162.31	+0.07	0	0	0	1	1	0	06
167.9	168.14	+0.14	0	1	0	1	0	1	15
173.8	173.48	-0.19	0	0	0	1	0	1	05
179.9	180.15	+0.14	0	1	0	1	0	0	14
186.2	186.29	+0.05	0	0	0	1	0	0	04
192.8	192.86	+0.03	0	1	0	0	1	1	13
203.5	203.65	+0.07	0	0	0	0	1	1	03
210.7	210.17	-0.25	0	1	0	0	1	0	12
218.1	218.58	+0.22	0	0	0	0	1	0	02
225.7	226.12	+0.18	0	1	0	0	0	1	11
233.6	234.19	+0.25	0	0	0	0	0	1	01
241.8	241.08	-0.30	0	1	0	0	0	0	10
250.3	250.28	-0.01	0	0	0	0	0	0	00
Notone			1	1	0	0	0	0	30

Table 1 - CTCSS Programming Chart

(A)Explanation of Load/$\overline{\text{Latch}}$ function

Load Configuration	Load/$\overline{\text{Latch}}$	Result
Data loading	0	No change while serial data train is loaded
Data loaded	0 - 1 - 0	Loaded serial data is latched

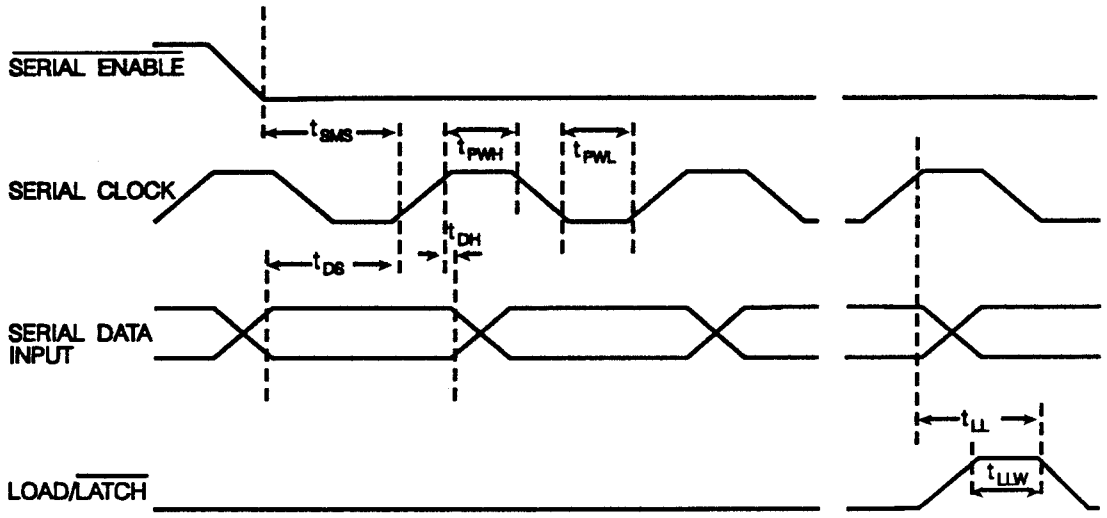
(B) Explanation of Control Input

Load Configuration	Load/$\overline{\text{Latch}}$	Control	RX/$\overline{\text{TX}}$, $\overline{\text{Private Enable}}$
Serial Control Input	0 - 1 - 0	0	Serial Load
Serial Control Input	X	1	Transparent

Notes: "0 - 1 - 0" is a strobe pulse as shown in Figures 4 and 5 (Timing).
"X" denotes any logical state.

Table 2 - Load/$\overline{\text{Latch}}$ and Control Functions

Control instructions are input to the MX275 by serial means, using Data Inputs and Load/Latch as shown below.



	Min.	Typ.	Max.	Unit
Serial Mode Enable Set Up Time (t_{SMS})	250	-	-	ns
Clock "High" Pulse Width (t_{PWH})	250	-	-	ns
Clock "Low" Pulse Width (t_{PWL})	250	-	-	ns
Data Set Up Time (t_{DS})	150	-	-	ns
Data Hold Time (t_{DH})	50	-	-	ns
Load/Latch Set Up Time (t_{LL})	250	-	-	ns
Load/Latch Pulse Width (t_{LLW})	150	-	-	ns

Figure 4 - Serial Load Timing (see notes 1 and 9 in Specification section)

D0-D5	NOTONE	RX/TX	PRIVATE ENABLE	PTL	RXTONE DETECT	RXTONE DECODER	TONE OUTPUT	TONE PHASE	TX PATH	RX PATH	PATH STATE	TONE
TONE	1	0	0	1	0	1	YES	0°	OPEN	BIAS	INV	TX, TONE
TONE	1	0	0	0	0	1	YES	180°	OPEN	BIAS	INV	TX, TONE REV
NOTONE	0	0	0	X	0	1	BIAS	X	OPEN	BIAS	CLR	TX, NOTONE
TONE	1	1	0	1	0	1	BIAS	X	BIAS	BIAS	X	INCOMPATIBLE
TONE	1	1	0	0	0	1	BIAS	X	BIAS	OPEN	CLR	INCOMPATIBLE
TONE	1	1	0	X	1	0	BIAS	X	BIAS	OPEN	INV	COMPATIBLE
NOTONE	0	1	0	X	X	0	BIAS	X	BIAS	OPEN	CLR	RX, NOTONE
TONE	1	0	1	1	0	1	YES	0°	OPEN	BIAS	CLR	TX, TONE
TONE	1	0	1	0	0	1	YES	180°	OPEN	BIAS	CLR	TX, TONE REV
NOTONE	0	0	1	X	0	1	BIAS	X	OPEN	BIAS	CLR	TX, NOTONE
TONE	1	1	1	1	0	1	BIAS	X	BIAS	BIAS	X	INCOMPATIBLE
TONE	1	1	1	0	0	1	BIAS	X	BIAS	OPEN	CLR	INCOMPATIBLE
TONE	1	1	1	X	1	0	BIAS	X	BIAS	OPEN	CLR	COMPATIBLE
NOTONE	0	1	1	X	X	0	BIAS	X	BIAS	OPEN	CLR	RX, NOTONE

ALGEBRAIC FUNCTIONS:
RX PATH ON = RX* (PTL + RX TONE DECODER)
CLEAR PATH = NOTONE + PRIVATE ENABLE + (P* H* RX TONE DECODER)
NOTONE (D0-D5) = 000011
CARRIER FREQUENCY = 3333Hz DURING INVERTED PATH(TX or RX)

NOTES: 1. The Pre- and De-emphasis circuits remain in the transmit path in both Clear and Invert modes.
2. Power remains applied to the CTCSS tone decoder at all times.
3. During Clear operation the carrier frequency is turned off to reduce spurious emissions.

Table 4 - Functions and Outputs

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 4.0 V
Input Voltage at any pin	-0.3V to (V_{DD} + 0.3 V)
Sink/Source Current	
(Supply pins)	±30 mA
(Other pins)	±20 mA
Total Device Dissipation	
@ T_{AMB} 25°C	800 mW max.
Derating	10 mW/°C
Operating Temperature	-15°C to +60°C
Storage Temperature	-55°C to +125°C

Operating Limits

Measured using the standard test circuit (Fig. 3) and under the following conditions unless otherwise noted.

V_{DD}	2.7V
T_{AMB}	25°C
Xtal/Clock f_0	4.0 MHz
Audio level 0dB ref	250 mVrms

Composite input signal = 300 mVrms, 1 kHz tone in, 75 mVrms (6 kHz band limited) gaussian noise, and a 30 mVrms CTCSS tone.

Characteristics		Note	Min.	Typ.	Max.	Unit
Static Values						
Supply Voltage		2.2	2.7	3.2	V	
Supply Current	TX		-	4.0	10.0	mA
	RX		-	3.0	4.6	mA
Impedances	Speech In	1	87	155	223	kΩ
	Speech Out	1,8	500	850	1200	Ω
	Tone In	1	410	540	664	kΩ
	Tone Out	1,2,8	616	1800	2966	Ω
I/O Logic	Input "1"	1,9,10	70%	-	-	V_{DD}
	Input "0"	1	-	-	30%	V_{DD}
	Output "1" (source 0.1mA)	1	80%	-	-	V_{DD}
	Output "0" (sink 0.1mA)	1	-	-	20%	V_{DD}
Serial Clock		1	250	-	-	ns
Dynamic Values						
CTCSS Encode						
Tone Output Level		2	350	400	460	mVrms
Tone Accuracy			-0.3	f_o	0.3	$\%f_o$
Distortion			-	3.5	5	%
T-T Level D			-	13	47	mVrms
Risetime to 90%	≥100Hz	1	-	10	50	ms
180°Phase Reversal	90% ≥100Hz	1	-	10	50	ms
CTCSS Decode						
Signal Threshold		4	30	10	-	mVrms
Must Decode B/E			-0.5	±2	0.5	$\%f_o$

Characteristics		Note	Min.	Typ.	Max.	Unit
CTCSS Decode...						
Response Time	>100 Hz	4,5	-	170	250	ms
Deresponse Time	>100 Hz	4	-	150	250	ms
Don't Decode B/E	Adjacent Tone		0.5	±1	-0.5	%

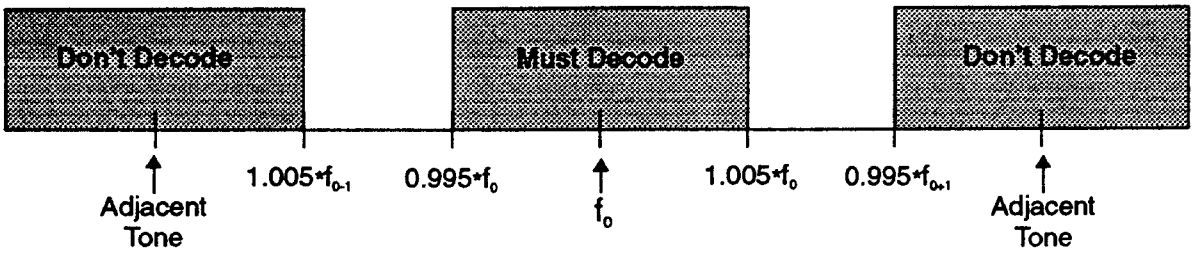


Figure 5 - Do Not Decode Band-edge Adjacent Tone

Speech Filter	**TX/RX**					
Passband		3	300	-	3000	Hz
Passband Gain		3,7	-1.5	0	1	dB
Ripple		3,7	-3	-	1	dB
Distortion	Clear	3	-	6	10	%
CTCSS Rejection	f_{in}<250Hz	3	25	32		dB
AC/SC Noise		6	-	2.5	7.9	mVrms
Scrambling	**TX/RX**					
Inversion Carrier			3329.7	3333	3336.3	Hz
Carrier Breakthrough		1,3	-	-58	-46	dB
Baseband Breakthrough		1,3	-	-54	-42	dB
Carrier Rejection	f_{in}>3333Hz	3	20	-	-	dB
Baseband Reject	f_{in}>3633Hz	3	45	-	-	dB

NOTES

1. Untested parameter — derived by statistical characterization.
2. An emitter follower output.
3. With reference to an input signal of 1 kHz @ 0dB.
4. Composite signal.
5. f_o > 100 Hz, (for 100Hz > f_o > 67Hz: t = [100/f_o(Hz)] x 250ms), per ANSI/TIA/EIA-603.
6. AC Short-Circuit input, speech path enabled.
7. <6dB per octave roll-off, <500 Hz >2500 Hz per ANSI/TIA/EIA-603
8. Capacitive loads not to exceed 15pf.
9. External Pull-Up or active CMOS drive recommended.
10. Includes LOAD/LATCH don't load immunity testing.

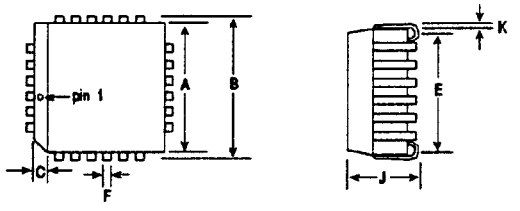
Package Information

The MX275 24-lead Plastic Leaded Chip Carrier package is shown in Figure 6. For identification purposes it has an ident spot adjacent to pin 1 and a chamfered corner between pins 3 & 4.

Handling Precautions

The MX275 is a CMOS LSI circuit which includes input protection. However, precautions should be taken to prevent static discharges which may cause damage.

Figure 6 - MX275LH PLCC-24



Package Tolerances

Dimension in.(mm)	Min.	Max.
A	.382 (9.70)	.410 (10.40)
B	.417 (10.60)	.435 (11.05)
C	.045 (1.15)x45°	typical
D	.050 (1.27)	typical
E	.366 (9.30)	typical
F	.018 (0.45)	.022 (0.55)
H	.250 (6.35)	typical
J	.128 (3.25)	.146 (3.70)
K	.007 (0.17)	.011 (0.27)

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CAUTION
MOS Device. May be damaged by static discharge. Observe handling precautions.

Specifications are subject to change.

Document No. 20480090.013

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COMMUNICATION MICROSYSTEMS

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CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CML Product Data

In the process of creating a more global image, the three standard product semiconductor companies of CML Microsystems Plc *(Consumer Microcircuits Limited (UK), MX-COM, Inc (USA) and CML Microcircuits (Singapore) Pte Ltd)* have undergone name changes and, whilst maintaining their separate new names *(CML Microcircuits (UK) Ltd, CML Microcircuits (USA) Inc and CML Microcircuits (Singapore) Pte Ltd*), now operate under the single title **CML Microcircuits**.
These companies are all 100% owned operating companies of the CML Microsystems Plc Group and these changes are purely changes of name and do not change any underlying legal entities and hence will have no effect on any agreements or contacts currently in force.

CML Microcircuits Product Prefix Codes

Until the latter part of 1996, the differentiator between products manufactured and sold from MXCOM, Inc. and Consumer Microcircuits Limited were denoted by the prefixes MX and FX respectively. These products use the same silicon etc. and today still carry the same prefixes. In the latter part of 1996, both companies adopted the common prefix: CMX.

This notification is relevant product information to which it is attached.

CML Microcircuits (USA) [formerly MX-COM, Inc.] Product Textual Marking

On CML Microcircuits (USA) products, the **'MX-COM'** textual logo is being replaced by a **'CML'** textual logo.

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