DOUBLE DATA RATE (DDR) SDRAM

MT46V16M8 – 4 Meg x 8 x 4 banks

For the latest data sheet revisions, please refer to the Micron Web site: www.micron.com/dramds

FEATURES

- 200 MHz Clock, 400 Mb/s/p data rate
- V_{DD} = +2.65V ±0.10V
- $V_{DD}Q$ = +2.65V ±0.10V
- Bidirectional data strobe (DQS) transmitted/ received with data, i.e., source-synchronous data capture
- Internal, pipelined double-data-rate (DDR) architecture; two data accesses per clock cycle
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- DLL to align DQ and DQS transitions with CK
- Four internal banks for concurrent operation
- Data mask (DM) for masking write data
- Programmable burst lengths: 2, 4, or 8
- Concurrent Auto Precharge option supported
- Auto Refresh and Self Refresh Modes
- ^{t}RAS lockout (^{t}RAP = ^{t}RCD)

OPTIONS — PART NUMBER

- Configuration
  16 Meg x 8 (4 Meg x 8 x 4 banks) — 16M8
- Plastic Package
  66-Pin TSOP (400mil with 0.65mm pin pitch) — TG
- Timing - Cycle Time
  5ns @ CL = 3(1) — -5
- Self Refresh
  Standard — none

NOTE: 1. Supports modules with 3-4-4 timing

GENERAL DESCRIPTION

The DDR400 SDRAM is a high-speed CMOS, dynamic random-access memory that operates at a frequency of 200 MHz (^{t}CK=5ns) with a peak data transfer rate of 400Mb/s. DDR400 continues to use the JEDEC standard SSTL_2 interface and the *2n*-prefetch architecture.

The standard DDR200/DDR266 data sheets also pertain to the DDR400 device and should be referenced for a complete description of DDR SDRAM functionality and operating modes. However, to meet the faster DDR400 operating frequencies, some of the AC timing parameters, DC levels and operating temperatures are slightly tighter. This addendum data sheet will concentrate on the key differences required to support the enhanced speeds.

The Micron 128Mb data sheet provides full specifications and functionality unless specified herein.

CONFIGURATION

Architecture	16 Meg x 8
Configuration	4 Meg x 8 x 4 banks
Refresh Count	4K
Row Addressing	4K (A0–A11)
Bank Addressing	4 (BA0, BA1)
Column Addressing	1K (A0–A9)

KEY TIMING PARAMETERS

SPEED GRADE	CLOCK RATE CL = 3[1]	DATA-OUT WINDOW[2]	ACCESS WINDOW	DQS-DQ SKEW
-5	200 MHz	2.15ns	±0.50ns	+0.35ns

NOTE: 1. CL = CAS (Read) Latency
2. With a 50/50 clock duty cycle

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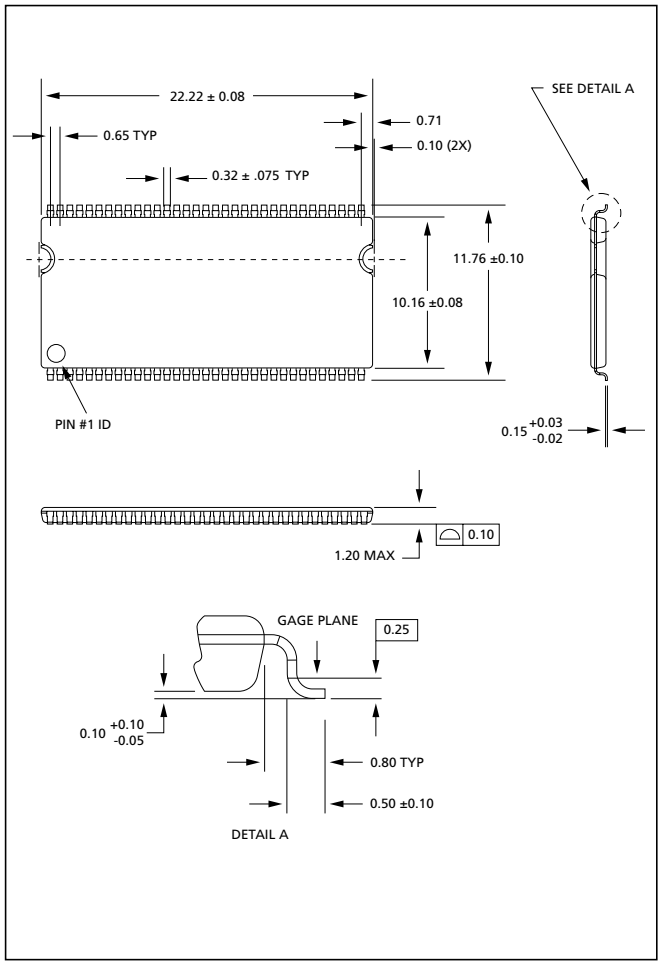
‡THIS DATA SHEET CONTAINS THE PRESENT DESCRIPTION OF A PRODUCT IN DEFINITION WITH NO FORMAL DESIGN IN PROGRESS.

66-PIN TSOP PACKAGE DIMENSION



66-PIN TSOP PACKAGE PIN ASSIGNMENT

(TOP VIEW)

x8					x8
VDD	1		66		VSS
DQ0	2		65		DQ7
VDDQ	3		64		VSSQ
NC	4		63		NC
DQ1	5		62		DQ6
VSSQ	6		61		VDDQ
NC	7		60		NC
DQ2	8		59		DQ5
VDDQ	9		58		VSSQ
NC	10		57		NC
DQ3	11		56		DQ4
VSSQ	12		55		VDDQ
NC	13		54		NC
NC	14		53		NC
VDDQ	15		52		VSSQ
NC	16		51		DQS
NC	17		50		DNU
VDD	18		49		VREF
DNU	19		48		VSS
NC	20		47		DM
WE#	21		46		CK#
CAS#	22		45		CK
RAS#	23		44		CKE
CS#	24		43		NC
NC	25		42		NC
BA0	26		41		A11
BA1	27		40		A9
A10/AP	28		39		A8
A0	29		38		A7
A1	30		37		A6
A2	31		36		A5
A3	32		35		A4
VDD	33		34		VSS

NOTE: 1. All dimensions in millimeters.
2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.

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PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
45, 46	CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQs and DQS) is referenced to the crossings of CK and CK#.
44	CKE	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates the internal clock, input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for POWER-DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit and for disabling the outputs. CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK, CK#, and CKE) are disabled during POWER-DOWN. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_2 input but will detect an LVCMOS LOW level after V_{DD} is applied.
24	CS#	Input	Chip Select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
23, 22, 21	RAS#, CAS#, WE#	Input	Command Inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
47	DM	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins.
26, 27	BA0, BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
29-32 32, 35, 36 36, 38, 39 40, 29, 41	A0, A1, A2 A3, A4, A5 A6, A7, A8 A9, A10, A11	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA0, BA1) or all banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command.
2, 5, 8 11, 56, 59 62, 65	DQ0-2 DQ3-5 DQ6-7	I/O	Data Input/Output.
51	DQS	I/O	Data Strobe: Output with read data, input with write data. DQS is edge-aligned with read data, centered in write data. It is used to capture data.

(continued on next page)

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PIN DESCRIPTIONS (continued)

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
4, 7, 10, 13, 14, 16, 17, 20, 20, 25, 42, 43, 53, 54, 57, 60, 63	NC	-	No Connect: These pins should be left unconnected.
19, 50	DNU	–	Do Not Use: Must float to minimize noise on Vref
3, 9, 15, 55, 61	$V_{DD}Q$	Supply	DQ Power Supply: +2.65V ±0.10V. Isolated on the die for improved noise immunity.
6, 12, 52, 58, 64	$V_{SS}Q$	Supply	DQ Ground. Isolated on the die for improved noise immunity.
1, 18, 33	V_{DD}	Supply	Power Supply: +2.65V ±0.10V.
4, 48, 66	V_{SS}	Supply	Ground.
49	V_{REF}	Supply	SSTL_2 reference voltage.

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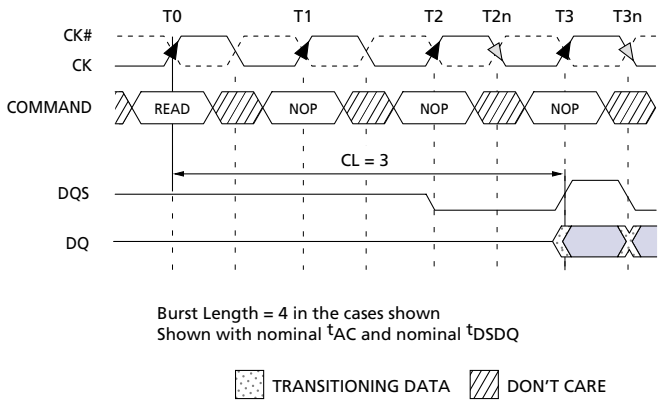
READ LATENCY

The READ latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The latency should be set to 3 clocks, as shown in the CAS Latency Diagram and Mode Register Definition Diagram.

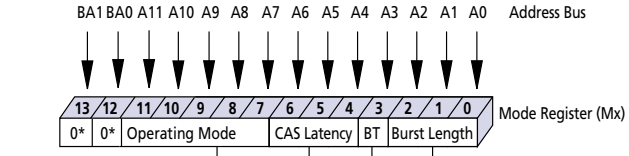
If a READ command is registered at clock edge *n*, and the latency is *m* clocks, the data will be available nominally coincident with clock edge *n* + *m*.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

CAS Latency Diagram



Mode Register Definition Diagram



* M13 and M12 (BA0 and BA1) must be "0, 0" to select the base mode register (vs. the extended mode register).

	Burst Length	
M2 M1 M0	M3 = 0	M3 = 1
0 0 0	Reserved	Reserved
0 0 1	2	2
0 1 0	4	4
0 1 1	8	8
1 0 0	Reserved	Reserved
1 0 1	Reserved	Reserved
1 1 0	Reserved	Reserved
1 1 1	Reserved	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

M6 M5 M4	CAS Latency
0 0 0	Reserved
0 0 1	Reserved
0 1 0	Reserved
0 1 1	3
1 0 0	Reserved
1 0 1	Reserved
1 1 0	Reserved
1 1 1	Reserved

M11	M10	M9	M8	M7	M6-M0	Operating Mode
0	0	0	0	0	Valid	Normal Operation
0	0	0	1	0	Valid	Normal Operation/Reset DLL
-	-	-	-	-	-	All other states reserved

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ABSOLUTE MAXIMUM RATINGS*

V_{DD} Supply Voltage Relative to V_{SS} ..... -1V to +3.6V
$V_{DD}Q$ Supply Voltage Relative to V_{SS} .... -1V to +3.6V
V_{REF} and Inputs Voltage Relative to V_{SS} .. -1V to +3.6V
I/O Pins Voltage Relative to V_{SS} . -0.5V to $V_{DD}Q$ +0.5V
Operating Temperature, T_A (ambient) .. 0°C to +50°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1–5, 16; refer to DDR200/266 data sheet for all notes)
(0°C ≤ T_A ≤ +50°C; V_{DD} = +2.65V ±0.10V, $V_{DD}Q$ = +2.65V ±0.10V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{DD}	2.55	2.75	V	36, 41
I/O Supply Voltage	$V_{DD}Q$	2.55	2.75	V	36, 41, 44
I/O Reference Voltage	V_{REF}	0.49 x $V_{DD}Q$	0.51 x $V_{DD}Q$	V	6, 44
I/O Termination Voltage (system)	V_{TT}	V_{REF} - 0.04	V_{REF} + 0.04	V	7, 44
Input High (Logic 1) Voltage	V_{IH}(DC)	V_{REF} + 0.15	V_{DD} + 0.3	V	28
Input Low (Logic 0) Voltage	V_{IL}(DC)	-0.3	V_{REF} - 0.15	V	28
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ V_{DD}, V_{REF} pin 0V ≤ V_{IN} ≤ 1.35V (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (DQs are disabled; 0V ≤ V_{OUT} ≤ $V_{DD}Q$)	I_{OZ}	-5	5	µA	
OUTPUT LEVELS: Full drive option - x8 High Current (V_{OUT} = $V_{DD}Q$-0.373V, minimum V_{REF}, minimum V_{TT})	I_{OH}	-16.8	–	mA	37, 39
Low Current (V_{OUT} = 0.373V, maximum V_{REF}, maximum V_{TT})	I_{OL}	16.8	–	mA	

AC INPUT OPERATING CONDITIONS

(Notes: 1–5, 16; refer to DDR200/266 data sheet for all notes)
(0°C ≤ T_A ≤ +50°C; V_{DD} = +2.65V ±0.10V, $V_{DD}Q$ = +2.65V ±0.10V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	V_{IH}(AC)	V_{REF} + 0.310	–	V	14, 28, 40
Input Low (Logic 0) Voltage	V_{IL}(AC)	–	V_{REF} - 0.310	V	14, 28, 40
I/O Reference Voltage	V_{REF}(AC)	0.49 x $V_{DD}Q$	0.51 x $V_{DD}Q$	V	6

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CAPACITANCE (TSOP)

(Notes: 1-5, 14-17, 33; refer to DDR200/266 data sheet for all notes)
(0°C ≤ T_A ≤ 70°C; $V_{DD}Q$ = +2.65V ±0.10V, V_{DD} = +2.65V ±0.10V)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Delta Input/Output Capacitance:					
DQs, DQS, DM	DC_{IO}	–	0.50	pF	13, 24
DQ0-DQ7	DC_{IO}	–	0.50	pF	13, 24
Delta Input Capacitance: Command and Address	$DC_{I}1$	–	0.50	pF	13, 29
Delta Input Capacitance: CK, CK#	$DC_{I}2$	–	0.25	pF	13, 29
Input/Output Capacitance: DQs, DQS, DM	C_{IO}	4.0	5.0	pF	13
Input Capacitance: Command and Address	$C_{I}1$	2.0	3.0	pF	13
Input Capacitance: CK, CK#	$C_{I}2$	2.0	3.0	pF	13
Input Capacitance: CKE	$C_{I}3$	2.0	3.0	pF	13

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 1-5, 14-17, 33; refer to DDR200/266 data sheet for all notes)
(0°C ≤ T_A ≤ 50°C; $V_{DD}Q$ = +2.65V ±0.10V, V_{DD} = +2.65V ±0.10V)

AC CHARACTERISTICS			-5 (TSOP)			
PARAMETER		**SYMBOL**	**MIN**	**MAX**	**UNITS**	**NOTES**
Access window of DQs from CK/CK#		^tAC	-0.6	+0.6	ns	
CK high-level width		^tCH	0.45	0.55	^tCK	30
CK low-level width		^tCL	0.45	0.55		
Clock cycle time	CL = 3	^tCK	5	5	ns	45,52
DQ and DM input hold time relative to DQS		^tDH	0.45	na	ns	26,31
DQ and DM input setup time relative to DQS		^tDS	0.45		ns	26,31
DQ and DM input pulse width (for each input)		^tDIPW	1.4		ns	31
Access window of DQS from CK/CK#		^tDQSCK	-0.50	+0.50	ns	
DQS input high pulse width		^tDQSH	0.4		^tCK	
DQS input low pulse width		^tDQSL	0.4		^tCK	
DQS-DQ skew, DQS to last DQ valid, per group, per access		^tDQSQ		0.35	ns	25, 26
Write command to first DQS latching transition		^tDQSS	0.75	1.25	^tCK	
DQS falling edge to CK rising - setup time		^tDSS	0.22		^tCK	
DQS falling edge from CK rising - hold time		^tDSH	0.22		^tCK	
Half clock period		^tHP	^tCH,^tCL		ns	34
Data-out high-impedance window from CK/CK#		^tHZ		+0.60	ns	18,42
Data-out low-impedance window from CK/CK#		^tLZ	-0.60		ns	18,43
Address and control input hold time (fast slew rate)		^tIH_F	0.75		ns	14
Address and control input setup time (fast slew rate)		^tIS_F	0.75		ns	14
Address and control input hold time (slow slew rate)		^tIH_S	na		ns	14
Address and control input setup time (slow slew rate)		^tIS_S	na		ns	14
Address and control input pulse width		^tIPW	1.8		ns	
LOAD MODE REGISTER command cycle time		^tMRD	10		ns	
DQ-DQS hold, DQS to first DQ to go non-valid, per access		^tQH	^tHP - ^tQHS		ns	25, 26
Data Hold Skew Factor		^tQHS		0.50	ns	
ACTIVE to AUTOPRECHARGE command		^tRAP	20		ns	46
ACTIVE to PRECHARGE command		^tRAS	40	70,000	ns	35
ACTIVE to ACTIVE/AUTO REFRESH command period		^tRC	60		ns	
AUTO REFRESH command period		^tRFC	70		ns	50
ACTIVE to READ or WRITE delay		^tRCD	20		ns	
PRECHARGE command period		^tRP	20		ns	
DQS read preamble		^tRPRE	0.9	1.1	^tCK	42
DQS read postamble		^tRPST	0.4	0.6	^tCK	
ACTIVE bank *a* to ACTIVE bank *b* command		^tRRD	10		ns	
DQS write preamble		^tWPRE	0.25		^tCK	
DQS write preamble setup time		^tWPRES	0		ns	20, 21
DQS write postamble		^tWPST	0.4	0.6	^tCK	19
Write recovery time		^tWR	15		ns	
Internal WRITE to READ command delay		^tWTR	2		^tCK	
Data valid output window		na	^tQH - ^tDQSQ		ns	25
REFRESH to REFRESH command interval		^tREFC		140.6	µs	23
Average periodic refresh interval		^tREFI		15.6	µs	23
Terminating voltage delay to V_{DD}		^tVTD	0		ns	
Exit SELF REFRESH to non-READ command		^tXSNR	75		ns	
Exit SELF REFRESH to READ command		^tXSRD	200		^tCK	

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