MK1492-03

MICROCLOCK Intel™ Mobile/SDRAM Clock Source

Description

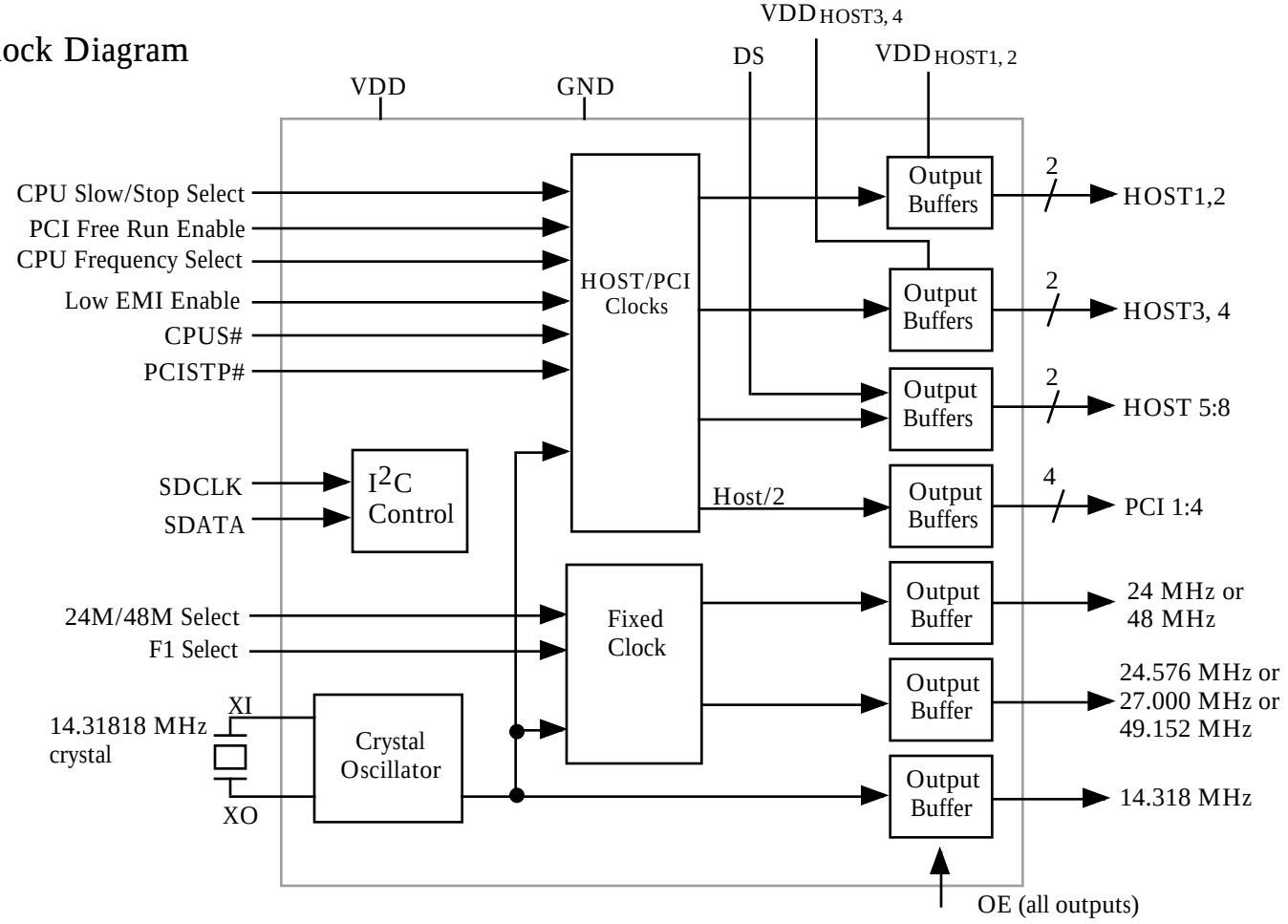
The MK1492-03 is a low cost, low jitter, high performance clock synthesizer for Intel's 430TX and 440BX chipsets for Pentium™ and Pentium II Processor based computer applications. Using patented analog Phase-Locked Loop (PLL) techniques, the device accepts a 14.318 MHz crystal input to produce multiple output clocks up to 75 MHz. It provides selectable Host and Host/2 PCI local bus clocks and a selectable 24/48 MHz clock for Super I/O or Universal Serial Bus (USB). The device has up to eight Host output clocks, and includes a serial port for controlling the output clocks.

The chip has three different power down modes to reduce power consumption.

Features

- I2C Serial Port for ACPI support
- Packaged in 28 pin, 150 mil wide SSOP
- Provides all critical timing for Intel mobile chipsets
- Separate VDD and auto adjust for Host 1,2 supports 3.3 V or 2.5V processors
- 48MHz USB or 24MHz SIO support
- Single pin CPU(Host) slowdown to 33.3MHz option
- Multiple power down modes
- Low EMI Enable pin reduces EMI radiation on HOST and PCI clocks (patented)
- Selectable PCIF on up to 3 outputs
- Support for AC97 audio clocks

Block Diagram



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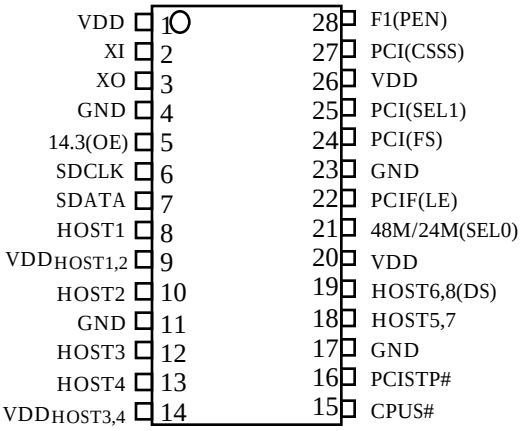
Pin Assignment



48M/24M Frequency Select Table (MHz)

SEL0	48M/24M
0	24.0
1	48.0

PCIF Enable Control

PEN	Pin 25	Pin 24
0	PCI	PCI
M	PCI	PCIF
1	PCIF	PCIF

F1 Frequency Select

SEL1	F1
0	24.576
M	27.0
1	49.152

Host/PCI Frequency Select Table

CPUS#	CSSS	FS	OE=M HOST	OE=1 HOST
1	X	0	60.0	50.0
1	X	1	66.66	75.0
M	0	X	33.33	33.33

Output Enable Control Table

OE	ALL CLOCK OUTPUTS
0	TRISTATED
M, 1	ENABLED

EMI Control

LE	Low EMI
0	ON
1	OFF

HOST7,8 Enable

DS	HOST7,8
0	ENABLED
1	TRISTATED

Power Down Control Table

PCISTP#	CPUS#	CSSS	MODE	HOST3:8	HOST1,2	PCI	PCIF	48/24	14.3	DESCRIPTION
1	1	X	ON	ON	ON	ON	ON	ON	ON	All Clocks On.
0	1 or M	X	PCI STOP	U	U	LOW	U	U	U	PCI Outputs synchronously enter and leave low state
X	M	0	CPU SLOW	33MHz	33 MHz	U	16.6M	ON	ON	Host smooth transition to/from 33 MHz.
X	M	1	CPU STOP	ON	LOW	U	ON	ON	ON	Host Outputs synchronously enter and leave low state
X	0	X	Power Down	LOW	LOW	LOW	LOW	LOW	LOW	All outputs low. PLLs and Oscillator off.
M	M	X	PLL STOP	LOW	LOW	LOW	LOW	LOW	ON	Oscillator on. PLLs off.

Key: 1 = connected to VDD, 0 = connected to ground, M = VDD/2, X = any valid logic level, U = unchanged (not affected) from previous state. Combination Input/Outputs should be connected to VDD or Ground through a 10 kΩ resistor as shown on page 7.

Pin Descriptions

Pin #	Name	Type	Description
1, 20, 26	VDD	P	Connect to +3.3V. Must be same voltage on all pins.
2	XI	I	Crystal connection. Connect to a 14.31818 MHz crystal or input clock.
3	XO	O	Crystal connection. Connect to a 14.31818 MHz crystal, or leave unconnected for clock.
4, 11, 17, 23	GND	P	Connect to Ground.
5	14.3(OE)	O/TI	14.318 MHz output. Amplitude matches VDD. Tri-State input control for all clocks.
6	SDCLK	I	I^2C Serial Port Clock
7	SDATA	I	I^2C Serial Port Data
8, 10	HOST 1,2	O	Host Output Clocks 1, 2. Amplitude matches $VDD_{HOST1,2}$. Auto adjusts for low skew at 2.5 V.
9, 14	$VDD_{HOST1,2 \text{ or } 3,4}$	P	Connect to CPU VDD supply (3.3V or 2.5V).
12, 13, 18	HOST 3,4,5,7	O	Host Output Clocks. HOST7,8 enabled by DS input per table above.
15	CPUS#	TI	CPU Stop power down control; defined in table above. Signal connection on page 7.
16	PCISTP#	TI	PCI Stop power down control; defined in table above. Signal connection on page 7.
19	HOST6,8(DS)	I/O	Host Output Clock and DS input. HOST7,8 enabled by DS input per table above.
21	48M/24M(SEL0)	I/O	Fixed frequency clock and fixed frequency select input per table above.
22	PCIF(LE)	I/O	PCI Output clock that continues to run in PCI STOP mode. Low EMI enable input.
24	PCI(FS)	I/O	PCI Output clock, and CPU Frequency Select input. See PCIF and PCI tables above.
25	PCI(SEL1)	O/TI	PCI Output clock, andSEL1 Select input. See PCIF and F1 tables above.
27	PCI(CSSS)	I/O	PCI output clock and CPU slow or stop mode select input per table above.
28	F1(PEN)	O/TI	F1 clock output and PCIF Enable input.

Key: I = Input, TI = tri-level input, O = Output, P = Power supply connection, I/O = Input on power up, becomes an Output after 10ms

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Electrical Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (note 2)					
Supply voltage, VDD	Referenced to GND			7	V
Inputs and Clock Outputs	Referenced to GND	-0.5		VDD+0.5	V
Ambient Operating Temperature		0		70	°C
Soldering Temperature	Max of 10 seconds			260	°C
Storage temperature		-65		150	°C
DC CHARACTERISTICS (VDD = 3.3V unless noted)					
Operating Voltage, VDD		3.0	3.3	3.6	V
Operating Voltage, $VDD_{HOST1,2 \text{ or } 3,4}$			2.5/3.3	VDD	V
Input High Voltage, VIH		2			V
Input Low Voltage, VIL				0.8	V
Output High Voltage, VOH	IOH=-8mA	2.4			V
Output Low Voltage, VOL	IOL=8mA			0.4	V
Output High Voltage, VOH	IOH=-8mA	VDD-0.4			V
Operating Supply Current, IDD	No Load, 66.6MHz		62		mA
Power Down mode Supply Current			3		µA
Short Circuit Current	Each output		±50		mA
Input Capacitance			7		pF
AC CHARACTERISTICS (VDD = 3.3V unless noted)					
Input Frequencies			14.318		MHz
Output Clock Rise Time	0.8 to 2.0V			1.5	ns
Output Clock Fall Time	2.0 to 0.8V			1.5	ns
Output Clock Duty Cycle, all MHz clocks	At 1.5V	45	49 to 51	55	%
HOST3:8 Output to Output Skew	Rising edges at 1.5V			250	ps
Skew of HOST 1,2 with respect to HOST 3:8				250	ps
PCI Output to Output Skew	Rising edges at 1.5V			500	ps
Lead of HOST outputs with respect to PCI	Rising edges at 1.5V	1	1.75	4	ns
Cycle to Cycle Jitter, CPU Clocks				250	ps
Absolute Clock Period Jitter, Other MHz Clocks		-500		500	ps
EMI reduction, peaks of 5th - 19th odd harmonics	66.6 MHz HOST clock		6	11	dB
Power up time, CPUS# going high to all clocks stable			8	20	ms
Power on time, applied VDD to all clocks stable			12	25	ms

Note 2. Stresses beyond those listed under Absolute Maximum Ratings could cause permanent damage to the device. Prolonged exposure to levels above the operating limits but below the Absolute Maximums may affect device reliability.

External Components

The MK1492 requires some inexpensive external components for proper operation. Decoupling capacitors of 0.1µF should be connected on each VDD pin to ground, as close to the MK1492 as possible. A series termination resistor of 33Ω may be used for each clock output. See the discussion on page 7 for other external resistors required for proper I/O operation. The 14.3 MHz oscillator has internal caps that provide the proper load for a parallel resonant crystal with C_L=12pF. For tuning with other values of C_L, the formula 2*(C_L-12) gives the value of each capacitor that should be connected between X1 and ground and X2 and ground.

Power-On Default Conditions

Input Pin#	Function	Default	Condition
5	OE	M	All outputs enabled.
15	CPUS#	1	HOST clocks running.
16	PCISTP#	1	PCI clocks running.
19	DS	1	HOST7, HOST8 disabled.
21	SEL0	1	48/24 (pin 21) set to 48 MHz
22	LE	1	Low EMI function OFF
24	FS	1	HOST frequency = 66.66 MHz.
25	SEL1	M	F1 (pin 28) set to 27 MHz
27	CSSS	1	Allows CPU STOP mode. Refer to Power Down Control Table on page 2.
28	PEN	M	PCI (pin 25) set to PCI clock (33.33 MHz). PCI (pin 24) set to PCIF clock (33.33 MHz).

General I^2C Serial Interface Operation

A. The I^2C address for the MK1492-03 is D2(hex). For the clock generator to be addressed by an I^2C controller, this address must be sent as a start sequence, with an acknowledge bit between each byte as shown below.

MK1492-03 Address (7 bits) + R/W# bit D2(hex)	ACK	8 bits dummy Command code	ACK	8 bits dummy Byte count	ACK

Then Bytes 0, 1, 2, 3, 4, 5 in sequence unless a STOP condition is encountered.

B. The MK1492-03 is an I^2C slave component only. It does not have any read-back capability.

C. The data transfer rate supported by the MK1492-03 is 100K bits/sec (standard mode).

D. The input is operating at 3.3 V logic levels (refer to Electrical Specifications Table).

E. The data byte format is 8-bit bytes.

F. To simplify the I^2C interface, the protocol is set to use only block writes from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop condition is encountered.

G. In the power down mode (CPUS# Low), the SDATA and SCLK pins are tristated and the internal data latches maintain all prior programming information.

H. At power-on, all registers are set to a default condition. See Byte 0 detail for its default condition; Bytes 1 through 5 default to a 1 (Enabled output state).

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Serial Configuration Command Bitmaps

Byte 0: Functional and Frequency Select Clock Register (1 = enable, 0 = disable)
Note: PD = Power-On Default

Bit	Pin #	Description	PD
7	--	(Reserved) MSB	0
6	--	(Reserved)	0
5	--	(Reserved)	0
4	--	(Reserved) LSB	0
3	--	Not used	1
2	21	48/24 MHz (Frequency Select) 1 = 48 MHz, 0 = 24 MHz	1
1	--	Bit 1 Bit 0	0
0		1 1 - Tri-State all outputs	0
		1 0 - Spread Spectrum for HOST and PCI clocks	
		0 1 - Normal Operation (Test Mode not supported)	
		0 0 - Normal Operation	

Byte 1: CPU, 24/48 MHz Active/Inactive Register (1 = enable, 0 = disable)

Bit	Pin #	Name	Intel Description
7	28	F1	48/24 MHz (Active/Inactive)
6	21	48M/24M	48/24 MHz (Active/Inactive)
5	--	--	(Reserved)
4	N/A	--	CPUCLK4 (Active/Inactive)
3	10	HOST2	CPUCLK3 (Active/Inactive)
2	10	HOST2	CPUCLK2 (Active/Inactive)
1	8	HOST1	CPUCLK1 (Active/Inactive)
0	8	HOST1	CPUCLK0 (Active/Inactive)

Notes: Bits 0 and 1 must always be at the same state. Bits 2 and 3 must always be at the same state.

Byte 2: PCI Active/Inactive Register (1 = enable, 0 = disable)

Bit	Pin #	Name	Intel Description
7	--	--	(Reserved)
6	22	PCIF	PCICLK_F (Active/Inactive)
5	N/A	--	PCICLK5 (Active/Inactive)
4	N/A	--	PCICLK4 (Active/Inactive)
3	N/A	--	PCICLK3 (Active/Inactive)
2	27	PCI	PCICLK2 (Active/Inactive)
1	25	PCI	PCICLK1 (Active/Inactive)
0	24	PCI	PCICLK0 (Active/Inactive)

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Serial Configuration Command Bitmaps (cont.)

Byte 3: SDRAM Active/Inactive Register (1 = enable, 0 = disable)

Bit	Pin #	Name	Intel Description
7	N/A	--	SDRAM7
6	N/A	--	SDRAM6
5	N/A	--	SDRAM5
4	N/A	--	SDRAM4
3	19	HOST6,8	SDRAM3 (Active/Inactive)
2	18	HOST5,7	SDRAM2 (Active/Inactive)
1	13	HOST4	SDRAM1 (Active/Inactive)
0	12	HOST3	SDRAM0 (Active/Inactive)

Byte 4: SDRAM Active/Inactive Register (1 = enable, 0 = disable)

Bit	Pin #	Name	Intel Description
7	N/A	--	SDRAM15
6	N/A	--	SDRAM14
5	N/A	--	SDRAM13
4	N/A	--	SDRAM12
3	N/A	--	SDRAM11
2	N/A	--	SDRAM10
1	N/A	--	SDRAM9
0	N/A	--	SDRAM8

Byte 5: Peripheral Active/Inactive Register (1 = enable, 0 = disable)

Bit	Pin #	Name	Intel Description
7	--	--	(Reserved)
6	--	--	(Reserved)
5	--	--	(Reserved)
4	N/A	--	IOAPIC0
3	--	--	(Reserved)
2	--	--	(Reserved)
1	N/A	--	REF1
0	5	14.3	REF0 (Active/Inactive)

Notes: Inactive means outputs are held LOW and are disabled from switching.
Byte 6 is not available on the MK1492-02.

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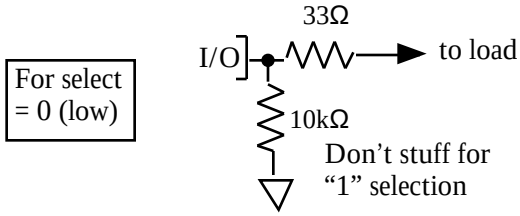
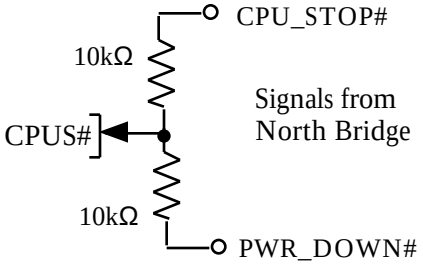
I/O Structure

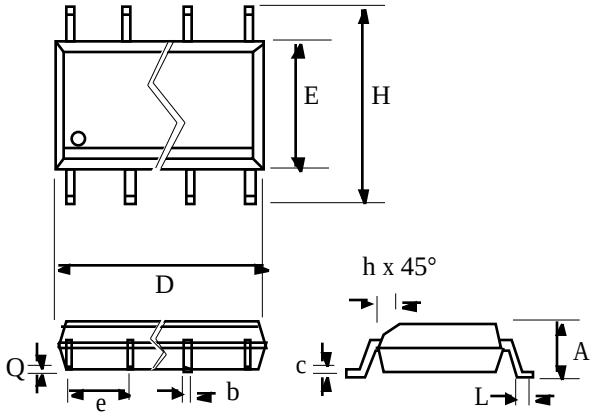
The MK1492 provides more functionality in a 28 pin package by using a unique I/O technique. The device checks the status of all I/O pins during power-up. This status (pulled high or low) then determines the frequency selections and power down modes (see the tables on page 2). Within 10ms after power up, the inputs change to outputs and the clocks start up. In the diagrams to the right, the 33Ω resistors are the normal output termination resistors. The 10kΩ resistor pulls low to generate a logic zero. Internal pull-up resistors (approx. 100kΩ) are present on DS, SEL0, FS, LE, CPUS#, PCISTP#, and CSSS. Internal resistors on PEN, SEL1, and OE pull to a mid-level (M).

The CPUS# input should be connected as shown to implement the 0, M, and 1 selections per the Power Down Control Table on page 2. Contact MicroClock for suggested connections of PCISTP# if the PLL STOP mode will be used.





Package Outline and Package Dimensions



28 pin SSOP

	Inches		Millimeters	
Symbol	Min	Max	Min	Max
A	0.061	0.068	1.55	1.73
b	0.008	0.012	0.203	0.305
c	0.007	0.010	0.190	0.254
D	0.385	0.400	9.780	10.160
E	0.150	0.160	3.810	4.064
H	0.230	0.245	5.840	6.223
e	.025 BSC		0.635 BSC	
h		0.016		0.410
L	0.016	0.035	0.406	0.889
Q	0.004	0.01	0.127	0.254

Ordering Information

Part/Order Number	Marking	Low EMI Feature	Package	Temperature
MK1492-03R	MK1492-03R	Yes	28 pin SSOP	0-70°C
MK1492-03RTR	MK1492-03R	Yes	Add Tape & Reel	-