DS04-25101-2E

FUJITSU

DATA SHEET

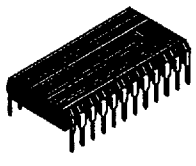
ASSP FLOPPY DISK VFO

MB4108A

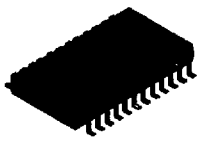
VARIABLE FREQUENCY OSCILLATOR FOR FLOPPY DISK DRIVES

The Fujitsu MB4108A is variable frequency oscillator (VFO) IC for use in floppy-disk interfaces. It provides a complete data separation function, with a minimum of external parts and no adjustments, and can be used with a variety of disk controllers. It locks onto the read signal from the disk drive, which normally has jitter due to rotation speed variations and peak shifting and produces a stable read signal for the controller. It also produce a window signal which can be used to differentiate the clock and data pulse in the read signal. The MB4108A includes functions for sync field detection, automatic loop filter gain switching and address and index mark detection.

- The analog VFO (PLL) circuitry allows a wide read margin for the data separator.
- Can be connected to both 8-inch and 5-inch floppy disk drives using the same external components.
- Handles both double-density (MFM) and single-density (FM) disks.
- Can be used with various floppy disk controllers such as the MB8876A, MB8877A, FD1791 and μPD765.
- The discrimination function for gap and sync fields prevents incorrect locking on the gap field.
- The quick sync function (high gain) in the sync field is automatically switched to the stable tracking function (low gain).
- Because the sync pattern detector (data: 00H, clock: FFH) and the IBM format mark detector control PLL gain, the index, ID and data fields can be locked onto without special control signals.
- A master clock is generated for the floppy disk controller, to prevent spikes when switching between 8 and 5 inch floppy disks.
- External circuitry requires very few components and no adjustment.
  Internal clock: 7 resistors, 5capacitors, 1crystal or ceramic resonator
  External clock: 5 resistors, 3 capacitors
- Plastic DIP Package (Suffix: -P)
  Plastic SOP (Suffix: -PF)



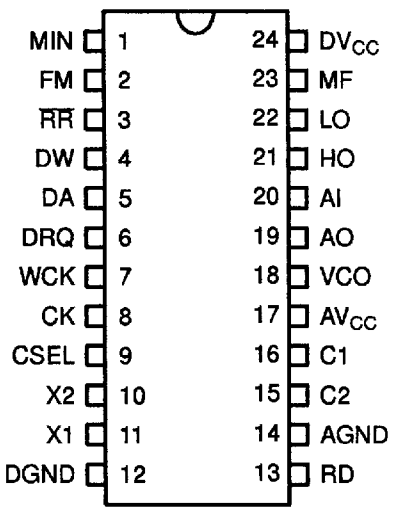
DIP-24P-M02



FPT-24P-M02

PIN ASSIGNMENT

(TOP VIEW)



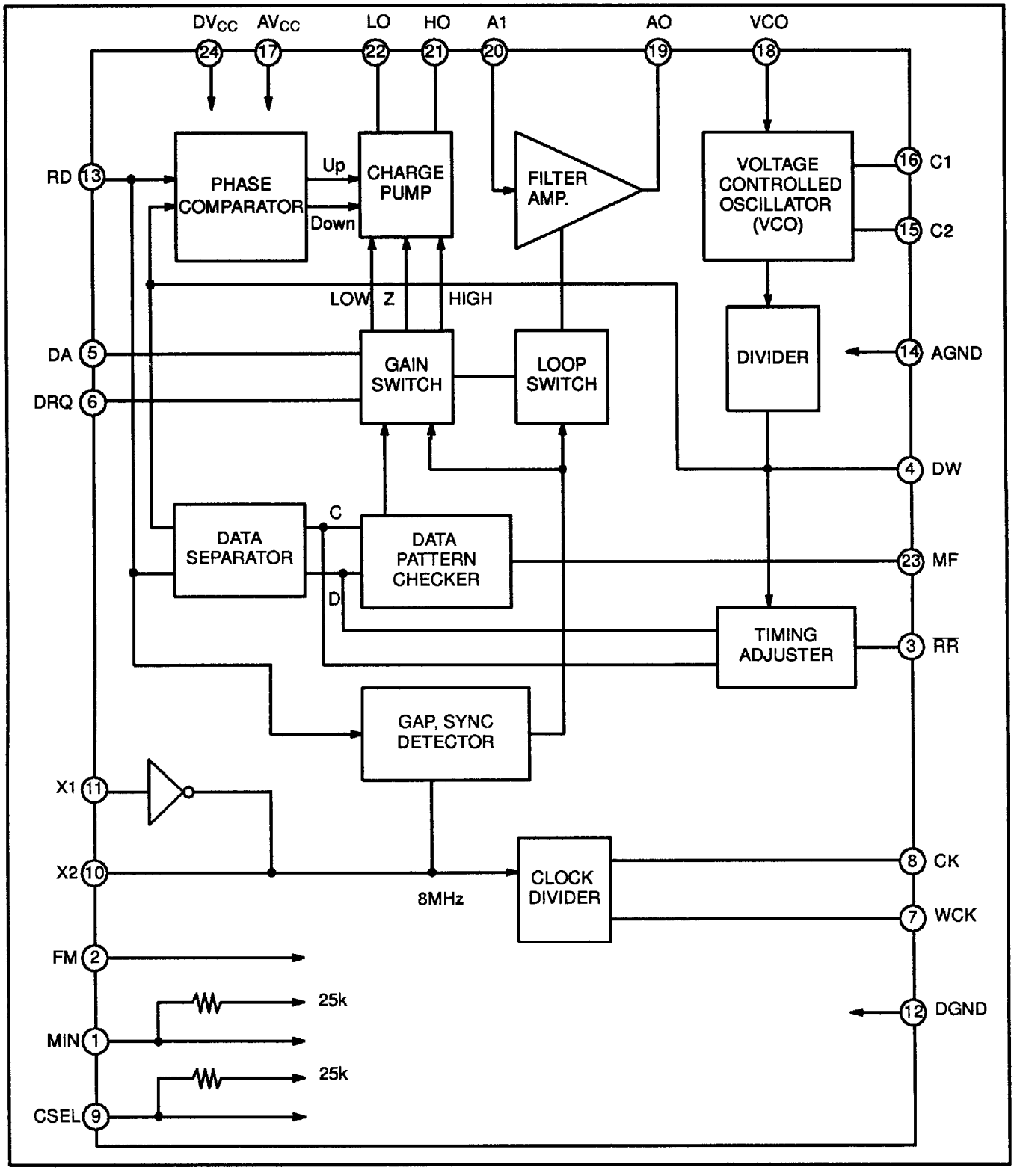
ABSOLUTE MAXIMUM RATINGS (see NOTE) (Ta=25°C)

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{CC}		7	V
Input Voltage	V_{IN}		7	V
Power Dissipation	P_D	Ta≤75°C	550	mW
Storage Temperature	T_{STG}		-55 to +125	°C
MF Input Voltage	V_{MF}		V_{CC}+0.3	V

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Symbol	Function
1	MIN	Selects type of floppy disk 5-inch floppy disk (MIN): High 8-inch floppy disk (STD): Low
2	FM	Selects the disk density Single density (FM system): High Double density (MFM system): Low
3	$\overline{RR}$	Read data signal for FDC includes clock and data pulse.
4	DW	Data window signal for separating the $\overline{RR}$ signal into data and clock pulses.
5	DA	Input for indicating a data field when there is no DRQ signal. When DA = H, the PLL keeps a low gain. Either DA or DRQ is used, but not both and the unused in is kept low.
6	DRQ	Input for Data Request. After mark is detected, PLL is kept as low gain when DRQ = H (positive edge trigger). 3 bytes data is input, PLL becomes high gain (Free run) when DRQ = L.
7	WCK	The µPD 765 system FDC write clock pulse is output from this pin 8-inch/MFM : T=1µs 8-inch/MF : T=2µs 5-inch/MFM : T=2µs 5-inch/MF : T=4µs
8	CK	The FDC clock pulse is output from this pin MB8877A system/ 8-inch : 2MHz MB8877A system/ 5-inch : 1MHz µPD 765 system/ 8-inch : 8MHz µPD 765 system/ 5-inch : 4MHz
9	CSEL	Select the FDC type (On chip pull-up resistor) MB8877A, FD1791 system : High µPD 765 system : Low
10	X2	Inverting output of the crystal oscillator The pin is open when 8MHz external clock is used.
11	X1	Inverting input of the crystal oscillator Input pin when 8MHz external clock is used.
12	DGND	Ground of digital circuit
13	RD	Source read data input from FDD
14	AGND	Ground for analog circuit such as VCO, filter amplifier
15 16	C1 C2	An external capacitor is connected to set VCO oscillation frequency
17	AV_{CC}	Power supply for analog circuit such as VCO and filter amplifier.
18	VCO	VCO control current input
19	AO	Low pass filter (LPF) output in the VFO circuit
20	AI	Low pass filter (LPF) input in the VFO circuit
21	HO	Output pin to be externally connected to the LPF amplifier. This pin is selected at frequency lock after a sync field is detected. High signal decreases VCO frequency and Low signal increases it (high gain).

PIN DESCRIPTION (Continued)

Pin No.	Symbol	Function
22	LO	Output pin to be externally connected to the LPF amplifier. This pin is selected after frequency lock for phase synchronization. High signal delays the VCO phase and low signal advances it (low gain).
23	MF	When free run mode and high gain mode, MF becomes high. After mark is detected, it becomes low and keeps low level during low gain.
24	DV_{CC}	Power supply for digital circuit

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	4.75	5.00	5.25	V
Operating Temperature	Ta	-20	+25	+75	°C

DC CHARACTERISTICS

(V_{CC}=5V,Ta=25°C)

Parameter	Symbol	Condition		Value			Unit	Pin name	Note
				Min	Typ	Max			
Power Supply Current	I_{CC}	V_{CC}=5.25V		-	70	100	mA	V_{CC}	*1
Input High Voltage	V_{IH}	V_{CC}=4.75 to 5.25V Ta=-20 to 75°C		2.0	-	-	V	MIN, FM, DA, DRQ, CX, X1, RD	
Input Low Voltage	V_{IL}			-	-	0.8	V		
Input High Current	I_{IH}	V_{CC}=5.25V, V_I=2.7V		-	-	20	µA	FM, DA, DRQ, X1, RD	
Input Current	I_I	V_{CC}=5.25V, V_I=7.0V		-	-	0.1	mA		
Input Low Current	I_{IL}	V_{CC}=5.25V, V_I=0.4V		-400	-20	-	µA		
Open-circuit Input Voltage	V_{IP}			4.85	5.0	-	V	MIN, CS	
Input Low Current	I_{ILP}	V_I=0V		-1.1	-0.6	-	mA		
Output High Voltage*1	V_{OH1}	V_{CC}=4.75V, I_{OH}=-1.2mA Ta=-20 to 75°C		2.7	3.3	-	V	$\overline{RR}$, DW	*2
Output Low Voltage*1	V_{OL1}	V_{CC}=4.75V Ta=-20 to 75°C	I_{OL}=12mA	-	0.28	0.4	V		*3
			I_{OL}=24mA	-	0.35	0.5	V		
Short-Circuit Output Current*1	I_{OS1}	V_{CC}=5.25V Ta=-20 to 75°C		-30	-	-160	mA		*2

Note: *1 AV_{CC} and DV_{CC} are connected together.
*2 The output stage is set high.
*3 The output stage is set low.

DC CHARACTERISTICS (Continued)

(V_{CC}=5V,Ta=25°C)

Parameter	Symbol	Condition		Value Min	Value Typ	Value Max	Unit	Pin name	Note
Output High Voltage*2	V_{OH2}	V_{CC}=4.75V, I_{OH}=−0.4mA Ta=−20 to 75°C		2.7	3.3	−	V	WCK, CK	*2
Output Low Voltage*2	V_{OL2}	V_{CC}=4.75V Ta=−20 to 75°C	I_{OL}=4mA	−	0.28	0.4	V	WCK, CK	*3
			I_{OL}=8mA	−	0.35	0.5	V		
Short-Circuit Output Current*2	I_{OS2}	V_{CC}=5.25V Ta=−20 to 75°C		−20	−	−110	mA	WCK, CK	*2
Output High Voltage*3	V_{OH3}	V_{CC}=4.75V, I_{OH}=−0.4mA Ta=−20 to 75°C		2.7	3.3	−	V	X2	*2
Output Low Voltage*3	V_{OL3}	V_{CC}=4.75V, I_{OL}=1mA Ta=−20 to 75°C		−	0.28	0.4	V	X2	*3
Output Leakage Current	I_{OH4}	V_{CC}=5.25V, V_O=5.25V		−	−	20	µA	MF	*2
Output Low Voltage	V_{OL4}	V_{CC}=5.25V, I_O=1mA Ta=−20 to 75°C		−	0.35	0.5	V	MF	*3
Output High Voltage	V_{HH}	I_{OH}=−1mA		3.3	3.7	−	V	HO	*2
Output Low Voltage	V_{LH}	I_{OL}=1mA		−	2.0	2.4	V	HO	*3
Output High Voltage	V_{HL}	I_{OH}=−0.2mA		3.8	4.2	−	V	LO	*2
Output Low Voltage	V_{LL}	I_{OL}=0.2mA		−	1.5	1.9	V	LO	*3
V_{CC} Free Running Frequency	f_{FR}			1.6	2.0	2.4	MHz		

Notes: *2 The output stage is set high.
*3 The output stage is set low.

AC CHARACTERISTICS

(V_{CC}=5V, f_{X1}=8MHz)

Pin Name	Parameter	Symbol	Condition		Value			Unit
					Min	Typ	Max	
CK	Rising Time	t_r	C_L=25pF		–	3	–	ns
	Falling Time	t_f			–	2	–	
	Frequency	f_{CK}	CSEL=H MB8876A	MIN=L	–	2	–	MHz
				MIN=H	–	1	–	
			CSEL=L μPD765	MIN=L	–	8	–	
				MIN=H	–	4	–	
	Duty Ratio	DR_{CK}	CSEL=H	C_L=25pF	–	50	–	%
			CSEL=L		–	50	–	
WCK	Rising Time	t_r	C_L=25pF		–	3	–	ns
	Falling Time	t_f			–	2	–	
	Cycle Time	T_{CY}	MIN=L	MFM=H	–	1	–	μs
				MFM=L	–	2	–	
			MIN=H	MFM=H	–	2	–	
				MFM=L	–	4	–	
	High level Width	T_{WH}	MIN=L	MFM=H	–	250	–	ns
				MFM=L	–	250	–	
			MIN=H	MFM=H	–	500	–	
				MFM=L	–	500	–	
DW	Rising Time	t_r	C_L=25pF		–	3	–	ns
	Falling Time	t_f			–	2	–	
	Window Pulse Width (High level width)	T_W	MIN=L	MFM=H	–	1	–	μs
				MFM=L	–	2	–	
			MIN=H	MFM=H	–	2	–	
				MFM=L	–	4	–	

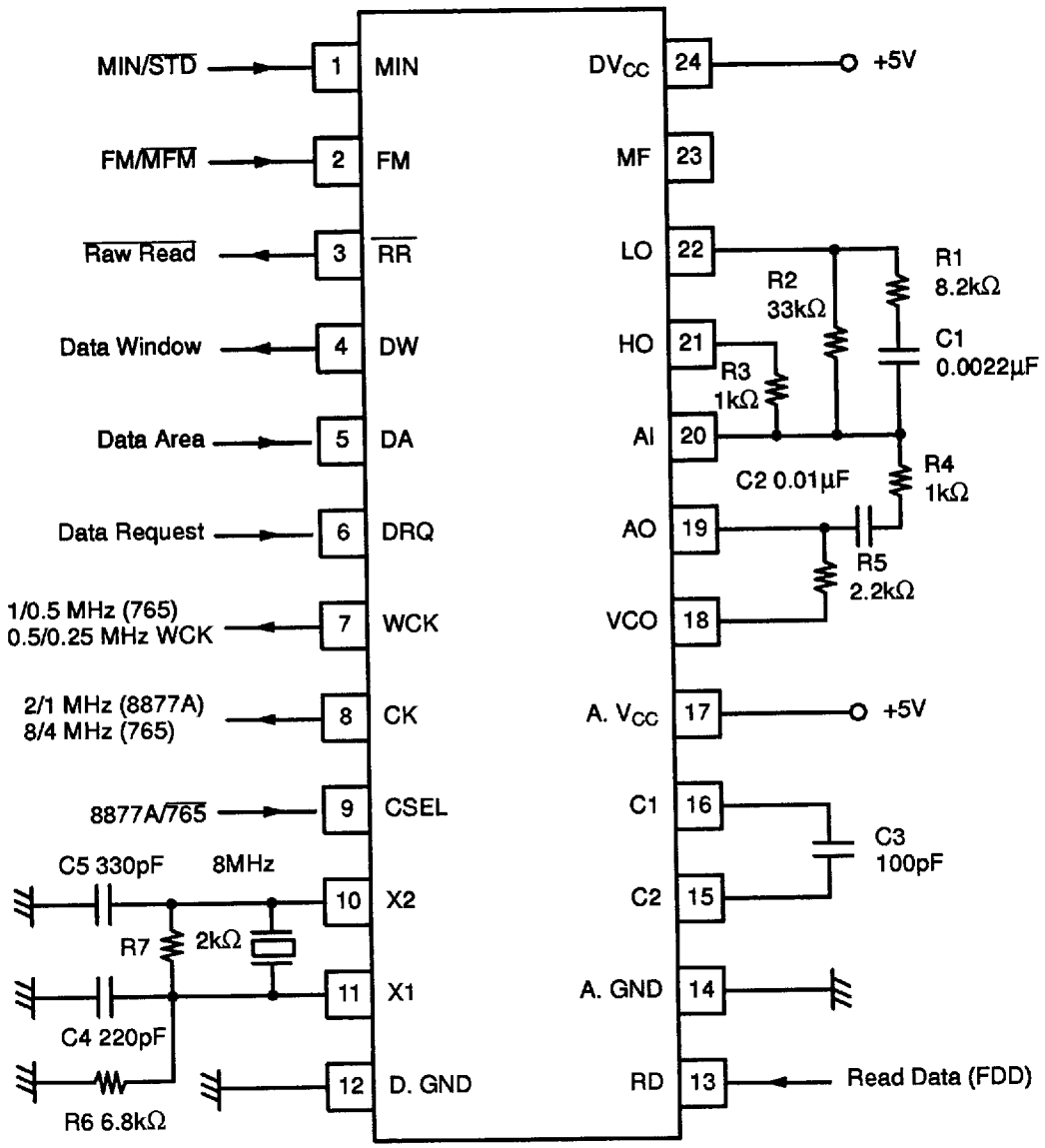
AC CHARACTERISTICS

(V_{CC}=5V, f_{X1}=8MHz)

Pin Name	Parameter	Symbol	Condition		Value			Unit
					Min	Typ	Max	
$\overline{RR}$	Rising Time	t_r	C_L=25pF		–	3	–	ns
	Falling Time	t_f			–	2	–	
	Low-level Width	T_{WL}	MIN=L	MFM=H	–	0.25	–	µs
				MFM=L	–	0.5	–	
			MIN=H	MFM=H	–	0.5	–	
				MFM=L	–	1	–	
	Time Deviation from DW Center	T_D			–	10	–	ns
RD	High-level Width	T_{WH}			50	–	–	
DRQ	High-level Width	T_{WH}			50	–	–	
X1	External Clock Duty Ratio	DXET	f_{X1}=8MHz/9.6MHz		40	50	60	%

TYPICAL CONNECTION CIRCUIT

Fig. 1 – STANDARD EXTERNAL CIRCUITS



Notes: 1. C_3 (±5%), R_5 (±1%), otherwise C (±10%), R (±5%)

2. Since the 8MHz internal and 8MHz external clocks require precision of ±1%, a ceramic resonator can be used when WCK and CK do not required a high precision.

TYPICAL APPLICATION CIRCUIT

Interface with FDD, FDC

Fig. 2 – Applying Data Request

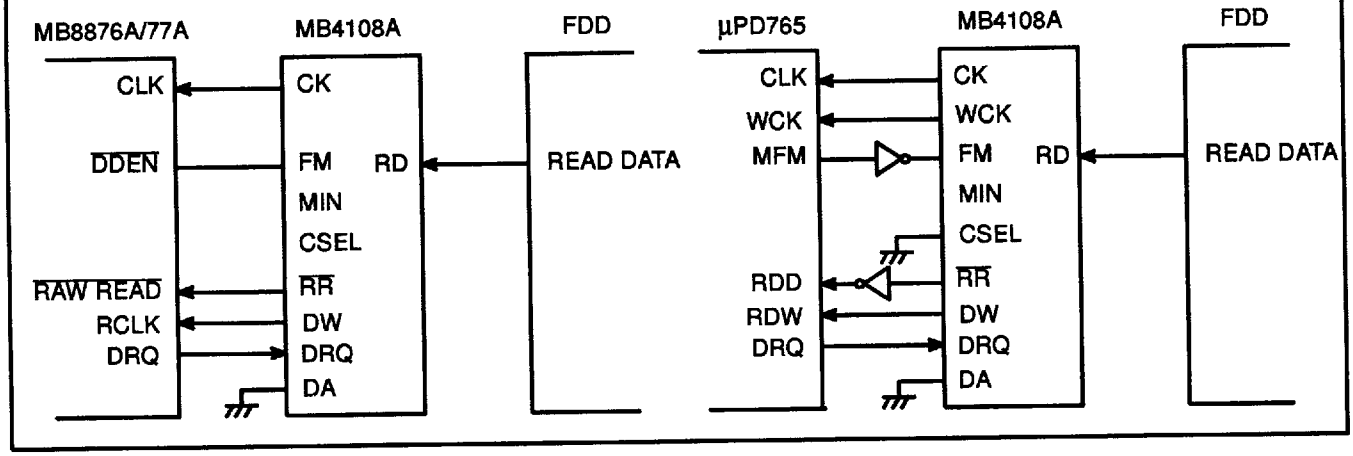
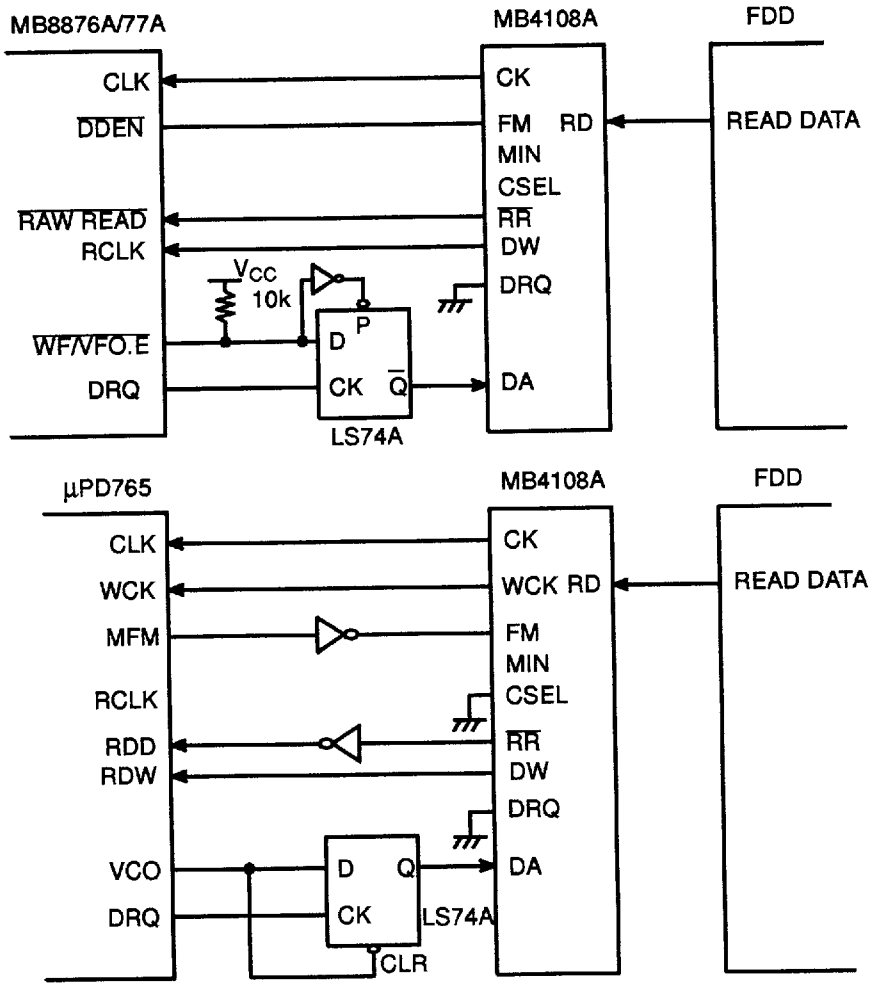
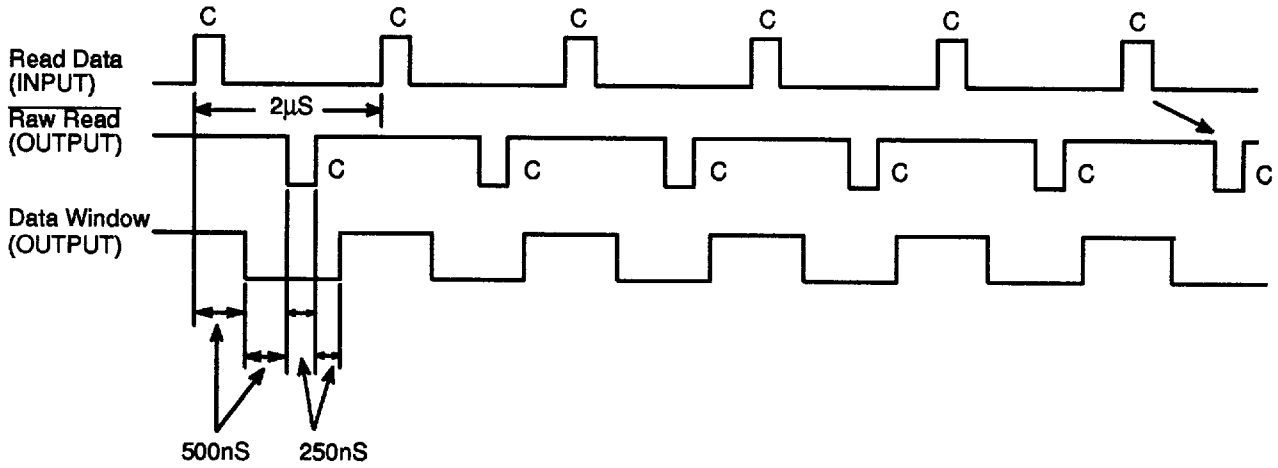


Fig. 3 – Applying VFO Enable/VCO Sync, Data Request

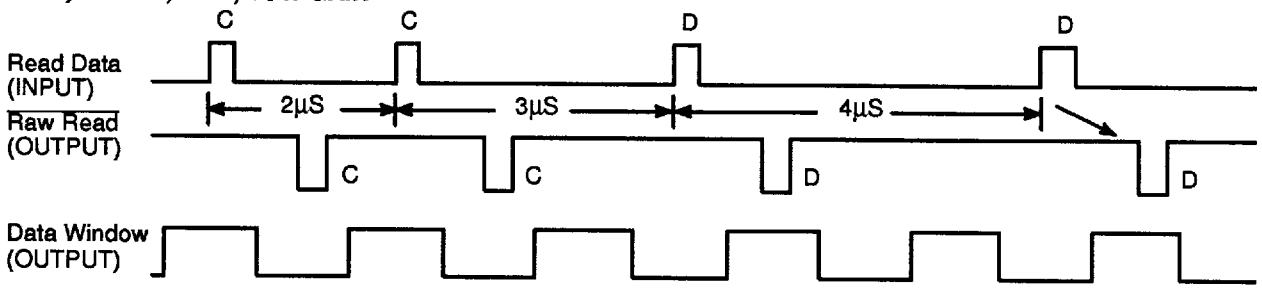


TIMING DIAGRAM

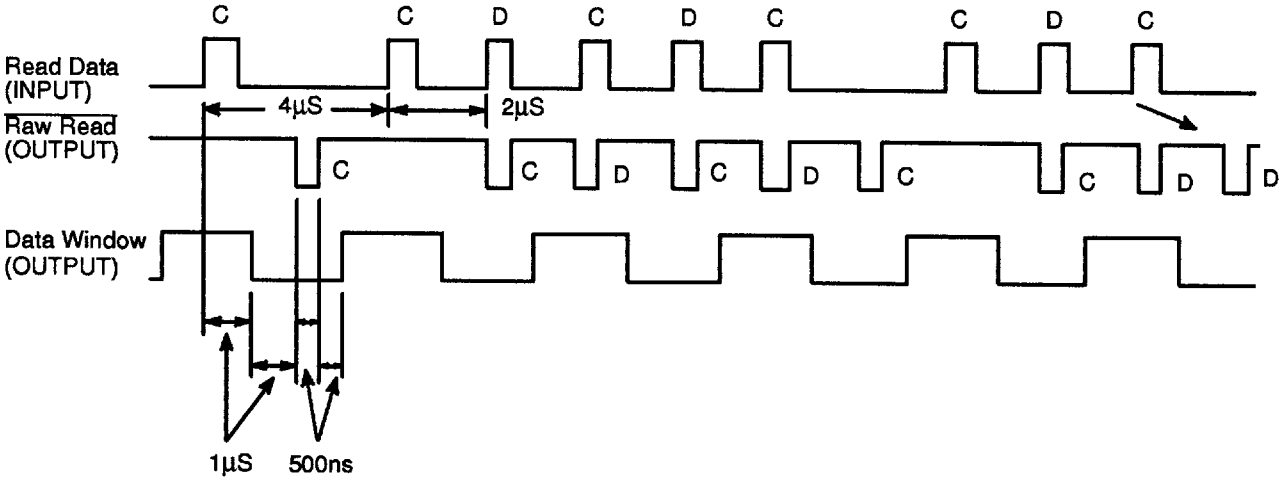
I) 8 INCH, MFM, HIGH GAIN (SYNC FIELD)



II) 8 INCH, MFM, LOW GAIN



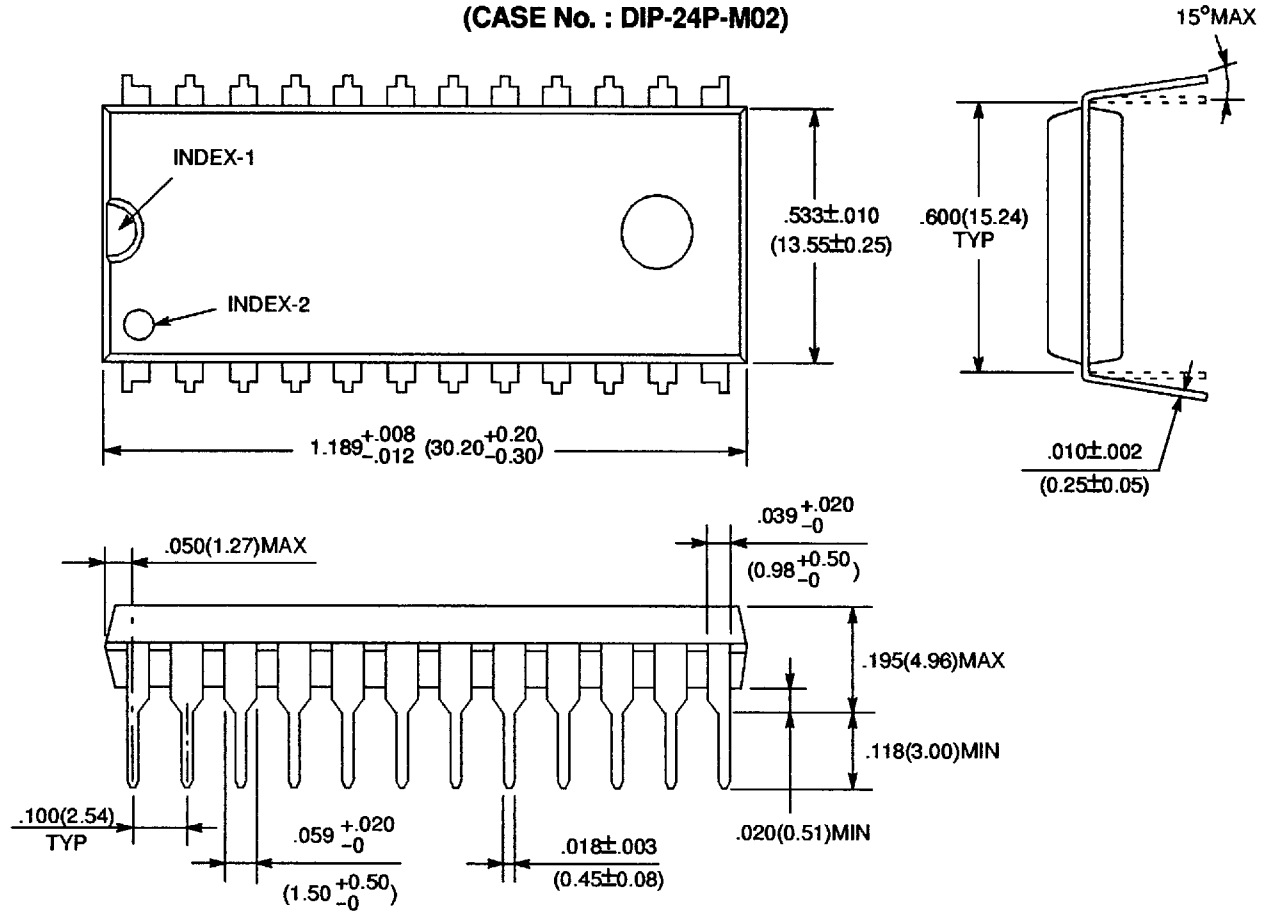
III) 8 INCH, FM, LOW GAIN



Notes : 1. The above times are doubled for 5-inch floppy disks.
2. C=clock pulse, D=data pulse.

PACKAGE DIMENSIONS

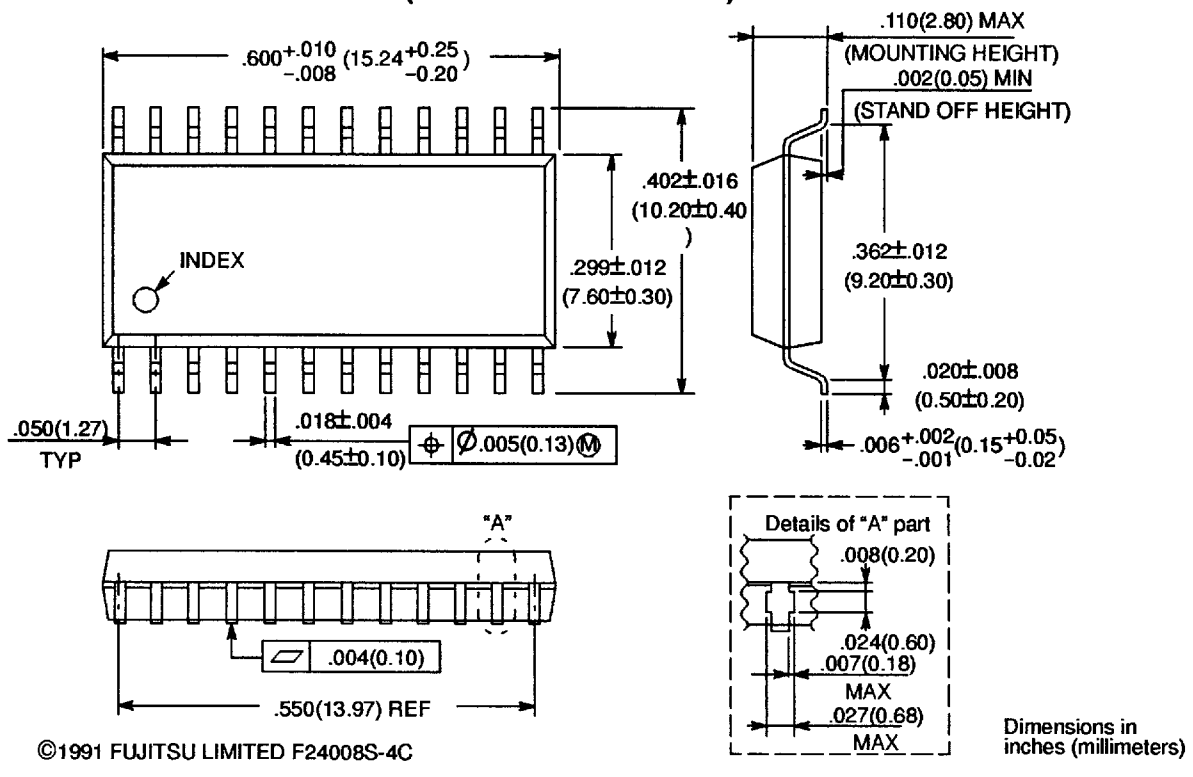
24-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-24P-M02)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

24-LEAD PLASTIC FLAT PACKAGE
(CASE No. : FPT-24P-M02)



Dimensions in inches (millimeters)