
HN624416 Series

1048576-word × 16-bit/ 2097152-word × 8-bit CMOS
Mask Programmable ROM

HITACHI

ADE-203-466 (Z)
Preliminary
Rev. 0.0
Nov. 20, 1995

Description

The HN624416 is a 16-Mbit CMOS mask-Programmable ROM organized either as 1048576 words by 16 bits or 2097152 words by 8 bits. Realizing low power consumption, this memory is allowed for battery operation. And a high speed access of 100/120 ns (max) is the most suitable to the system using a high speed micro-computer by 16 bits.

Feature

- Single 5 V supply
- High speed
Access time: 100/120 ns (max)
- Low power
Active: 660 mW (max)
Standby: 165 μ W (max)
- Byte-wide or word-wide data organization (Switched by BHE terminal)
- Three-state data output for or-tying
- Directly TTL compatible
All inputs and outputs
- Pin compatible with 8 Mbit Mask ROM (HN62448)

Ordering Information

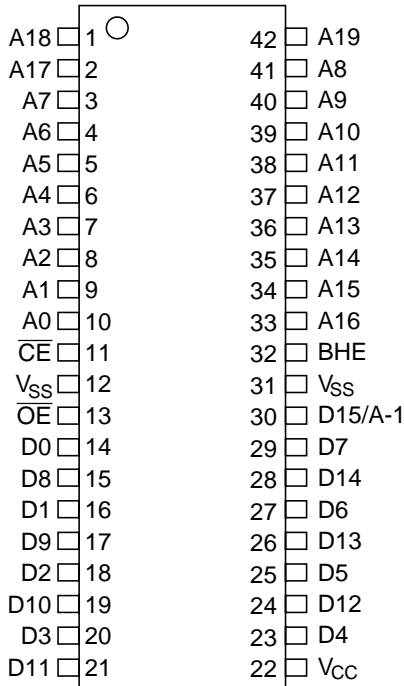
Type No.	Access time	Package
HN624416P-10	100 ns	600 mil 42-pin plastic DIP (DP-42)
HN624416P-12	120 ns	
HN624416FB-10	100 ns	600 mil 44-pin plastic SOP (FP-44D)
HN624416FB-12	120 ns	
HN624416TT-10	100 ns	400 mil 44-pin plastic TSOP II (TTP-44D)
HN624416TT-12	120 ns	

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

HN624416 Series

Pin Arrangement

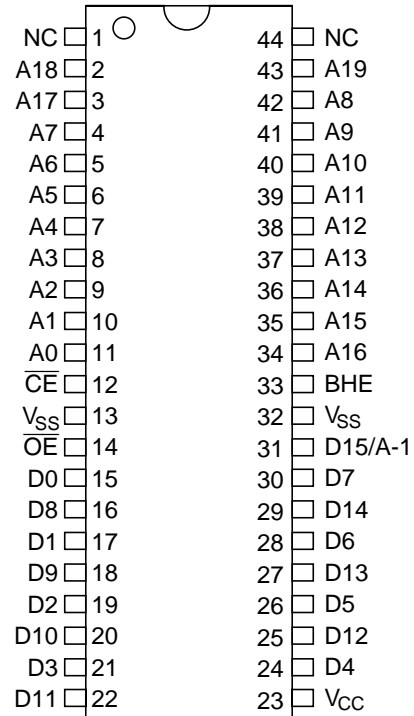
HN624416P Series



(Top View)

HN624416FB Series

HN624416TT Series

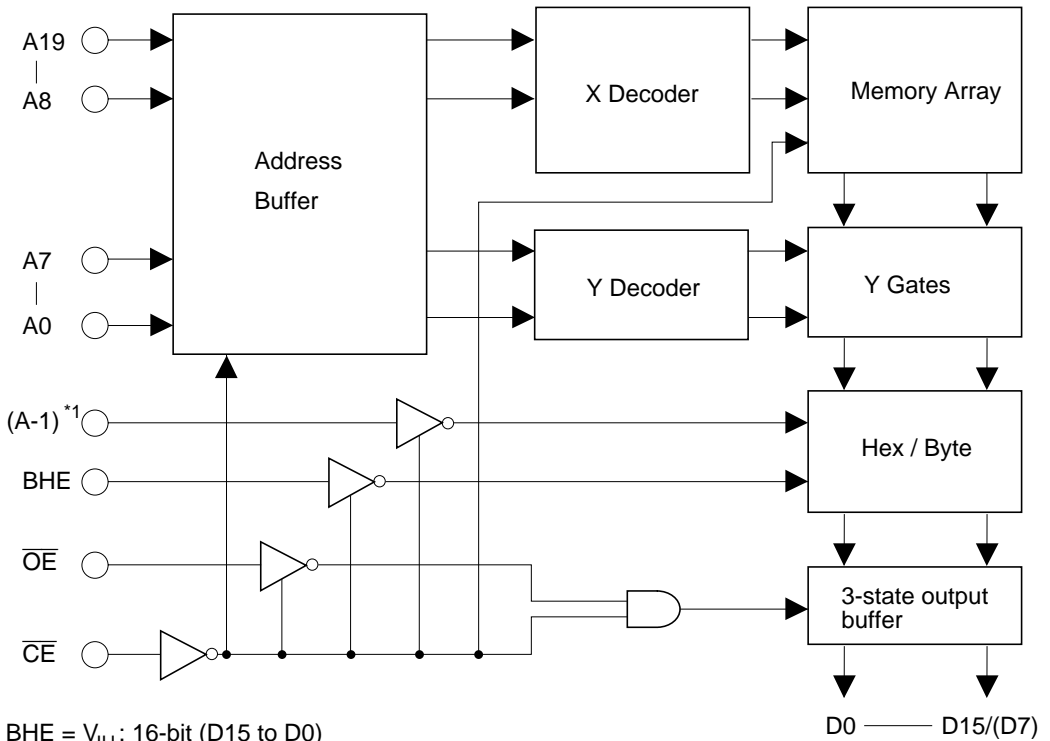


(Top View)

Pin Description

Pin name	Function
A-1, A0 to A19	Address inputs
D0 to D15	Data outputs
BHE	8/16 bit (byte/word) mode switch
\overline{CE}	Chip enable
\overline{OE}	Output enable
NC	No connection
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



BHE = V_{IH} : 16-bit (D15 to D0)
 BHE = V_{IL} : 8-bit (D7 to D0)

Note: 1. A-1 is least significant address.

When BHE is 'low', D14 to D8 goes the high impedance state, and D15 should be A-1.

Mode Selection

Mode	Pin				Data output		Address input	
	\overline{CE}	\overline{OE}	BHE	D15/A-1	D0-D7	D8-D15	LSB	MSB
Standby	H	\times^1	\times	\times	High-Z ²	High-Z	—	—
Output disable	L	H	\times	\times	High-Z	High-Z	—	—
Read (16-bit)	L	L	H	Dout	D0 to D7	D8 to D15	A0	A19
Read (8-bit)	L	L	L	L	D0 to D7	High-Z	A-1	A19
Read (8-bit)	L	L	L	H	D8 to D15	High-Z	A-1	A19

Notes: 1. \times : Don't care.

2. High-Z: High impedance

HN624416 Series

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage ^{*1}	V_{CC}	-0.3 to + 7.0	V
All input and output voltage ^{*1}	V_{in}, V_{out}	-0.3 to $V_{CC} + 0.3$	V
Operating temperature range	T_{opr}	0 to + 70	°C
Storage temperature range	T_{stg}	-55 to + 125	°C
Temperature under bias	T_{bias}	-20 to + 85	°C

Note: 1. With respect to V_{SS} .

Recommended DC Operating Conditions ($T_a = 0$ to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.2	—	$V_{CC} + 0.3$	V
	V_{IL}	-0.3	—	0.8	V

DC Characteristics ($V_{CC} = 5.0$ V \pm 10%, $V_{SS} = 0$ V, $T_a = 0$ to + 70°C)

Parameter		Symbol	Min	Max	Unit	Test conditions
Supply current	Active	I_{CC}	—	120/100	mA	$V_{CC} = 5.5$ V, $I_{DOUT} = 0$ mA, $t_{RC} = 100/120$ ns
	Standby	I_{SB1}	—	30	μ A	$V_{CC} = 5.5$ V, $\overline{CE} \geq V_{CC} - 0.2$ V
	Standby	I_{SB2}	—	3	mA	$V_{CC} = 5.5$ V, $\overline{CE} \geq 2.2$ V
Input leakage current		$ I_{IL} $	—	10	μ A	$V_{in} = 0$ to V_{CC}
Output leakage current		$ I_{OL} $	—	10	μ A	$\overline{CE} = 2.2$ V, $V_{out} = 0$ to V_{CC}
Output voltage		V_{OH}	2.4	—	V	$I_{OH} = -205$ μ A
		V_{OL}	—	0.4	V	$I_{OL} = 1.6$ mA

Capacitance ($V_{CC} = 5.0$ V \pm 10%, $V_{SS} = 0$ V, $T_a = 25$ °C, $V_{in} = 0$ V, $f = 1$ MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance ^{*1}	C_{in}	—	10	pF
Output capacitance ^{*1}	C_{out}	—	15	pF

Note: 1. This parameter is sampled and not 100% tested. D15/A-1 pin is output.

AC Characteristics ($V_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = 0 \text{ V}$, $T_a = 0 \text{ to } +70^\circ\text{C}$)

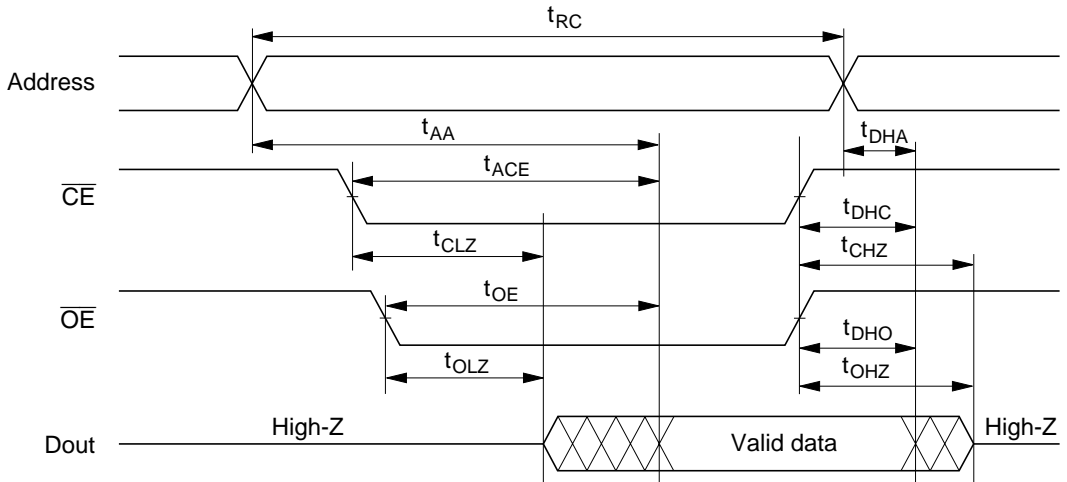
- Output load: 1TTL + $C_L = 100 \text{ pF}$ (including jig)
- Input pulse level: 0.45 to 2.4 V
- Input and output timing reference level: 1.5 V
- Input rise and fall time: 5 ns

Parameter	Symbol	HN624416-10		HN624416-12		Unit	Note
		Min	Max	Min	Max		
Read cycle time	t_{RC}	100	—	120	—	ns	
Address access time	t_{AA}	—	100	—	120	ns	
\overline{CE} access time	t_{ACE}	—	100	—	120	ns	
\overline{OE} access time	t_{OE}	—	40	—	50	ns	
BHE access time	t_{BHE}	—	100	—	120	ns	
Output hold time from address change	t_{DHA}	5	—	5	—	ns	
Output hold time from \overline{CE}	t_{DHC}	0	—	0	—	ns	
Output hold time from \overline{OE}	t_{DHO}	0	—	0	—	ns	
Output hold time from BHE	t_{DHB}	0	—	0	—	ns	
\overline{CE} to output in high-Z	t_{CHZ}	—	30	—	30	ns	1
\overline{OE} to output in high-Z	t_{OHZ}	—	30	—	30	ns	1
BHE to output in high-Z	t_{BHZ}	—	30	—	30	ns	1
\overline{CE} to output in low-Z	t_{CLZ}	5	—	5	—	ns	
\overline{OE} to output in low-Z	t_{OLZ}	5	—	5	—	ns	
BHE to output in low-Z	t_{BLZ}	5	—	5	—	ns	

Note: 1. t_{CHZ} , t_{OHZ} and t_{BHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

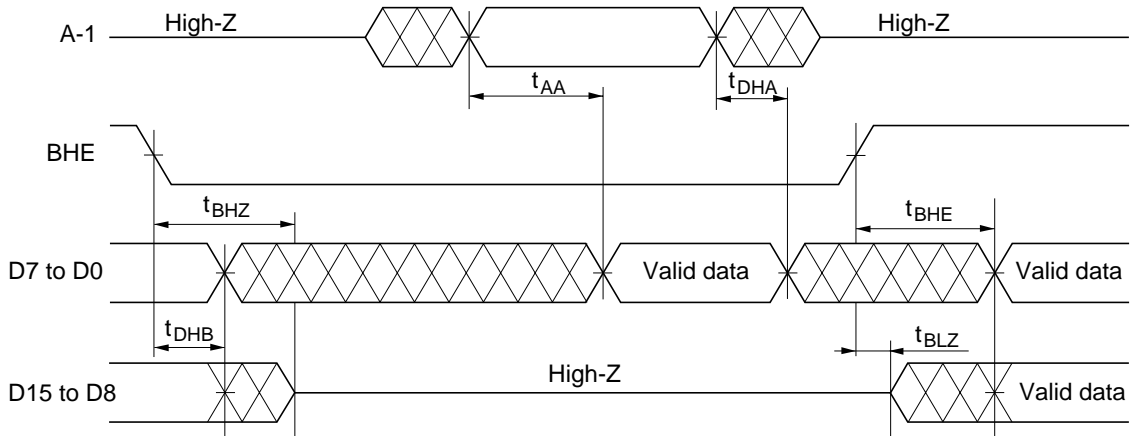
Timing Waveforms

Word Mode (BHE = 'V_{IH}') or Byte Mode (BHE = 'V_{IL}')



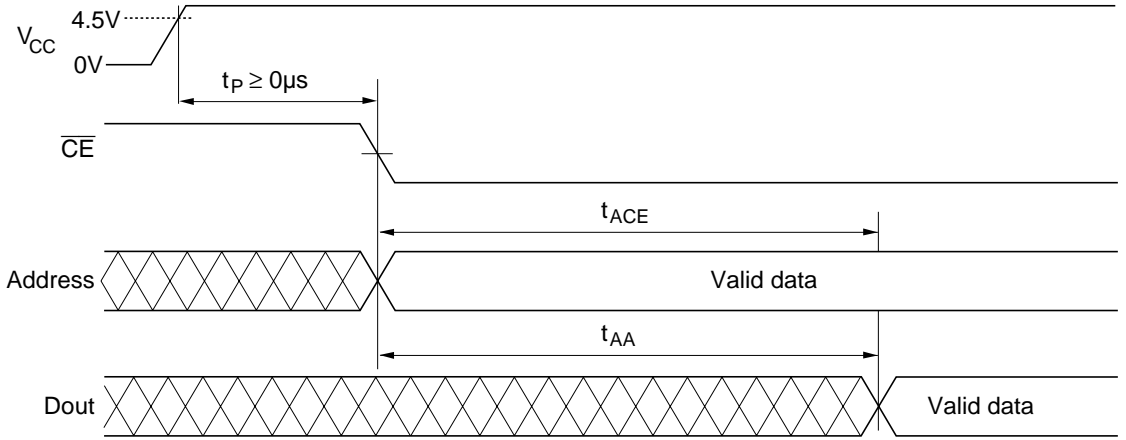
- Notes: 1. t_{DHA} , t_{DHC} , t_{DHO} : Determined by faster.
 2. t_{AA} , t_{ACE} , t_{OE} : Determined by slower.
 3. t_{CLZ} , t_{OLZ} : Determined by slower.

Word Mode, Byte Mode Switch



- Notes: 1. \overline{CE} and \overline{OE} are enable, A19 to A0 are valid.
 2. D15/A-1 pin is in the output state when BHE is high, \overline{CE} and \overline{OE} are enable.
 Therefore, the input signals of opposite phase to the output must not be applied to them.

Power Up Sequence



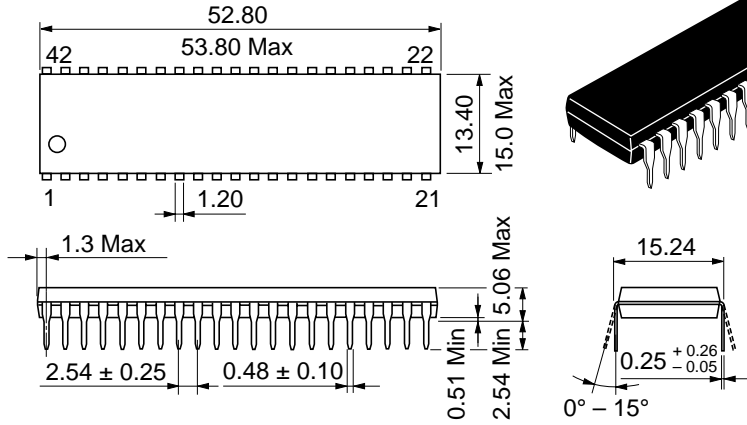
Notes: 1. This device is used ATD (Address Transition Detector). Therefore, transfer either \overline{CE} or address (A19 to A0) after power up to 4.5V.

HN624416 Series

Package Dimensions

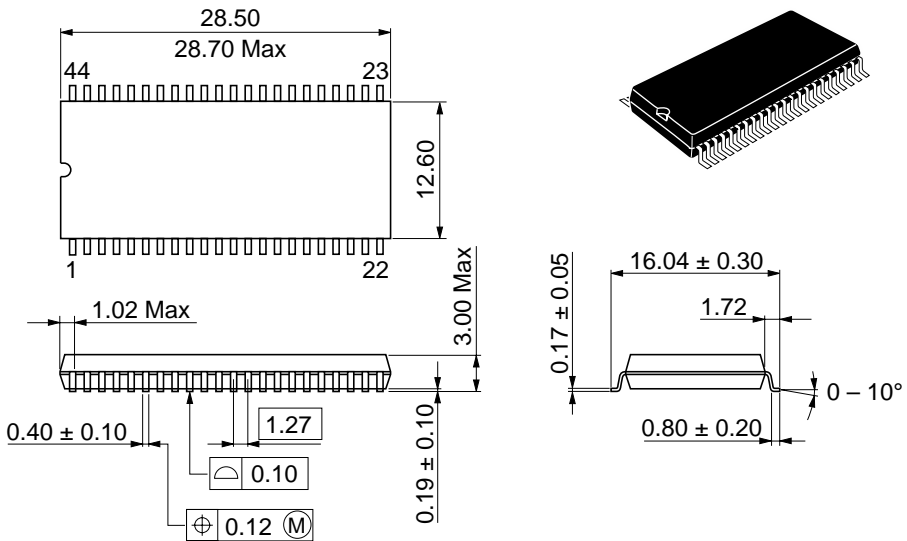
HN624416P Series (DP-42)

Unit: mm



HN624416FB Series (FP-44D)

Unit: mm



Package Dimensions (cont)

HN624416TT Series (TTP-44D)

Unit: mm

